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Graphene Etching on Well-Defined Solid Surfaces

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1. Introduction

Graphene is a two-dimensional material with hexagonal carbon network, and multilayer of graphene has been well-known as graphite. In 2004, it was reported that single-layer graphene can be exfoliated from graphite and observed using an optical microscope when a graphene sheet is attached on a 300 nm-thick SiO₂/Si wafer (Novoselov et al., 2004). Graphene exhibits an extremely high mobility, 200,000 cm²/Vs, which is 200 times as fast as that of Si. This high mobility was theoretically expected and then a mobility of 230,000 cm²/Vs was experimentally observed in a suspended graphene sheet (Bolotin et al., 2008). Since the sp² bonding of carbon is very strong, a mechanically and chemically stable two-dimensional network with few defects is realized in spite of an expectation that an atomic layer would be intrinsically unstable (Stolyarova et al., 2007). Owing to the small weight of carbon atom and the strong bonding between the atoms, thermal conductivity of graphene is in the highest group in the materials (Balandin et al., 2008). These features are effectively utilized when graphene is applied to electronic devices. Up to now, many reports have shown that graphene electronics is very promising for post-Si devices, but serious problems are also pointed out. For example, compatibility of high-quality graphene and wafer-scale processing is a big challenge. Although high-quality graphene can be obtained by exfoliation of graphene flakes from graphite, its size is small and the position control is almost impossible. Wafer-scale preparation of graphene sheets and their processing can be realized by epitaxial graphene on SiC (Berger, et al., 2004), chemical vapour deposition of graphene on a metal substrate (Sutter et al., 2008; Bae et al., 2010; Li et al., 2009), or coating of graphene oxide (Eda et al., 2008; Li et al., 2008). However, the quality of those graphene is not sufficient for high-performance devices.

In this article, we show our recent results about substrate engineering toward graphene integrated devices. We first describe properties and features of graphene on solid surfaces and then show strategy about etching of graphene, where “etching” is used for cutting of graphene sheets through chemical reactions. Based on this background, we show our experimental results about tight attachment of graphene onto oxide substrates, such as sapphire and titania, and characterize the interface properties between the graphene sheet and the substrate surface. Finally, we show processing of graphene sheets attached on the sapphire surfaces using the atomic structures on the substrate surface as templates. Here, we would like to emphasize that the interface properties between the graphene sheet and the substrate is particularly important and that etching and local properties of the graphene

sheets can be controlled by utilizing the atomic structure of the substrate surface because graphene consists of a single-atomic layer and, therefore, their shape and properties are strongly influenced by the substrate structure and properties.

2. Substrate strategy in graphene devices

Silicon integration technology has been exponentially developed according to the well-known Moore's law (Moore, 1998), but it is now expected that such trend will be saturated in the near future. To keep the present trend, there are two approaches: one is improvement of the conventional technology by introducing new materials and processing, and the other employment of completely different concept of device architecture. The former category called "more Moore" is based on down-scaling of the device processing. Silicon on insulator (SOI) (Yoshimi, 2002) has a long history and started with silicon on sapphire (SOS), in which a silicon thin layer is epitaxially grown on a sapphire surface. After the proposal of SOS, SIMOX (separation by implanted oxygen) and direct wafer bonding techniques have been developed. The SOI devices exhibit small parasitic capacitance and facile availability of full-depletion operation mode in MOSFET (metal-oxide-semiconductor field effect transistor). Therefore, device performance using SOI is almost equal to that of down-scaled devices fabricated by the next generation processing. On the other hand, concept of the latter class called "more than Moore" has not been established, but nanocarbon is one of the promising candidates of the materials for future electronic devices. Carbon nanotubes (CNTs) (Iijima, 1991) have been attracting great interest as alternative materials of Si because of its high electron mobility, thermal stability, high durability against a high electric current density. Though CNT-FETs have been developed for last 15 years and their high potential performance has been reported (Tan et al., 1998; Collins et al., 2001), reliable handling and position control are still difficult towards integrated devices. Moreover, separation of semiconducting CNTs from metallic ones is required. Therefore, industrialization of CNT FETs in the near future is thought to be questionable.

Graphene possesses compatibility with the planar technique that has been playing a principal role in the Si integration technology. It means that we can utilize the sophisticated technology, such as lithography, in fabrication of graphene devices, though the concrete image of the graphene device is still ambiguous at this moment. Since there is no structural variation in graphene, electronic structure is uniquely controlled within the two-dimensional plane (Stolyarova et al., 2007). As can be seen in graphene separated from natural graphite, atomic network of graphene is almost defect-free. We can conclude that graphene is a suitable material for integrated electronic devices. Graphene is flexible and deformed by a small external force though the bonding between individual atoms is extremely strong. Moreover, the electronic properties of graphene strongly depend on its shape, size, and deformation (Geim, 2009; Ertler et al., 2009). Therefore, graphene should be tightly fixed on the substrate in device applications that require a high reliability. For example, electrical conductivity of epitaxial graphene on SiC single crystal depends on the direction with respect to the atomic steps on the SiC surfaces (Yakes et al., 2010; Odaka et al., 2010). In the actual devices, graphene should be attached on an insulating substrate, which we call graphene on insulator, GOI. Requirements to GOIs are atomically defined surfaces to obtain a flat graphene without deformation and tight attachment between the graphene sheet and the substrate, so that variety of device processing can be utilized. In addition to the compatibility with the conventional technology, a new processing with atomic level

resolution is desired to effectively utilize the mono-atomic scale of graphene. Finally, wafer-scale GOIs are required in the industrialization stage. A wafer-scale integration of graphene devices has already been proposed (Lee et al., 2010). Though this requirement is indispensable, we focus on the interface control in small-size GOIs and etching to obtain various patterns of graphene sheets in this article.

Concerning adhesivity between graphene sheets and solid surfaces, it is well-known that apparent height of graphene attached on the SiO₂/Si substrate is much greater than the interlayer spacing of graphite, 0.34 nm, in air (Stolyarova et al., 2007; Ishigami et al., 2007; Geringer et al., 2009). Since chemical bond is not formed between graphene and SiO₂, atomic-scale roughness on the SiO₂ surface seems to prevent tight attachment at the interface. To form a device-level interface with non-covalent bonding, atomically flat substrate surface is required. Under this condition, Van der Waals force effectively works and adhesivity similar to that in epitaxial growth can be obtained, as appears in graphite. This requirement can be realized by using single crystals with atomically flat terraces and regularly ordered atomic steps. Techniques to well-ordered atomic steps have been developed in semiconductor technology, such as Si and GaAs.

Fig. 1 shows our substrate strategy towards GOI devices. From the above discussion, it can be concluded that the materials for GOI substrate should be highly insulating, and their surfaces are covered with flat terraces accompanied with well-ordered step arrangement. Some metal oxides satisfy these requirements, such as sapphire (Al₂O₃), titania (TiO₂), quartz (SiO₂). In particular, sapphire is highly insulating and chemically stable. On sapphire surfaces, step arrangement can be well-controlled, which means that atomically flat terraces can be obtained on the entire substrate surface. Since sapphire is an oxide crystal, no further oxidation occurs and, therefore, terraces can be kept atomically flat through processing in air and in solution. Another important advantage of sapphire is that production technique of high-quality large-scaled wafers has been established in SOS using Si and light-emitting devices using nitride semiconductors. In this article, we use sapphire as the most suitable substrate for GOIs and briefly show results of graphene attachment on titania and quartz surfaces.

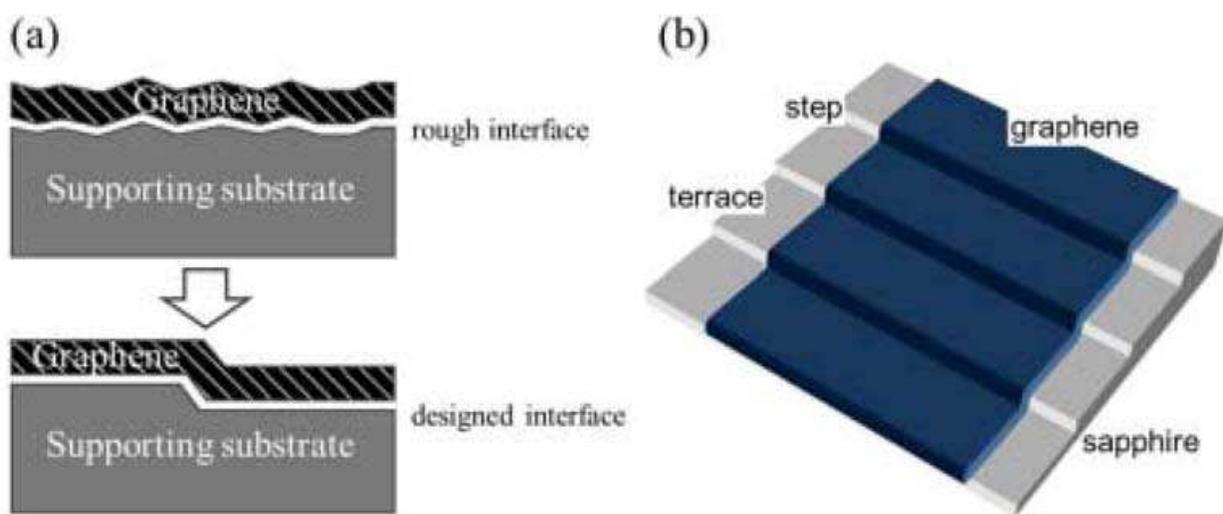


Fig. 1. Substrate strategy towards graphene-on-insulator devices. (a) Cross-sectional views of the interfaces and (b) GOI using substrates that exhibit well-ordered step/terrace structure.

3. Processing strategy in graphene devices

Si-MOSFETs have been developed with down-scaling that includes reduction of channel depth and the gate oxide thickness. Graphene is originally single-atomic layer and has no room for further reduction. In other word, reduction of lateral size to atomic level is required to make full use of the features of graphene. Because conventional lithography uses thick polymer resist masks, etching of graphene using such masks cannot be applied to atomic-scale processing. The processing strategy based on the substrate engineering may be divided into two methods. One consists of incorporation of strain distribution into the graphene sheet by locally bending the sheet using substrate patterns and modulation of the electrical, mechanical and chemical properties of the graphene sheet. The other is cutting graphene to separate individual device areas without thick resist masks. The former strategy has recently been proposed, where topographic patterns on the substrate is used to locally deform the graphene sheets (Pereira & Neto, 2009). This strategy is promising because graphene can be easily deformed owing to its flexibility and the properties can be controlled by the deformation. In other techniques for functionalization of graphene sheets, cutting accompanied with bond breaking or chemical termination accompanied with defect formation is used. The former strategy based on deformation of graphene also has advantage that the whole process can be done only by patterning of the substrate without handling graphene itself. However, the isolation between individual devices, which is one of the important elements in the integrated devices to avoid crosstalk, is not perfect. In the etching, a couple of technique has been proposed. One is crystallographic etching where metal nanoparticles, such as Fe, Co, and Ni, placed on a graphene surface are used as catalyst (Datta et al., 2008). The graphene sheet is located in H₂ or H₂-containing flow at elevated temperatures. Carbon of graphene is reacted with hydrogen gas and CH₄ gas forms by the following reaction:



Since CH₄ gas is quickly released to the vapour phase, graphene etching proceeds. The notable feature of this etching mode is that the etching occurs along the zigzag edge of graphene because the energy required for removal of the carbon atoms along the zigzag edge is much larger than that along the armchair edge (Ci et al., 2008). As a result, crystallographic etching occurs and atomically straight trenches directed to one of three zigzag edges form. The movement of the metal nanoparticles is sensitive to deformation of graphene (Campos et al., 2009). For example, when a metal nanoparticle approaches a trench formed in advance, its movement direction is changed because graphene lattice near the pre-existing trench is deformed owing to instability of graphene edges. This is a remarkable feature because graphene nanoribbon, which is one of the methods to open bandgap in graphene electronic structure (Han et al., 2007), can be self-assembled. Moreover, since the etching begins from the graphene edge, etching patterns can be controlled by the arrangement of the nanoparticles (Ci et al., 2009). Another proposal to cut graphene is oxidation of graphene in O₂ atmosphere at elevated temperatures using Ag nanoparticle as catalyst by the following reaction (Severin et al., 2009):



In this technique, crystallographic etching does not occur and irregular trench forms. However, this technique has an advantage that the reaction temperature is lower than that in the hydrogenation reaction shown in the reaction (1).

Fig. 2 shows our processing strategy for graphene devices. First, we employ etching mode based on the reaction expressed by eq. (1) and Fe nanoparticles are used as catalyst. In the application of graphene to electronic devices, graphene should be tightly attached on the substrate surface. Since the etching of graphene is strongly influenced by the externally introduced deformation, we can use the deformation patterns introduced by the topography of the substrate surface. In this strategy, atomic structures, even a single-atomic step, can produce an abrupt deformation in graphene when the graphene film is tightly attached to the terraces on both side areas of the atomic step. As shown later, we have developed etching of few-layer-graphene (FLG) utilizing deformation introduced into graphene from atomic structure of the substrate surface. Another factor of the etching based on atomic structure of the substrate surface is interaction between the metal nanoparticles and specific structure on the substrate surface. Directional control of the etching is also shown in section 6.

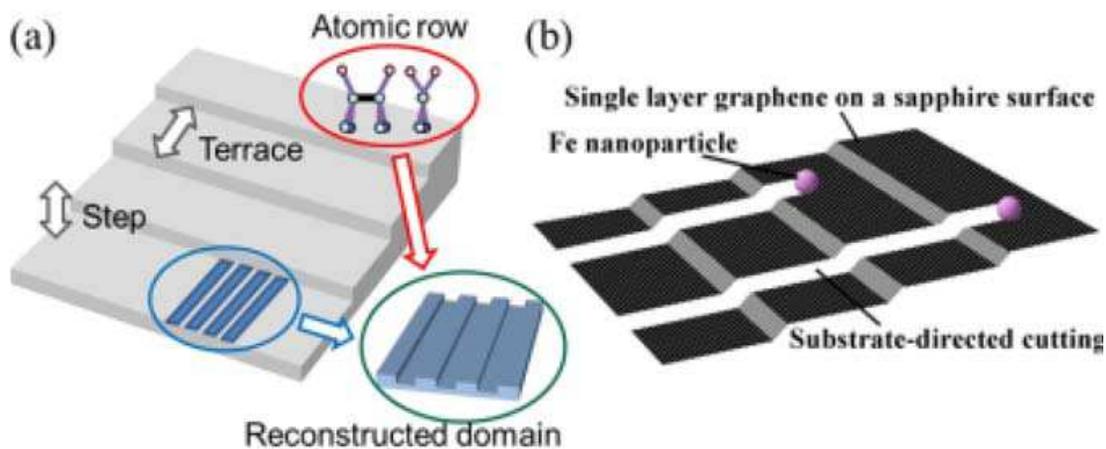


Fig. 2. Processing strategy of graphene-on-insulator. (a) Atomic structure control on substrate surface and (b) etching controlled by the substrate.

4. Graphene on single crystalline oxides

We show morphology and interface characterization of FLG or graphene on single crystalline sapphire surfaces (Tsukamoto & Ogino, 2009). In this study, we used (0001) and (1-102) surfaces, and atomic step arrangement is controlled in advance of the attachment process. Fig. 3 shows AFM images of typical step arrangement on a sapphire (0001) surface. Just after polishing and chemical etching, the atomic steps are randomly distributed, as shown in Fig. 3(a). After annealing in air at 1000 °C, regularly ordered atomic steps are obtained, as shown in Fig 3(b). In the equilibrium state, single height atomic steps are separated by terraces with similar width that is uniquely determined by the macroscopic miscut angle of the substrate. Upon annealing at 1400 °C, a couple of atomic steps are gathered and form step bunches, as shown in Fig. 3(c). This is one of the powerful tool to control deformation in the attached graphene sheets because the number of steps in step-bunches, which is controlled by the annealing temperature, directly determines the magnitude of deformation introduced into the attached graphene sheet. Similarly, step arrangement can be controlled also on sapphire (1-102) surface.

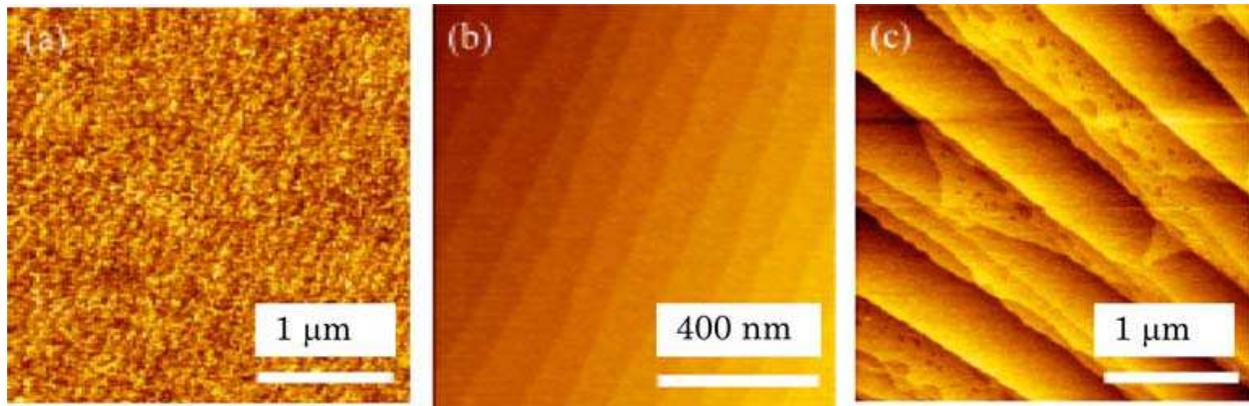


Fig. 3. AFM images of typical step arrangement on sapphire surfaces. (a) Randomly distributed steps, (b) uniformly distributed single-atom steps, and (c) bunched steps.

Fig. 4 shows atomic force microscopy (AFM) images of graphene on a sapphire (1-102) surface, where graphene flakes were mechanically exfoliated from highly oriented pyrolysis graphite (HOPG) and attached on the sapphire surface. Fig. 4(a) shows topography and Fig. 4(b) frictional force image. Before graphene attachment, the sapphire surface was annealed at 1000 °C in air and atomically flat terraces separated by ordered step arrays were formed. Just before the attachment, sapphire surface was cleaned using a $\text{H}_2\text{SO}_4\text{-H}_2\text{O}_2$ solution. Height of the graphene flake in Fig. 4(a) is 0.35 - 0.38 nm, which is similar to the layer spacing in HOPG. As previously reported, when graphene flakes were attached on amorphous SiO_2 layer prepared by thermal oxidation of Si, heights of 0.6 - 0.8 nm were observed (Stolyarova et al., 2007; Ishigami et al., 2007; Geringer et al., 2009). This means that atomically uniform contact is not obtained in the graphene/ SiO_2 system. Since integrated electronic devices are fabricated through hundreds of processing including wet cleaning, thermal process and etching, atomically uniform contact is required. Our experimental results show that single crystalline insulating substrate is much more suitable than amorphous substrates, though generally SiO_2 is an ideal insulator. Frictional force image shown in Fig. 4(b) was taken simultaneously with topographic image, where the brightness corresponds to magnitude of the frictional force. In this operation mode, the cantilever of AFM is laterally scanned, and topographic and frictional force images are taken from the vertical bending and the lateral torsion of the cantilever, respectively. Figure 5(a) shows origin of the frictional force in AFM observation in air. The frictional force on solid surfaces exposed to air is usually determined by the resistance to the cantilever movement induced by the meniscus formed between the cantilever tip and the surface. Therefore, the observed frictional force is larger when the surface is more hydrophilic. In our experiment, the cantilever tip is made by Si_3N_4 , which is hydrophilic. Since the sapphire surface used in our experiment was treated by acid, it is terminated with OH group generated by the acid treatment. Both the sapphire and the cantilever surfaces are hydrophilic, and a large meniscus forms. Therefore, the observed frictional force on sapphire surface is relatively large, as shown in Fig. 5(b). Graphene, on the other hand, is an extremely hydrophobic material and, therefore, exhibit a low frictional force, as shown in Fig. 5(b). Thus, we can easily distinguish the graphene surface from the substrate. This is a useful tool particularly in graphene etching, because we can directly determine whether the bottom of the trench is sapphire surface or remaining graphene layer surface. Moreover, the spatial resolution of hydrophilic areas inside a large hydrophobic area is higher than the topographic image

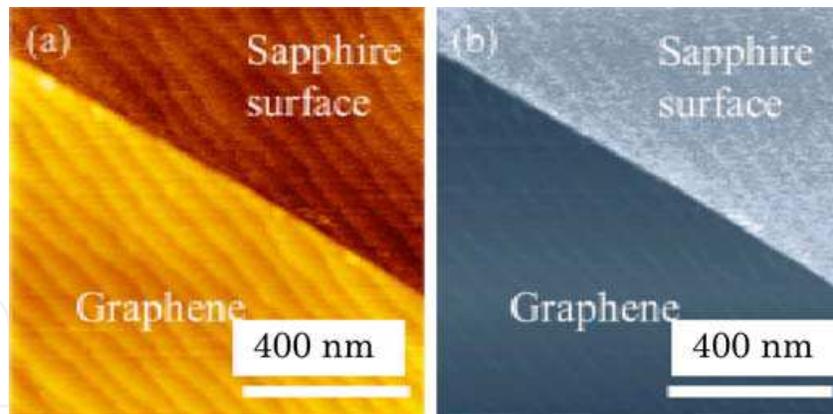


Fig. 4. Atomic force microscopy (AFM) images of graphene attached on a sapphire surface. (a) Topography and (b) frictional force image.

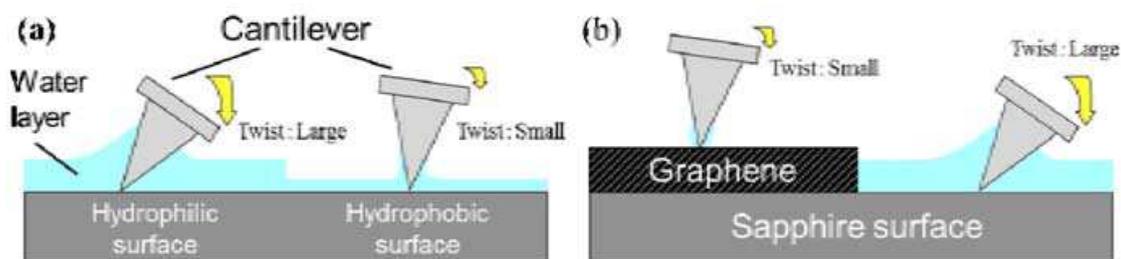


Fig. 5. Origin of the frictional force in AFM observation. (a) General explanation and (b) sapphire surface partially covered with graphene.

because frictional force is generated even on an area smaller than radius of the tip apex. From the above discussion, we can conclude that the top-right area in Fig. 4, which exhibits a larger frictional force, is a sapphire surface and the bottom-left a graphene flake one. In Fig. 4(a), the step/terrace structure on the substrate surface is almost exactly reproduced on the graphene surface. This means that, owing to atomically uniform contact of graphene on single-crystalline sapphire surfaces, atomic-level topography can be precisely transferred to the graphene surface. Topographic control of the suspended graphene surface is almost impossible owing to its large flexibility. On the other hand, atomic-level control on solid surfaces has been highly developed mainly in semiconductor surfaces. On Si surfaces, formation mechanism of atomic-step arrangement was intensively studied (Ogino et al., 1999a) and artificial positioning of steps is realized. One example is a wafer-scale control of atomic steps on Si(111) surface where position of atomic-steps or step bunches can be uniquely determined (Ogino et al., 1995). When small hole arrays are pre-patterned on Si(111) surfaces, atomic steps on the surface are rearranged according to the hole pattern during high-temperature annealing. By utilizing these techniques, arrangement of self-assembled nanostructures, such as Ge quantum dots, is also controlled because nucleation of nanostructures is often initiated at the steps (Ogino et al., 1999b). In GOI, however, Si substrate is not suitable because Si itself is semiconducting. Although thermally grown SiO₂ layer on Si is a good insulator, it is amorphous and does not possess well-defined atomic structures. On the other hand, sapphire is an insulating oxide and exhibits well-ordered atomic steps. Wafer-scale control of atomic step arrangement was also demonstrated, as shown in Fig. 6. Atomic structure on sapphire surfaces is preserved in air or in water as well as in vacuum because no further oxidation occurs. We, therefore, can transfer topography of well-controlled sapphire surface to graphene surface attached on insulating substrate.

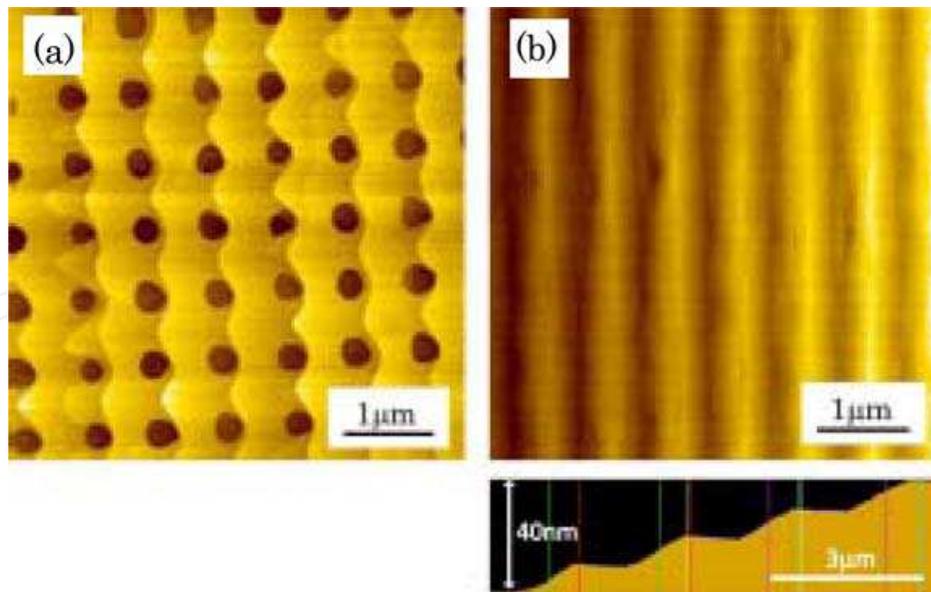


Fig. 6. Artificial control of step arrangement on sapphire surface using small hole arrays on the substrate. (a) Step rearrangement during annealing and (b) final step arrangement.

As previously described, sapphire is the best candidate for GOI substrate. However, some other oxides are possibly useful for specific applications. We attached graphene on titania (TiO_2) or quartz (SiO_2) single-crystal surfaces and observed the surface morphology. Fig. 7 shows topography of graphene flakes attached on (a) a $\text{TiO}_2(001)$ surface and (b) a $\text{SiO}_2(100)$ surface. On both surfaces, buried atomic-steps appear on the graphene flake surfaces. TiO_2 is well known as a catalytic material of photochemical reaction. It was reported that graphene oxide can be effectively reduced on TiO_2 particle surfaces (Williams et al., 2008) and it suggests that graphene on TiO_2 single crystal has potential applications in functional devices equipped with photochemical reactivity. Quartz is also a good material for radio frequency oscillator and graphene modification of quartz surface may have potential applications to specific oscillation functionality. Mica is a layered crystalline material similar to graphite and a large area of atomic-level flatness is obtained. Using mica, flat graphene surfaces can be obtained (Lui et al., 2009).

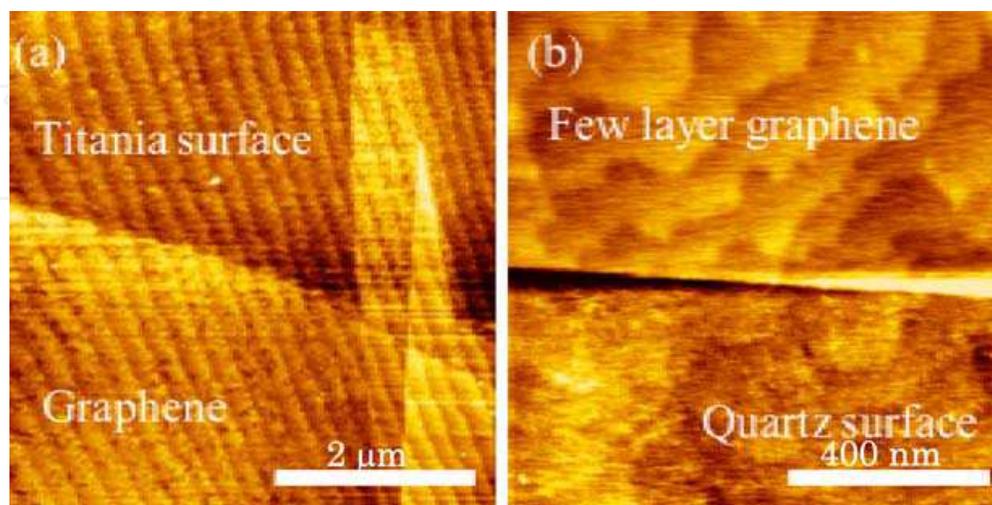


Fig. 7. AFM images of topography on graphene flakes on single crystalline (a) $\text{TiO}_2(001)$ and (b) $\text{SiO}_2(100)$ surfaces.

We have described physical properties of graphene-substrate interfaces. Another important factor is chemical properties of the interface. Here, we demonstrate a chemical effect of the sapphire substrate on graphene bonding using phase-separated sapphire (0001) surface (Isono et al., 2010). Generally, atomic steps originating from miscut of the surface exist even when the surface is carefully flattened. When a sapphire (0001) surface is annealed at high temperatures above 1300 °C, steps on the surface are gathered and form step bunches. If the miscut direction is rotated from the direction that would generate crystallographically straight steps, step arrangement consists of straight step bunches and crossing steps that is required to keep the macroscopic miscut direction, as shown in Fig. 8(a). We call this type of surface a cross-stepped surface. In the case of sapphire (0001) surface, the most stable crystallographic step direction is that perpendicular to [1-100] and the second that to [1-102]. Fig. 8(b) shows an AFM image of cross-stepped sapphire surface in air. On this surface, ellipsoidal domains, which we call domain A, are observed inside terraces surrounded by step bunches and crossing steps. Fig. 8(c) shows frictional force image of the same area as that shown in Fig. 8(b), where domain A exhibits lower frictional force than the other terrace areas, which we call domain B. This means that domain A is more hydrophobic than domain B. According to previously published papers, sapphire (0001) surface is terminated with Al atoms (Hass et al., 1998) and those Al atoms are terminated with OH groups after the acid treatment, which we used to clean the surface. Therefore, sapphire surface after the acid treatment is generally hydrophilic, as experimentally observed. However, the chemical properties of domain A are much different. We think that domain A is, at least partially, terminated with epoxy groups, and OH group termination, which makes the surface hydrophilic, is suppressed. Domain A grows upon high temperature annealing and the growth is saturated owing to increase in the peripheral stress energy. This kind of phase separation on a solid surface has been reported on other systems (Jones et al., 1996; Komeda & Nishioka, 1997), and it is widely accepted that this occurs to minimize the surface energy.

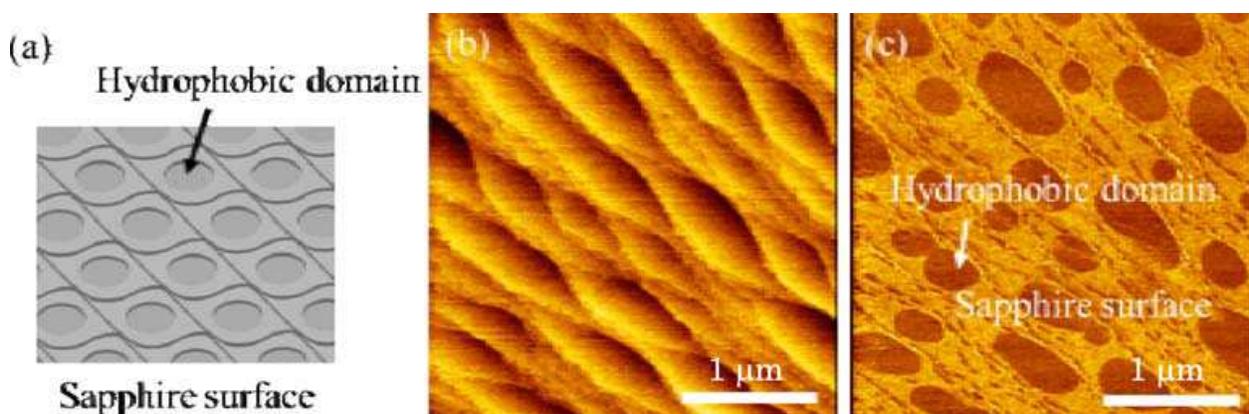


Fig. 8. Cross-stepped sapphire (0001) surface. (a) Schematic view, (b) AFM topographic image, and (c) frictional force image.

Fig. 9(a) shows surface topography of an as-deposited FLG flake on a phase-separated sapphire (0001) surface. On the domain A, flat FLG surface is observed whereas roughness at atomic-level height appears on domain B. Fig. 9(b) is a model for the surface topography. Although domain A is relatively hydrophobic, low-density of water molecules still exist. Since graphene is strongly hydrophobic, graphene and domain A are bonded by a hydrophobic interaction. Therefore, residual water molecules at the interface are swept out

and move to the interface between graphene and relatively hydrophilic domain B. Therefore, the amount of interface water in domain B, which is originally larger than that in domain A, further increases. In a recent paper, observation of single- or few-layer of water molecules was reported between graphene and mica surfaces (Xu et al., 2010). In our case, water layer thickness is probably larger than monolayer of water molecule, and water droplets are also observed. It is known that graphene is impermeable even for He gas (Bunch et al., 2008). In Fig. 9(a), a hydrophobic domain is surrounded by hydrophilic domains. If also opposite domain pattern is obtained, we can confine any species of atom or molecule beneath a graphene flake and directly observe single molecule behaviour because graphene deforms even on a single molecule, as shown in Fig. 9(a). Therefore, graphene on a phase-separated sapphire surface is a good stage to observe single atom or molecule dynamics using a scanning probe. In the case of GOI, confinement of any molecules at the interface should be avoided.

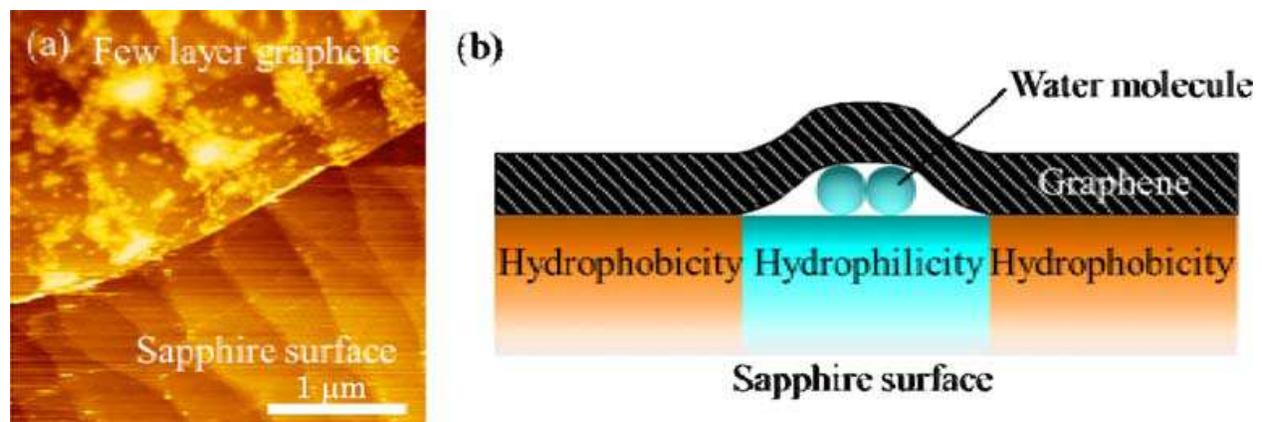


Fig. 9. Graphene on phase-separated sapphire (0001) surface. (a) AFM topographic image, and (b) interface model.

5. Etching of graphene on sapphire substrate

In this section, we show our experimental results about graphene or FLG etching using the reaction expressed by eq. (1) (Tsukamoto & Ogino, 2010). First, sapphire (1-102) substrates were thermally annealed above 1000 °C to obtain well-defined step-terrace structure, and then graphene or FLG exfoliated from HOPG was attached on the substrate. Fe nanoparticles as catalyst were prepared from isopropanol solution of $\text{Fe}(\text{NO}_3)_3/9\text{H}_2\text{O}$. The solution was spin-coated on the graphene-attached substrate and then inserted in a furnace after drying. Fe oxide nanoparticles were formed during raising temperature and then reduced to metal nanoparticles by H_2 gas at the initial stage of etching. Graphene etching was performed at 900°C for 10 or 45 min, and the surface morphology was observed by AFM.

Fig. 10(a) shows AFM image on a 30 nm thick FLG surface after etching, where a wide trench (trench A) and a narrow one with a turning point (trench B) are observed. From the cross sectional profiles, etching depth was found to be only monolayer of graphene. A nanoparticle, probably a Fe nanoparticle, is observed at the etching front of the trench A. The trench A clearly demonstrates that the etching proceeds with movement of the metal nanoparticles, and initial position and movement direction of the metal nanoparticles are essential for designing etching patterns. Since the FLG shown in Fig. 10(a) is enough thick,

the buried step-terrace structure is hidden under the FLG surface. Therefore, the substrate surface exhibits almost no effect on the etching mode, and crystallographic etching, which has already been reported, dominantly occurs. However, the trench B changes its etching direction by 120 degree around the deformation of the surface layer indicated by a white broken circle. This suggests that the etching direction, therefore the movement of the catalytic nanoparticles, is strongly affected even by small deformation of the top graphene layer. Fig. 10(b) shows an AFM image on which triangular graphene islands are regularly ordered. In this case, the FLG is enough thick for crystallographic etching to occur. First, a graphene belt was formed by parallel crystallographic etching and another Fe nanoparticle moved inside the belt. The Fe nanoparticle is reflected by 60 degree when it reaches the trench. Therefore, multiple reflection occurs and triangle islands are sequentially formed. The present etching mode is useful to fabricate regular patterns though the shape and direction are limited to triangle and three crystallographic directions, respectively.

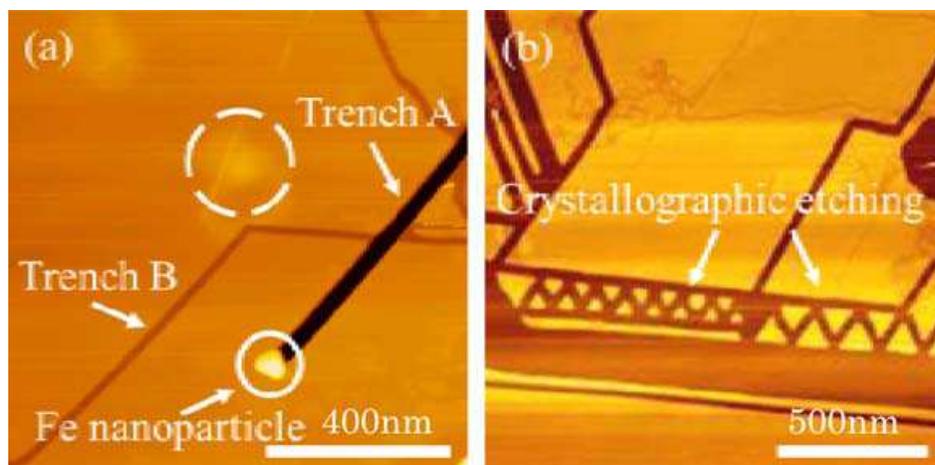


Fig. 10. (a) Etching processes of few-layer-graphene (FLG) along the crystallographic directions, (b) example of regular pattern formation.

Fig. 11(a) shows an AFM image of etching features on 6 nm thick FLG on a sapphire surface, where the etching conditions were same as those for Fig. 10. In this image, etching directions are roughly determined by the crystallographic orientations, but the formed trenches are not straight but fluctuated. This suggests that the etching mode in Fig. 11 was affected by two factors: crystallographic orientations of graphene and atomic roughness on the substrate surface. Fig. 11(b) shows an etching pattern of 3 nm thick FLG on a sapphire surface on which step/terrace structure appears. On this surface, trenches along crystallographic orientation are observed. The whole etching pattern was formed by reflection of Fe nanoparticles at both a pre-existing trench edge indicated by white arrows A and buried steps indicated by white arrows B. Since FLG is tightly attached on the sapphire surface with regularly ordered steps, large strain is locally introduced just above the atomic steps. The observed fluctuation in Fig. 11(a) is attributed to the strain induced by the roughness of the substrate surface and its major contribution is atomic steps. In Fig. 11(a), we observe some characteristic etching patterns. The Fe nanoparticles turn their moving direction at a pre-existing trench, as indicated by (A) in Fig 11(a), and never cross the trench. When there is no catalytic particle inside a triangular island surrounded by trenches, no further etching occurs, as indicated by (B). On the other hand, if catalytic nanoparticles remain inside the triangular island, they continue to divide the triangular island and, in some cases, triangular

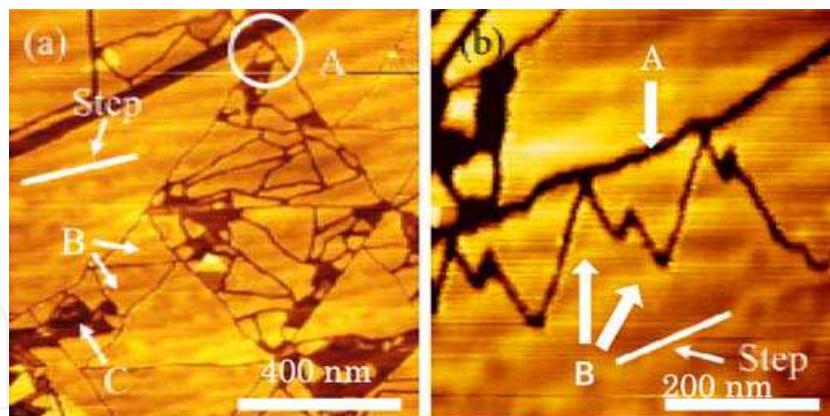


Fig. 11. Etching mode of a FLG, in which crystallographic etching is modified by atomic structure on the substrate surface. (a) Various patterns in this etching mode and (b) reflection of Fe nanoparticles at buried steps.

voids are finally formed, as indicated by (C) in Fig. 11(a). These results show that initial arrangement of catalytic nanoparticles is the key factor to design the FLG island patterns.

Fig. 12(a) shows another AFM image of etching pattern on 6 nm thick FLG attached on a sapphire surface. On this surface, two trenches are observed. The relatively wide trench indicated by A is confined in an area above single buried terrace and consequently the macroscopic direction is parallel to the steps. However, the local direction of the trench A is fluctuated according to the crystallographic orientations inside the terrace. In Fig. 12(a), trench B with relatively narrow width is also observed. This is almost completely straight, which means trench B follows one of the crystallographic orientations though the FLG thickness is same as trench A. This suggests that influence of buried atomic steps on the etching shape is larger for larger Fe nanoparticles than for a smaller one, or that movement of a smaller nanoparticle is more strongly subject to crystallographic orientation. Fig. 12(b) shows an AFM image on another area on the same sample, where an almost straight trench along a single step is observed. From the above experimental results, we can conclude that the FLG etching is controlled by two factors; crystallographic orientations of the FLG and atomic structure on the substrate surface. As previously mentioned, we have a variety of techniques to artificially design atomic structures, in particular step arrangement, which has been developed in semiconductor surfaces. Therefore, the patterning technique of FLG based on substrate engineering is promising for future integration of graphene or FLG devices.

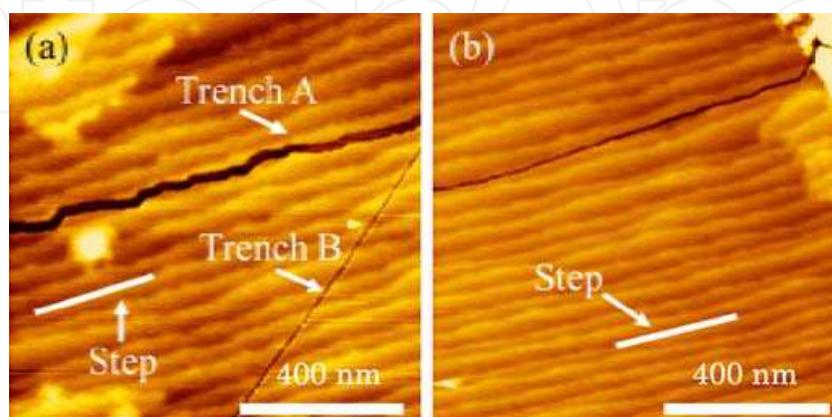


Fig. 12. Graphene etching subject to buried steps. (a) Etching confined in an area above single terrace, (b) etching along a single step.

In the etching of FLG, only the topmost layer of FLG flake is etched and the trench depth is a single layer of graphene. This is because etching is always initiated from graphene edge and never on the FLG terrace, at least within our experiment. Next, we describe etching mode of single layer of graphene on sapphire (1-102) surfaces that exhibits wide terraces. Upon annealing at 1000 °C for 3 h in air, a comb-shaped pattern appeared on the terraces, as shown Fig. 13(a), where the sample was cleaned using H₂SO₄ and H₂O₂ mixed acid. From the cross-sectional profile of this pattern, we found that the boundaries between bright (high) and dark (low) areas are not atomic steps, but the height difference is smaller than the unit step height. In the frictional force image, difference in the hydrophilicity is clearly observed. This means that the stripe domains exhibit different surface chemistry from each other. This is similar to the phase separation that we previously found on sapphire (0001) surfaces shown in Fig. 8, where there are two chemically different domains (Isono et al., 2010). Because the surface was treated with acid, it is more or less hydroxylated. The observed difference in hydrophilicity is attributed to a difference in OH group density. This means that the atomic structures, or bonding configurations of surface termination, on these domains are different and therefore exhibit different reactivity for acid. Generally, surface reconstruction induces surface strain. If two possible bonding configurations that exhibit different surface strain, phase separation occurs to reduce the strain energy. On a Si(001) surface, stripe domain structure similar to the comb-shaped pattern shown in Fig. 13(a) is observed (Jones et al., 1996; Komeda & Nishioka, 1997). Therefore, the comb-shaped pattern is attributed to a difference in atomic structure on the surface. Fig. 13(b) shows an AFM image of an etching pattern of single layer of graphene attached on the phase-separated sapphire surface, where the etching procedure using Fe nanoparticles was same as the previously-described experiments. On this surface, etching mode controlled by the crystallographic orientations or step of the substrate is not observed. However, a new etching mode appears, where the etching direction is almost perpendicular to the steps. There are two possible explanations for this etching mode. Since the graphene is a single-atomic layer, Fe nanoparticles move directly on the sapphire surface and the movement is possibly controlled by the interaction between the Fe nanoparticles and the substrate surface. In this explanation, Fe nanoparticles interact with the sapphire surface through comb-shaped domain pattern itself or atomic structure along the comb-shape. Another explanation is based on the strain induced into the graphene layer from the comb-shaped surface. In this case, etching direction is determined by the strain distribution on the graphene layer. We speculate that the comb-shaped pattern is directed to a particular crystallographic orientation and the movement of the Fe nanoparticles is controlled by the atomic structure along the same direction as comb-shaped pattern. This is similar to directional growth of carbon nanotubes (CNTs) on the sapphire surface, where CNTs recognize the atomic structure on the sapphire surface and grow along specific directions (Han et al., 2005; Ago et al., 2006).

In Fig. 13(b), two trenches parallel to each other are observed in the bottom area as well as an isolated trench in the top area. In the application of graphene to electronic devices, bandgap opening is thought to be crucial, and nanoribbon formation is one of the most promising approaches for it. Moreover, functional devices utilizing graphene edges have been proposed (Barone et al., 2006; Yan et al., 2007). The directional etching observed in Fig. 13(b) can be applied to formation of graphene nanoribbons. In this application, site and density control of catalytic nanoparticles again plays an important role.

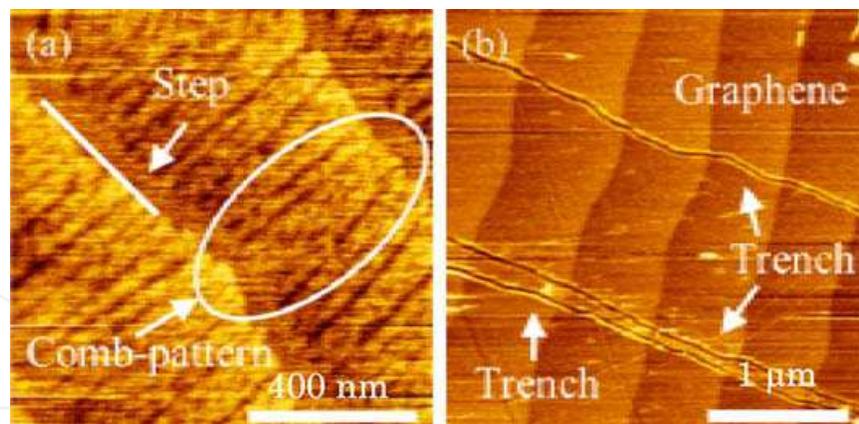


Fig. 13. AFM images of (a) phase separation on sapphire surface and (b) etching pattern of graphene attached on the phase-separated surface.

6. Summary

Graphene possesses tremendous potential for electronic devices owing to its high carrier mobility, high thermal conductivity, and large mechanical strength in spite of a single atomic layer material. In the application of graphene to reliable devices, graphene, which is too flexible for its devices to keep the stable performance, should be tightly fixed on a solid surface. Since such graphene sheet is single or few atomic layer, atomic-level structure and chemistry on the substrate surface directly influences the properties of the attached graphene sheets. Therefore, the selection of substrate is one of the important issues in graphene devices. We proposed sapphire as a substrate for integrated graphene devices because of its excellent insulating properties, high quality developed in the production of various devices using nitride semiconductors, and atomic level controllability of the surface. We have demonstrated that graphene or FLG can be tightly attached on the sapphire surface. Similar results have been obtained also on other single-crystalline oxides, such as quartz and titania surfaces, though their application targets are probably different from integrated electronic devices. Graphene on these well-defined surfaces exhibits buried step/terrace structures. Modulation of graphene shape using atomic structures on the substrate surface is promising as an alternative approach to functionalize the graphene layers. Development of graphene processing is also required for realization of the integration. We have demonstrated that etching using catalytic nanoparticles is powerful tool for graphene tightly attached on the well-defined substrates. In this technique, we can utilize etching mode using surface structures of the substrate in addition to crystallographic etching, which has been already proposed. Before concluding this chapter, we have to refer to large-scale formation of graphene layer on an insulating substrate, which is believed to be a critical issue toward wafer-scale processing of graphene. Since large-scale high-quality graphene sheet formation is a challenge, we also have to search another approach in the integration strategy. One possible approach is self-arrangement of well-shaped graphene flake on specific sites on the substrate. Since the expected scale of graphene devices is 10 nm or smaller, large area will not be required for individual device areas. The important factor is precise arrangement of the graphene, and surface design of the substrates will be a key technique in this alternative approach.

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8. References

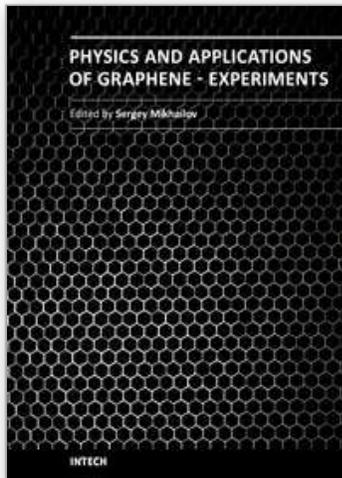
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