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Design and Simulation of Time-Pulse Coded Optoelectronic Neural Elements and Devices

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1. Introduction

Creation of intellectual systems is impossible without creation of proper tools, proper micro- and macroelement bases (Krasilenko et al., 1995, a; Krasilenko & Magas, 1999). So as any concrete technical decision is a compromise between many contradictory requirements taking into account solvable tasks, the creation of universal, effective, neural module as a macroelement base for neurobiologic (Krasilenko et al., 2002, a; Krasilenko et al. , 2001, a) is, probably, the future task. At the same time, searches for ways of creation of multifunction devices which work on new mathematical, logical, hybrid, neural, neural-fuzzy bases and others like that, especially on the basis of the biologically explained conceptions, will always be actual (Krasilenko et al., 2002, a; Levin, 1990, a; Shimbirev, 1990, a), because just life and time choose the most optimal solutions from all offered and existent.
The strategic direction of solution of various scientific problems, including the problem of creation of artificial intelligence (AI) systems, human brain simulators, robotics systems, monitoring and control systems, decision-making systems, as well as systems based on artificial neural networks, etc., becomes fast-acting and parallel processing of large arrays (2D) of data using non-conventional computational systems, matrix logics (multi-valued, signed-digit, fuzzy logics, continuous, neural-fuzzy and others) and corresponding mathematical apparatus (Krasilenko et al., 2001, a; Masahiko & Yatagai, 1997; Berger & Collings, 1997; Krasilenko et al., 1997,a; Leondes, 1998; Krasilenko, 1988,b). For numerous perspective realizations of optical learning neural networks (NN) with 2D structure (Masahiko & Yatagai, 1997) of recurrent optical NN (Berger & Collings, 1997) of the continuous logic equivalency models (CLEM) NN (Krasilenko et al. , 2001, a; Krasilenko et al., 1997,a; Leondes, 1998), the elements of matrix logic are required. Optic and optoelectronic technologies, methods and principles as well as corresponding element base provide attractive alternative for 2D data processing. These technologies and methods successfully solve problems of parallelism, input-output and interconnections. Signed-digit number system (SDNS) are considered to be most promising and widely used nowadays, among this systems we can find high-order systems, including the quaternion SDNS system (Krasilenko et al., 2001, c). The architectures based on the system embrace such features as high density of recording, they are less complicated and they contain few system components, stages of addition, etc. Only a few of them (Huang & Itoh & Yatagai, 1999) can

be used for processing of 2D data and perform wide range of needed arithmetic and logic operations (Guilfoyle & McCallum, 1996).

There exist a number of generalizations of continuous logic (CL) (Levin , 1990, a), (Shimbirev, 1990, a; Volgin, 1986). Among them we should note sequential logic, hybrid logic (HL), continuous discrete logic (CDL), controlled continuous logic (CCL) or predicate selective algebra (Volgin, 1986), fuzzy logic (Zadeh, 1965). In hybrid logic the threshold and dethreshold operations are basic, they realize transformations over continuous and discrete variables (Shimbirev, 1990, a). Hybrid logic (HL) is basic mathematical body for analysis and synthesis of hybrid (analog-digital) devices and systems. Functions max and min can be realized sequentially performing threshold and dethreshold operators, i.e. by means of hybrid logic (HL). Generalization of scalar two-valued logic on matrix case has led to intensive development of binary images algebra (BIA) (Huang et.al., 1989) and 2D Boolean elements for optic and optoelectronic processors (Huang & Itoh & Yatagai, 1999; Awwal & Iftekharuddin, 1999; Krasilenko et al., 2001, c; Guilfoyle & McCallum, 1996; Krasilenko et al. , 1988,a; Krasilenko et.al., 1991,a; Krasilenko & Dubthak, 1992). We would like to draw the attention to the fact, that both natural neurons and their more complex physical and mathematical models suggest discrete-analog and purely analog means for information processing with different level of accuracy, with the possibility of rearrangement of chosen coding system. This, in its turn, requires corresponding image neuron circuit engineering with programmable logic operations, with transition from analog to discrete processing, to storing etc. Thus, the search of means aimed at construction of elements, especially universal (at least quasi-universal or multifunctional) with programmable tuning, able to perform not only operations of two-valued logic, but other matrix (multi-valued, continuous, neuro-fuzzy, etc.) logic operations is very actual problem(Guilfoyle & McCallum, 1996).

Neuromodule, as it has been shown in works (Krasilenko et al., 1995, a; Krasilenko et al. , 2001, a; Krasilenko et.al , 1995,c) can serve such macroelement basis. Functioning of neural elements of such neuromodule must be described by future more generalized neurobiological (Krasilenko et al., 1995, a; Krasilenko et al. , 2001, a) or the most generalized at present time logics: continuous, hybrid, neural, fuzzy, neural-fuzzy and other logics (Krasilenko et al., 1995,a; Krasilenko et al., 2002, a; Krasilenko et al. , 2001, a; Levin , 1990, a; Shimbirev, 1990, a; Krasilenko et.al , 1995, c).

One of perspective directions of researches on creation of macrobase neural modules with intelligence and quasiuniversality, and which operate on afore-mentioned new mathematical bases, is the use of conception of time-pulse coded signals and the offered approach to creation of different elements and structures for effective and highly productive 1D and 2D data processing (Krasilenko et.al., 2004, a; Krasilenko et.al, 2004, b; Krasilenko et.al., 2005, a). Prospects of new optical and optoelectronic technologies (Masahiko & Yatagai, 1997; Guilfoyle & McCallum, 1996; Baukens et.al., 1997) are limited to narrow special processors. Therefore, to our mind, the central problem of new untraditional parallel architecture, picture logic structures and elements creation, neurocomputers, is the problem of logical universal and intelligence vector-matrix functional base (Krasilenko et al., 1995, a; Krasilenko & Magas 1999; Krasilenko et.al., 2004, a; Krasilenko et.al., 2005, a; Krasilenko et.al , 1995, c; Krasilenko et.al., 2005, b).

One of promising directions of research in this sphere is the application of time-pulse-coding architectures (TPCA), that were considered in works (Krasilenko et.al., 1991,a;

Krasilenko & Dubthak, 1992; Krasilenko, 1991,b) these architectures were generalized in (Krasilenko et al., 1995, a). The time-pulse representation of matrix continuous-logic variables by two-level optic signals not only permits to increase functional possibilities (up to universality), noiseproofnes, stability and decrease requirements regarding alignment and optical system, but also simplify control circuits and adjustment circuits on required functional performed, operation, and keep untouched the whole methodological basis of such universal elements construction irrespective of word length of a code and type of logic. It is shown, that it is possible to create more sophisticated problem-oriented processors, in which the specific time-pulse coded operands are used and to use the elements of only two-valued logic, which will realize functions of different logics, continuous etc. The two-stage structure is used for 2D-arrays processing: at the first stage – elementwise processing; at the second stage – overall processing. At the same time in works (Krasilenko et al., 1995, a; Krasilenko et.al , 1995, c) little attention is paid to such non-traditional basic components of TPCA as width-pulse, phase-pulse, photoconverters, photocurrents comparators. Considerable results, to our mind, for creation of ANN are the development of «equivalence» models and a proper «equivalence» paradigm (Krasilenko & Nikolskyy et.al., 2000, a; Krasilenko & Nikolskyy et.al., 2001, d). Computer simulation results of «equivalence» neural networks models (ENNM) have showed their efficiency and substantial advantages: increase of capacity to (2.5 – 4.0)N; where N is neurons amount, the possibility of spatially invariant recognition of very correlated 2D- and 1D-patterns (Krasilenko et.al., 2008, a; Krasilenko et.al., 2009, a; Krasilenko, 2001, e; Krasilenko et.al., 2002,b). Considerable foundation for development of the proper hardware tools and design of the newest macroelement base was expansion of scalar neurobiologic (NBL) and creation of mathematics of matrix neurobiologic with its base operations of the normalized equivalences (nonequivalence) of two vectors, «equivalence» of spatial functions of 2D-patterns, operations of autoequivalence of nonlinear transformations (Krasilenko et.al., 2009, a; Krasilenko, 2001, e; Krasilenko et.al., 2002,b) and whole family of new «equivalence» operations on the basis of use summarizing operations of continuous fuzzy and neuro-fuzzy logic: fuzzy negation, t-norm and s-norm (Krasilenko et al., 2002, a).

There are tens of different physical models of neurons (Bardachenko et.al., 2004; Krasilenko et.al, 2002, d). But majority of them realized by simplified old mathematic models. Models which have equivalency paradigm properties are described in works (Krasilenko et al., 2002, a; Krasilenko et.al., 2005, a; Krasilenko et.al., 2002, e). It is possible to design such neuron macroelement base on the basis of optical and optoelectronic technologies. The last allows to work out the problems of coupling, density et al. But such optoelectronic models for the equivalence paradigm, which are described in works (Krasilenko et.al., 2005, a; Krasilenko et.al., 2002, e; Krasilenko et.al.,2009, b) have some disadvantages. Realization of normalized equivalence or nonequivalence are considered very little, except paper (Krasilenko et. al., 2009, c). But synthesis and design of hardware representations of normalized equivalence or nonequivalence of two vectors (or even matrices) and their modifications (Krasilenko et al., 2002, a) is the most actual task. In paper (Krasilenko et.al., 2009,c) an approach to realize complement dual neuron elements - neuron equivalentor/nonequivalentor was offered. They are one of variants of more general neuron model. We used conception of pulse-time encoding, as in works (Krasilenko et.al., 2004, a; Krasilenko et.al, 2004, b) . Advantages of such biologically motivated conception are pulse-time (PWM or PPM) principle of signals and variables and operands encoding. Signals at the output of such neurons can be both

digital and analog or hybrid, and with two complement outputs. Then they realize principle of dualism that gives a number of advantages. Therefore, the purpose of this work is subsequent research and perfection of such complement time-pulse coded optoelectronic neural elements, which are named by us as the equivalentor-nonequivalentor neuron. This conceptual approach is used for two-valued, multivalued, neural and neuro-fuzzy continuous logics. Our second position consists in the following: the micromodel of neuron that is the model of heteroassociative memory (HAM) can realize any operation of neurobiologic as well as operations of discrete multivalued logic. For every input combination (situation, state) of vector of Boolean variables there are an output variable. Such model can operate in learning mode (tuning to necessary operations of memorizing of input and proper output variables) and in direct mode which consists of two phases: phase of recognition of input state and phase of forming of output signal. The traditional models of neurons that described in work (Rudenko & Bodjanskyy, 2005) have an input vector and a vector of weighing coefficients as a rule. In our view, the model of neuron must have not only one vector of weighing coefficients but a few. Set of such vectors which are memorized by a neuron will allow comparing of their closeness (remoteness), that is equivalence (nonequivalence), for recognition of a situation at inputs.

2. Motivation and short theoretical ground

2.1 Basic neurological operations of normalized equivalence

For solution of recognition problems a number of mathematics theories and methods is involved; the development of these theories and methods is connected with the advent of expert and intelligence systems: theory of fuzzy sets and theory of possibilities (Zadeh, 1965), theory of neural networks (Freeman James, 1992), and other mathematics methods (Madani, 1998). More purposefully the apparatus of algebraic and fuzzy sets of continuous logic (CL); its derivatives and generalizations, including hybrid, fuzzy predicate logic, neural logic etc. (Krasilenko et al., 1995, a; Levin , 1990, a; Shimbirev, 1990, a; Zhiging Wen, 1996) have become to be applied. Among non-parallel single-stage algorithms of multialternative recognition, an important role is played by numerous versions of algorithms, based on distances calculations (Evclidus, Mahalonobise, Hamming etc) (Shirman, 1996). However, widely spread method, used in static recognition, cluster analysis and other spheres, namely the method of classification by minimal space, has a drawback, due to non-sufficient fast action of necessary space between images calculation, vectors of large dimensions represent these images. Besides, quality of recognition, in particular, the number of stored and correctly recognized references in neuroassociative memory, depends greatly on chosen matrix, type, and space. In neural networks models and recognition algorithms in hidden layers, minimal spaces (while teaching) (Leondes, 1998; Freeman James, 1992) and criteria of maximum convergency are used as intermediate criteria, in some new equivalence models for recognition of strongly corrected images (Krasilenko et al. , 2001, a; Krasilenko et al., 1997,a). The interest to these new directions, neurofuzzy models, logic-algebraic apparatus, common neurobionic principles can be explained by the possibility to understand with their help the principles of human brain functioning. As neurophysiological studies show, frequency-dynamic model of neuron (FDMN), would be the most adequate (nowadays), and neurobiologic (NBL) as the most generalized (as compared with other known logics, such as hybrid, continuous, threshold etc.) could be used to describe the functioning of FDMN (Krasilenko et al., 1995, a;

Krasilenko et.al, 1995, c; Antamonov, 1974; Posin, 1970). Realizations of such FDMN are already known (Krasilenko et.al , 1995, c; Posin, 1970; Levshin, 1987) but they are rarely used, that is connected with their electronic realizations. Only new optic and optoelectronics technologies and their corresponding realization of neuromodules (arrays) with a great number of FDMN and simplified parallel one-cycle inputs-outputs, efficient realizations of interconnections by means of holograms or other optic methods are the most promising direction, permitting to decrease considerably the size and weight parameters, at the same time increasing the dimensions of arrays, performance and speed of data processing (Krasilenko et al., 1995, a; Krasilenko et al. , 2001, a). Basic operation of NBL, in authors opinion (Krasilenko et.al., 2000,b) or the set of operations may be not one, even functionally complete operation but also optimal, basic set of operations, which is necessary for most efficient algorithmic (and sequential in time and parallel simultaneously in space) execution of needed transformations over information signals. We realize that on this way it is quite impossible immediately to find out really final decision for all cases of infinite, complex and dynamic existence of nervous system of living beings. But consideration of such neurobiological models and their basic fundamental operations even for scalar NBL is of gnoseological aspect, it permits still at the stages of conceptual approaches and structural-functional and mathematical-model design rely on vitality and a ability to compete of the suggested solutions. In many neural models (with the exception (Krasilenko et al., 1997, a)) used for optical realization of different associative devices and neural nets, only carrier sets ${}^2C_b = \{-1;1\}^N$ and ${}^2C_u = \{0,1\}^N$ are used in bipolar (b) and unipolar (u) coding respectively. Models, proposed in (Krasilenko et al., 1997,a; Krasilenko et.al., 1996; Krasilenko et.al., 1997,b) and called equivalental, are more general and good for representation of bipolar and unipolar signals, including multilevel signals. The connections, especially braking, are described more natural there. In such models, the basic operation is a standard equivalency of vectors. The models are suitable for different methods of weighing. Considering their prospects, in this work we will show how to build associative (auto-associative and hetero-associative) memory of correlated 2-D images, including multilevel (grey scale) images, based on matrix-tensor models. Functioning of most adequate for present day, frequency-dynamic models of neurons is described by means of mathematic apparatus of continuous logic (CL), hybrid logic, neural-fuzzy logic and other logics, but in the long run, by means of more generalized logic – neurobiologic (NBL) (Shimbirev, 1990, a; Krasilenko et al. , 2001, a; Antamonov, 1974), which is the generalization of all known logics. It is impossible to find partial universal solution for all cases of such complex, versatile, infinite and dynamic existence of nervous system of living organisms. But gnoseological study of all known modules and taking into account the results of neurophysiological research, providing neuroelements with adequate properties and principles of information processing, still at the stages of conceptual approaches and structural functional synthesis allows to hope that the suggested technical solutions will be successfully realized and competitive. Functional and system requirements to neuromodules are considered in a paper (Freeman James, 1992) taking into account the list of neurons properties, some of their optoelectronic realizations, performing one of the basic operations of limited difference (LD) (a. $\dot{-}$ b) have been suggested. The connections among the limited difference (LD) and the basic operations are shown in works (Zadeh, 1965; Freeman James, 1992; Shimbirev, 1990, a; Krasilenko et al., 1997,a): max(a,b), min(a,b),

complement, functionally complete system of functions CL{$\wedge$, $\vee$, –}; operations of limited sum ($\dot{\cup}$) and limited product ($\dot{\times}$) of neuro-fuzzy logic (Shimbirev, 1990, a), operations of equivalence ($\overset{\vee}{\sim}$), ($\overset{+}{\sim}$), and non-equivalence ($\overset{\vee}{\not\sim}$), ($\overset{+}{\not\sim}$) of NBL (Krasilenko et al. , 2001, a; Antamonov, 1974) from the whole set of such operations being generalizations of XNOR and XOR of two-valued logic, permitting logically compare continuous (analog) and multilevel normalized unipolar and bipolar signals including scalar, vector and matrix. In the same works (Krasilenko et al. , 2001,a; Antamonov, 1974), the properties of these operations of equivalence (non-equivalence) are shown, that is why we don't concentrate our attention on this point, but we will use them, in case of necessity. Taking into consideration the above-described approach, consisting in universality, let us recollect some known facts regarding the number of functions. The number of Boolean functions of n variables in algebra of two-valued logic (ATL), which is also Boolean algebra, equals 2^{2^n}. In this ATL there are $N_2 = 2^n$ atoms, which are minterms. Functions of n variables k–valued logic (k>2) are reflections $A^n \to A$, where A={0, 1, ... k-1}, and the number of functions equals $N_k = k^{k^n}$. Algebra, formed by set $^{\wedge}C_u = [0,1]$ or $^{\wedge}C_b = [-1,1]$ is called CL algebra (ACL), and the number of CL functions, as reflections $C_u^n \to C_u$ depending on the CL algebra can be infinite or finite (the set of reflections is always infinite). CL functions are called only those functions of the set $N_{\wedge}$, which are realized by formulas. The number $N_{\wedge}$ of CL functions in the most developed CL algebra – quasi-Boolean Cleenee algebra ($\Delta = (C_u, \wedge, \vee, -)$), in which any function on any set of arguments takes the value of one of the arguments or its negation, is finite. In this case the number $N_{\wedge}(n)$ of functions of n arguments increases with increase of n very rapidly (Shimbirev, 1990, a): $Ч_{\wedge}(0) = 2$; $N_{\wedge}(1) = 6$; $Ч_{\wedge}(2) = 84$; $N_{\wedge}(3) = 43918$. It should be noted that among fuzzy logics, considered in (Shimbirev, 1990, a) and associated with three variations of fuzzy algebra, only one of them coincides with Cleenee algebra, and the notion of fuzzy functions coincides with the notion of CL-function. That is why the sign of equality not always can be put between terms “continuous” and “fuzzy logic”. Thus, our conception consists in creations of time-pulse coding elementary formal neurons, able, by means of their adjustment, (teaching, but not teaching the whole neural networks) to perform any required reflections $C_u^n \to C$ let even with a certain error. This reflection, in many cases, can be created by means of simple memorizing while teaching and often due to limited taught samples be only approximate, but with sufficient criterial evaluation. For the first time in the work (Krasilenko et.al., 1995, e), for constructing of models of neuronal associative memory (NAM) base binary operations of NBL “equivalence” $(\sim)$ and “non-equivalence” $(\not\sim)$ were used of such types:

$$a \overset{\vee}{\sim} b = \min\left\{\max\left(a, \overline{b}\right), \max\left(\overline{a}, b\right)\right\} = \left(a \vee \overline{b}\right) \wedge \left(\overline{a} \vee b\right); \tag{1}$$

$$a \overset{\vee}{\not\sim} b = \max\left\{\min\left(a, \overline{b}\right), \min\left(\overline{a}, b\right)\right\} = \left(a \wedge \overline{b}\right) \vee \left(\overline{a} \wedge b\right); \tag{2}$$

$$a \overset{+}{\sim} b = 1 - |a - b|; \tag{3}$$

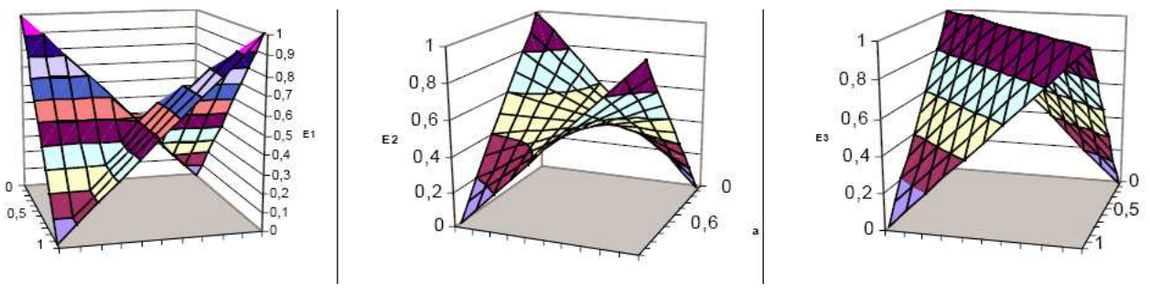
$$a \overset{+}{\not\sim} b = |a - b|, \text{ where } a, b \in C_u = [0,1],\ \overline{a} = 1 - a, \overline{b} = 1 - b. \tag{4}$$

In works (Krasilenko et al., 1997, a; Krasilenko et.al., 1997,b) new equivalental operations of NBL were introduced:

$$a \dot{\sim} b = a \cdot b + \overline{a} \cdot \overline{b} \ ; \tag{5}$$

$$a \dot{\not\sim} b = a \cdot \overline{b} + \overline{a} \cdot b \ , \tag{6}$$

with are more convenient in use, properties of there operations were determined, their connection with function of scalar with metric distances, the connection was demonstrated between "equivalental algebra" (EA) and other algebra's of continuous and multivalued logics. The variants of these equivalence operations on a carrier set $\hat{C}_u = [0,1]$ are shown on fig. 1 (a, b, c) respectively for: $eq^1 = a \overset{\vee}{\sim} b = \max\left\{\min(a,b), \min(\overline{a},\overline{b})\right\}$; $eq^2 = a \dot{\sim} b = a \cdot b + \overline{a} \cdot \overline{b}$; $eq^3 = a \overset{\pm}{\sim} b = 1 - |a - b|$.



$eq^1 = a \overset{\vee}{\sim} b$ $eq^2 = a \dot{\sim} b$ $eq^3 = a \overset{\pm}{\sim} b$

Fig. 1. Operations of equivalence

Their negations are first, second and third nonequivalence respectively. In general case for scalar variables $a, b \in \hat{C} = [A, B]$– continuous line segment, signals themselves and their functions and segment $\hat{C}$ can be brought to segments $[-D, D]$ (or [-1,1]) in bipolar coding and $[0, D]$ (or [0,1]) in unipolar coding. Further, a carrier set $\hat{C} = [0,1]$ and its variables will be considered. Besides, for easier transformations we can limit ourselves at first to operation of equivalence (nonequivalence) of the second type, namely ($\dot{\sim}$) and ($\dot{\not\sim}$) respectively. The terms of equivalental uni-dimension (1-D) and bi-dimension (2-D) functions were introduced: $E(\xi) = f\left(\vec{a}, \vec{b}_{\xi}\right) = \frac{1}{N}\sum_{i=1}^{N}\left(a_i \sim b_{i-\xi}\right)$, $\tilde{E}(\xi,\eta) = f\left(A, B\right) = A \tilde{*} B = \sum_{n=1}^{N}\sum_{m=1}^{M}\left(a_{n,m} \sim b_{\xi+n,\eta+m}\right)$, terms of systemic equivalental function $\Phi_{\sim}$ and systemic non- equivalental function $\Phi_{\dot{\not\sim}} = \overline{\Phi}_{\sim}$, with the help of which it is possible to study the basis of "equivalental" models (EMs) by analog with equalization function in known models. The connection of functions $\tilde{E}(\xi,\eta)$ with correlation functions was demonstrated (Krasilenko et.al., 1997,b). Normalized equivalence of two matrices $A = \left\{a_{ij}\right\}_{I \times J}$ and $B = \left\{b_{ij}\right\}_{I \times J} \in [0,1]^{I \times J}$ is determined in the following way (Krasilenko et.al., 1995, e; Krasilenko et.al., 1997,b): $A \underset{n}{\sim} B = \sum_{i=1}^{I}\sum_{j=1}^{J}\frac{\left(a_{ij} \sim b_{ij}\right)}{I \cdot J}$,

and correspondingly normalized non-equivalence: $A \underset{n}{\not\sim} B = \sum_{i=1}^{I}\sum_{j=1}^{J} \frac{\left(a_{ij} \not\sim b_{ij}\right)}{I \times J}$. It should be noted, if **1**=$\left[1\right]_{I\times J}$ (matrix of units) then $A \underset{n}{\sim} 1 = a_m$ (mean arithmetic value), and $A \underset{n}{\not\sim} 1 = A \underset{n}{\sim} 0 = 1 - a_m = \overline{a}_m$ (complementary mean arithmetic value). Operations $\left(\underset{n}{\sim}\right)$ and $\left(\underset{n}{\not\sim}\right)$ are measures of similarity (equivalence) and difference (non- equivalence, distance) of matrices, which are connected with. Hamming distance, in particular (Krasilenko et.al., 1997,b). Thus, by components operations $(\sim)$ and $(\not\sim)$ of scalar NBL are generalized on matrix case, and NBL logic becomes matrix NBL, i. e. (MNBL). The peculiarity of above considered measures or criteria on their base is that they are invariative to scale change (range) of input components of vectors, matrix, to the change of signal polarity, to the choice of coding type (unipolar of bipolar) to the change of constant component (simultaneous shift of all components by level) belong to the same range [-D, D], are normalized and interconnected (Krasilenko et al., 1997,a; Krasilenko et al. , 2001, a; Krasilenko et.al., 1997,b). Without loosing of community we can consider carrying set (for scalar case) $C_u = \left[0,1\right]$ and $C_u^N = \left[0,1\right]^N$ (for N-dimension (vector, matrix) case). Normalized equivalence $(\underset{n}{\sim})$ and nonequivalence $(\underset{n}{\not\sim})$ are more general new complementary metrics in matrix space R. In particular, $(\underset{n}{\not\sim})$ is a normalized metric distance $d_1(\mathbf{A},\mathbf{B})/m\times n$, and for A and B$\in \{0,1\}^N$ it turns into normalized distance of Hamming $d_n(\mathbf{A},\mathbf{B})/N$. The variants of operations of equivalence and nonequivalence depend on different types of operations of t-norms and s-norms used in them and integrated operations of crossing and joining up in fuzzy logic. Depending on type, variants of equivalent algebra (EA) (Krasilenko et al., 1997,a), as a new algebro-logical instrument for creation of equivalental theory of NNAM based on matrix NBL. We should note the fact that the usage of above-mentioned operations $(\sim)$ and $(\not\sim)$ allowed to create on their base "equivalence" models of artificial networks (ANN) and corresponding equivalence paradigm and theory, that allowed to describe processes in ANN, explain their dynamics, substantiate architectural realizations and technical solutions, that permitted to recognize even space-invariant and strongly correlated images at considerable increase (up to (2.5-4.0)N! at experiments) of the volume of associative memory (Krasilenko et.al., 2001, f; Krasilenko et.al., 2001, g). The contribution to the development of neuromodules is the enlargement of scalar NBL (generalized operations of equivalence) and mathematical models of NN on vector-matrix and matrix-tensor cases, and introduction of spatial normalized equivalence functions of two 2D-images, operations of "auto-equivalency" and "non-equivalency" (Krasilenko et al. , 2001, a; Krasilenko et.al., 2001, f; Krasilenko et.al., 2001, g; Krasilenko et.al., 2002, f).

2.2 Fuzzy set theory and fundamental operation of fuzzy logic

In common case in order to determine the fuzzy set the refection of universal set of objects $\hat{}C$ in the section [0, 1] is used: $\mu_A(x) : \hat{}C \to \left[0,1\right]$, determining for each $x \in \hat{}C$ its degree of belonging to fuzzy set A. Thus, the fuzzy set
can be determined as the set of pairs $\left(x, \mu_A(x)\right)$, where $x \in \hat{}C$, $\mu_A(x)$ - belonging function. Thus fuzzy subsets can be considered as an extension of traditional crisp set, of in other

words, the classical crisp set is a special case of a fuzzy set (Zhiging Wen, 1996). Assuming there are two fuzzy subsets $A=\{x,\mu_A(x)\}$ and $B=\{x,\mu_B(x)\}$, $x\in\hat{}C$ some common operations are defined as follows (Klir & Folger , 1998; Schmucker, 1989):

1. Complement with $\mu_{\bar{A}}(x)=1-\mu_A(x)$,
2. Union of fuzzy subsets A and B $\mu_{A\cup B}(x)=\max(\mu_A(x),\mu_B(x))\in\hat{}C=[0,1]$,
3. Intersection $\mu_{A\cap B}(x)=\min(\mu_A(x),\mu_B(x))$,
4. Equalization: $A=B$, $\mu_A(x)=\mu_B(x)$,
5. Symmetric difference $\mu_{A\Delta B}(x)=|\mu_A(x)-\mu_B(x)|\quad\forall x\in\hat{}C$.

2.3 The family of equivalence (non- equivalence) operations

Let us introduce new generalized operation of the its type of equivalence (non-equivalence) operation, written in the following form:

$$^{t,s}E'(a,b)=(atb)s(a_n tb_n)=(atb)s(\bar{a}t\bar{b}), \tag{7}$$

and as *t*-norm and *s*-norm any of their variants can be used (Kuzmin et.al., 1992; Krasilenko et al., 2002, a). The analysis of the whole spectrum of all possible $^{t,s}E'(a,b)$ shows, that the following operations are the most interesting in case of certain *t*- and *s*-norms:

$^{\bullet,+}E'(a,b)=a\cdot b+\bar{a}\cdot\bar{b}=a\dot{\sim}b$, (known operation see formula (5))

$^{\bullet,\dot{+}}E'(a,b)=a\cdot b+\bar{a}\cdot\bar{b}-a\cdot b\cdot\bar{a}\cdot\bar{b}=(a\dot{\sim}b)-(a\cdot b)\cdot(\bar{a}\cdot\bar{b})$, (new operation)

$^{\bullet,\vee}E'(a,b)=a\cdot b\vee\bar{a}\cdot\bar{b}=\max(a\cdot b,\bar{a}\cdot\bar{b})$, (new operation)

$^{\wedge,+}E'(a,b)=\min(a,b)+\min(\bar{a},\bar{b})=a\overset{+}{\sim}b$, (see formula (3) known operation)

$^{\wedge,\vee}E'(a,b)=a\tilde{\sim}b=(a\wedge b)\vee(\bar{a}\wedge\bar{b})$, (see formula (1) known operation)

$$^{\wedge,\dot{+}}E'(a,b)=(a\wedge b)\dot{+}(\bar{a}\wedge\bar{b})=\min(a,b)+\min(\bar{a},\bar{b})-\min(a,b)\cdot\min(\bar{a},\bar{b})=$$
$$=\left(a\overset{+}{\sim}b\right)-\min(a,b)\cdot\min(\bar{a},\bar{b});$$

It should be noted, that for the case of taking the complement by one the variables, these operations will have the following form:

$^{\bullet,+}E'(a,\bar{b})=a\cdot\bar{b}+\bar{a}\cdot b=a\not\sim b=^{\bullet,+}E'(\bar{a},b)$, (see formula (6))

$^{\bullet,\dot{+}}E'(a,\bar{b})=a\cdot\bar{b}+\bar{a}\cdot b-(a\cdot\bar{b})\cdot(\bar{a}\cdot b)=(a\not\sim b)-(a\cdot b)\cdot(\bar{a}\cdot\bar{b})$,

$^{\bullet,\vee}E'(a,\bar{b})=a\cdot\bar{b}\vee\bar{a}\cdot b=\max(a\cdot\bar{b},\bar{a}\cdot b)$, $^{\wedge,+}E'(a,\bar{b})=(a\wedge\bar{b})+(\bar{a}\wedge b)$,

$^{\wedge,\vee}E'(a,\bar{b})=(a\wedge\bar{b})\vee(\bar{a}\wedge b)=a\not\tilde{\sim}b$, (see formula (2) known operation)

$$^{\wedge,\dot{+}}E'(a,\bar{b})=(a\wedge\bar{b})+(\bar{a}\wedge b)-\min(a,\bar{b})\cdot\min(\bar{a},b)=^{\wedge,+}E'(a,\bar{b})-\min(a,\bar{b})\cdot\min(\bar{a},b)$$

Introducing new generalized operation of equivalence of II type (non-equivalence) we write in the following form: ${}^{s,t}E''(a,b)=(asb)t(\bar{a}s\bar{b})$ or taking into consideration the law of De Morgan so:

$${}^{s,t}E''(a,b)=\left((asb)_n\, s(\bar{a}s\bar{b})_n\right)_n=\left((\bar{a}t\bar{b})s(atb)\right)_n=\left({}^{t,s}E'(a,b)\right)_n=\overline{{}^{t,s}E'(a,b)} \tag{8}$$

we will obtain the connection between operations of I and II type. That is why, the II type of operations can be called the operation "non-equivalence" of the I type and designate it as: ${}^{t,s}NE'(a,b)={}^{s,t}E''(a,b)=\left({}^{t,s}E'(a,b)\right)_n$.Thus, formula (7) and (8) which is analogous to formula (7) determine new generalized operations of comparison (determination of equivalence or non-equivalence).

2.4 The short browse mathematical equivalence models of neural networks

The weighing coefficients of synapse connections matrix of equivalence models are determined through the normalized equivalence of *f*, namely (Krasilenko et al. , 2001, a; Krasilenko et al., 1997,a):

$$T_{ij}^{0}=\frac{1}{M}\sum_{m=1}^{M}\left(S_m^i\sim S_m^j\right)=f\left(\bar{S}^i,\bar{S}^j\right)$$

where S_m^i, S_m^j are proper values of *i*-th and *j*-th neuron of *m*-th standard learning pattern, $\vec{S}^i$ and $\vec{S}^j$ are vectors from all *i*-th or *j*-th components of all set from **M** vectors, whether $T_{ij}^{\beta}=\frac{1}{M}\sum_{M=1}^{M}\left(|\beta_m|\sim S_m^i\sim S_m^j\right)$ where β_m is vectors equivalence coefficient, and also it is the normalized equivalence of f vectors, that $\beta_m=f\left(\vec{X},\vec{S}^m\right)=\frac{1}{N}\sum_{i=1}^{N}(S_i^m\sim X_i^{in})$. Formulas for the neurons initial signals calculation in the equivalence models also taken to determination of the normalized equivalence of *f*, namely: $X_j^{out}(t+1)=\varphi_j\left[f(\vec{T}_j^{0/\beta},\vec{X}_{(t)}^{in})\right]$ where $\vec{T}_j^{0/\beta}$ is a *j*-th vector-column from a matrix $\mathbf{T}^{0/\beta}$, and $\vec{X}^{in}$ is an input vector. For initial vector X_j^{out} component calculation it is possible to take advantage of formula from works (Krasilenko et al., 1997,a; Krasilenko et.al., 1996; Krasilenko et.al., 1997,b) which is taken to finding of the normalized equivalence: $X_j^{out}=\varphi_j[f(\vec{R}^j\sim\vec{\beta})]$ where $\vec{R}^j$ is a vector from the *j*-th components of all **M** learning vectors $\vec{S}_{m\in 1\div M}$, and as a vector $\vec{\beta}$ with **M** dimension it is possible to use $\vec{\beta}$, $\vec{\beta}^{\alpha}$, and $\vec{\beta}^{\text{nonlinear}}$, thus $f\left(\vec{R}^j,\vec{\beta}\right)=\frac{1}{M}\sum_{m=1}^{M}(\vec{R}^j\sim\vec{\beta})$.

In addition, it is possible to show many other formulas, which are used in the equivalence models paradigm and based on calculations of the normalized equivalence or nonequivalence of vectors or matrices (Krasilenko et.al., 2008, a; Krasilenko et.al., 2009, a; Krasilenko et.al., 2002, f). The analysis of these formulas shows that in most cases one of vectors from which calculated *f*, there is a component with binary values, that $x_i\in\{0,1\}$, but not $[0,1]$. It considerably simplifies realization of such *f* operations, as all of equivalence types, namely ($\tilde{=}$), ($\tilde{\pm}$), ($\tilde{\sim}$), are taken to one. Mathematical formulas for calculation of f and $\bar{f}$, or

$\tilde{e}(\vec{x},\vec{w})$ and $\widetilde{ne}(\vec{x},\vec{w})$ are showed in paper (Krasilenko et.al., 2009, c) . But in most general case optoelectronic complementally dual neuron (equivalentor/nonequivalentor), including the normalized components of vectors $\vec{x}$ and $\vec{w}$, has analog homopolar encoded components, $x_i \in [0,1]$ and $w_i \in [0,1]$. We will mark also, that in work (Krasilenko et.al.,2008, b) it is showed that set of operations, normalized equivalence and nonequivalence is the functional complete system of continuous logic functions. Therefore f realizing from vector information is very actual. As follows from works, for example from paper (Krasilenko et.al., 2002, f), for the calculation of mean value (expected value) component of vector, it is necessary to calculate a normalized equivalence f from vector $\vec{A}$ and vector $\vec{1}$ with single components: $a_m = f\left[\vec{A},\vec{1}\right]$. Also $\overline{a}_m = f\left[\vec{A},\vec{0}\right] = \overline{f}\left[\vec{A},\vec{1}\right]$,where $\overline{f}$ –normalized nonequivalence. We will designate f various types of erations ($\tilde{\sim}$), ($\overset{+}{\sim}$), ($\overset{\vee}{\sim}$) or their generalizations (Krasilenko et al., 2002, a); ${}^{t,s}E'(a,b) = (atb)s(\overline{a}t\overline{b})$ by character ($\sim$) for simplicity.

3. Designing and modelling of multifunctional units of neural (continuous) logic

3.1 Structural-functional design of universal elements for neural (continuous) logic

Now let us discuss continuous logic (CL), modifying the approach, suggested in papers (Krasilenko et al., 1995, a; Shimbirev, 1990, a), but to make the understanding of the problem easier, we will consider here the scalar case for n (an example for two) arguments and for the realization of a random continuous-logic function, where their complements participate. We assume x_1, x_2 to be the arguments and their complements $\overline{x_1} = 1 - x_1$, $\overline{x_2} = 1 - x_2$, taking into account their dependence. The number of cube partitioning $[0,1]^n$ into areas or number of situations of mutual location of arguments in this case is $H = 2^n n!$ areas (if n=2 the number of the areas is 8), but not $(2n)!$ that is seen from the Fig. 2a, where the square $[0,1]^2$ partitioning is shown. In Fig. 2a the number of each area coincides with the number of situation indicated above, for which the relations between arguments in the given situation and values of the function $f(x_1,x_2) = (\overline{x_1} \wedge x_2) \vee (x_1 \wedge \overline{x_2})$ for each area are shown in the table, presented in Fig. 2b. At all points in the same area the function value, not in case of const "0" and "1", equals one of either the arguments or the complements. Fig. 2c shows values of $\tilde{EQ}$ function (notation from paper (Krasilenko et al., 1997, a)), which is calculated in the following way: $\tilde{EQ}(x_1,x_2) = x_1 \wedge x_2 \vee (\overline{x_1} \wedge \overline{x_2})$. Fig. 2d shows relations between x_2 and $\overline{x_1}$ for area I (the shaded area) and area II. Fig. 2e shows pairs, setting order relations between pairs, the connections in the pairs are shown by dotted and solid lines. Each situation of known subcode is definitely determined by setting of order relations between pairs and the number of such pairs equals 4 for n=2 (see Fig. 2e), in general case $n + 2C_n^2 = n^2$. Table (Fig. 2b) shows the states of comparators $K_1 \div K_4$ signals, comparing by pair the order relations in Fig. 2e. The usage of decoder, converting 4-digit binary codes at the output of comparators in 8-digit one-positional code (this is the difference between our approach from the approach, known from paper (Shimbirev, 1990, a), and in general case n^2-digit code of comparators into ($H = 2^n 2!$)-digit one-positional code, allows by means of formation of H adjusting signals y_h from the set of 2n arranged variables $\{x_1, \ldots x_n, \overline{x_1}, \ldots \overline{x_n}\}$ to select for each situation one of 2n arguments (direct or its complement). In our modified variant, as it is seen from Fig. 2,c,d the value of $\tilde{EQ}$ function ($\tilde{EQ} \in \{x_1, x_2, \overline{x_1}, \overline{x_2}\}$) determines one of the regions {7, 2, 3, 5} in the area I or one of the regions {4, 6, 8, 1} in the

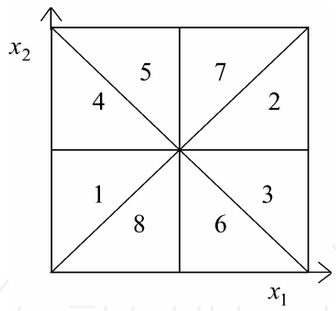


Fig. 2a. The number of each area coincides with the number of situation indicated above, for which the relations between arguments in the given situation and values of the function

Region	Situation	Situation	$f(x_1,x_2)$	Comparators outputs			
				1	2	3	4
1	$0 \le x_1 \le x_2 \le 1/2$	$x_1 \le x_2 \le \overline{x_2} \le \overline{x_1}$	x_2	1	0	1	0
2	$0 \le \overline{x_1} \le \overline{x_2} \le 0.5$	$\overline{x_1} \le \overline{x_2} \le x_2 \le x_1$	$\overline{x_2}$	0	1	0	1
3	$0 \le \overline{x_1} \le x_2 \le 0.5$	$\overline{x_1} \le x_2 \le \overline{x_2} \le x_1$	$\overline{x_2}$	0	1	1	1
4	$0 \le x_1 \le \overline{x_2} \le 0.5$	$x_1 \le \overline{x_2} \le x_2 \le \overline{x_1}$	x_2	1	0	0	0
5	$0 \le \overline{x_2} \le x_1 \le 0.5$	$\overline{x_2} \le x_1 \le \overline{x_1} \le x_2$	$\overline{x_1}$	1	1	0	0
6	$0 \le x_2 \le \overline{x_1} \le 0.5$	$x_2 \le \overline{x_1} \le x_1 \le \overline{x_2}$	x_1	0	0	1	1
7	$0 \le \overline{x_2} \le \overline{x_1} \le 0.5$	$\overline{x_2} \le \overline{x_1} \le x_1 \le x_2$	$\overline{x_1}$	1	1	0	1
8	$0 \le x_2 \le x_1 \le 0.5$	$x_2 \le x_1 \le \overline{x_1} \le \overline{x_2}$	x_1	0	0	1	0

Fig. 2b. Table shows the states of comparators $K_1 \div K_4$ signals, comparing by pair the order relations in Fig. 2e

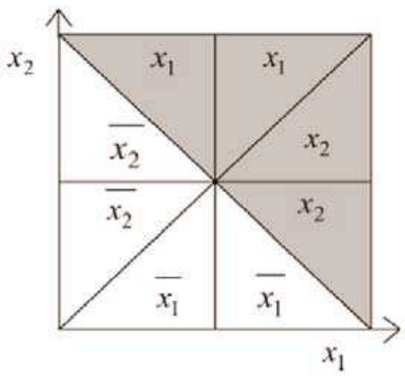


Fig. 2c. Values of $\overset{\vee}{E\tilde{Q}}$ function, which is calculated in the following way:

$\overset{\vee}{E\tilde{Q}}(x_1,x_2) = x_1 \wedge x_2 \vee (\overline{x_1} \wedge \overline{x_2})$

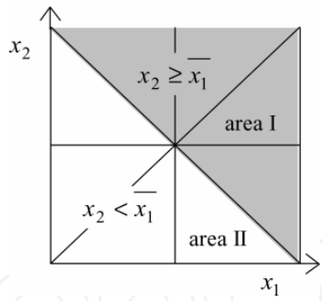


Fig. 2d. Shows relations between x_2 and $\overline{x_1}$ for area I (the shaded area) and area II

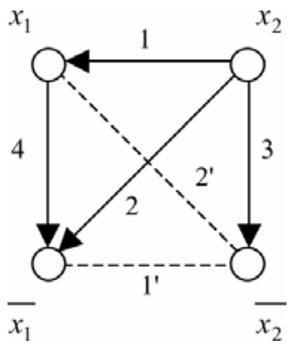


Fig. 2e. Shows pairs, setting order relations between pairs, the connections in the pairs are shown by dotted and solid lines

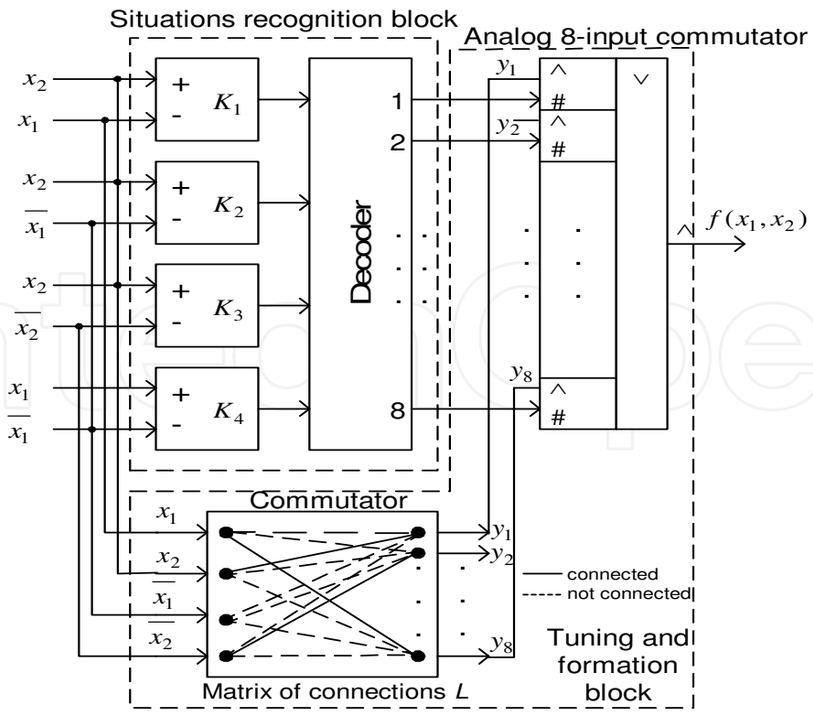


Fig. 3a. The universal continuous-logic neural element with programmable tuning

$\mathbf{L} =$

	y_1	y_2	y_3	y_4	y_5	y_6	y_7	y_8
x_1	0	0	0	0	0	1	0	1
x_2	1	0	0	1	0	0	0	0
$\overline{x_1}$	0	0	0	0	1	0	1	0
$\overline{x_2}$	0	1	1	0	0	0	0	0

Fig. 3b. Tuning matrix for the function $f(x_1, x_2)$ for the example, shown in Table 1

$\mathbf{L}' =$

	y_1	y_2	y_3	y_4	y_5	y_6	y_7	y_8
x_1	0	0	0	0	0	1	0	0
x_2	1	0	0	1	0	0	0	0
$\overline{x_1}$	0	0	0	0	1	0	1	0
$\overline{x_2}$	1	1	1	0	0	0	0	0

Fig. 3c. The tuning matrix *L*' shown on the figure differs from *L* in the first situation the constant $"1" = x_2 + \overline{x_2}$ is at the output, and in the 8-th situation "0" is at the output

area II. The scheme of the universal continuous logic element will have the view, shown in Fig. 3a and adjusting matrix is shown in Fig. 3b. By multiplying inputs vector $\{x_1, x_2, ...x_n, \overline{x_1}, \overline{x_2}, ...\overline{x_n}\}^{tr}$ by this matrix *L*, the adjusting vector $Y = \{y_1, ...y_H\}^{tr}$ is formed. The tuning matrix *L*' shown in Fig. 3c differs from *L* in the first situation the constant $"1" = x_2 + \overline{x_2}$ is at the output, and in the 8-th situation "0" is at the output. Thus, we have synthesized universal continuous-logic element (UCLE), its possible realization for matrix case we construct in the next sections. It should be noted, that the situations recognition block might include elements, which realize only neuro-fuzzy logic operations and can be considered as micro-level hetoro-associative neural network with analog inputs and digital outputs.

3.2 Time-pulse coding (TPC) universal elements of neuro-biologic

Let us return to the problem of presentation and coding of continuous signals. It is seen from Fig. 3a, that signal x_2 must be sent to 3 comparators and to 8 synapse-connections in adjusting commutator, thus it become clear, that coding of optic power arguments within the scheme is not effective. Having chosen both in matrix multivalued logic (MML) universal picture element (UPE) and matrix twovalued logic (MTL) UPE time-pulse coding, the scheme of UCLE can be converted into the form, shown in Fig. 4. It is taken into account that RS-triggers by means of sending pulses from the PPM output to these triggers can act as comparator of time delays, as it has been shown in paper (Krasilenko et al., 1995, a). The analysis of the scheme Fig. 4a shows that since time-pulse signals are formed at the circuit output, then phase-pulse photoconverters with complementary outputs are needed only for input of initial information; as a matter of fact, processor part can operate with already formed at previous step time-pulse coding results (CL functions of arguments t_{out}, $\overline{t_{out}}$) which are again sent at the input of this or the next array of such universal neural elements.

That is why, if we form, as it is seen in the scheme of Fig. 4b, two outputs: $f(x_1, x_2) \Rightarrow t_{out}(t_1, t_2)$ and $\overline{f}(x_1, x_2) \Rightarrow \overline{t_{out}}(t_1, t_2)$ or in general case several functional outputs, then pulse phase modulator (PPM) must have direct and complementary optic outputs.

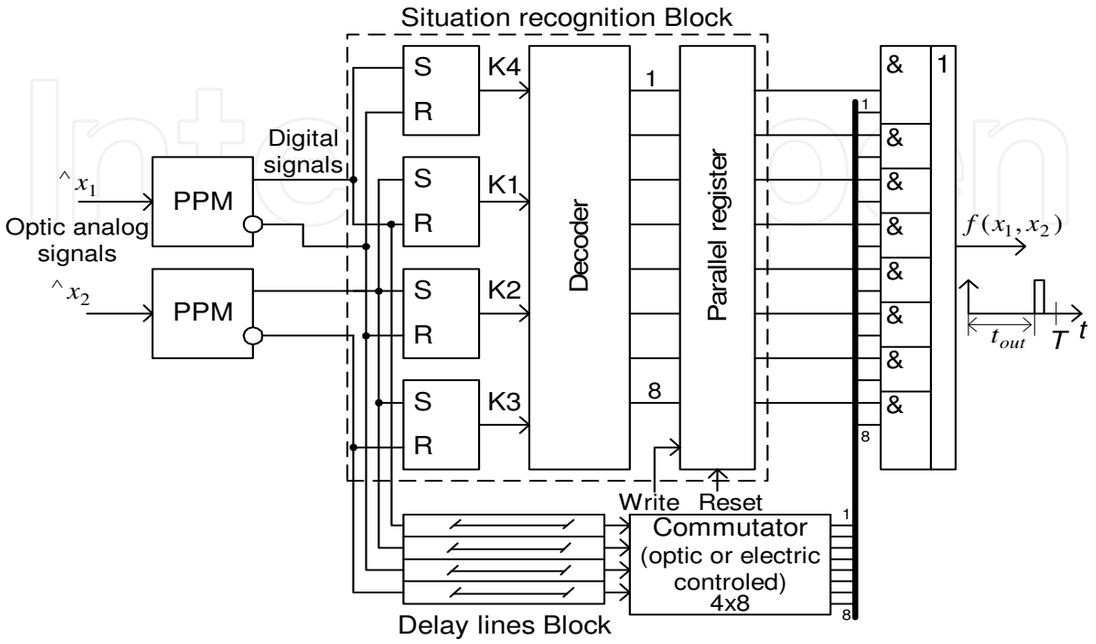


Fig. 4a. The universal continuous-logic neural element

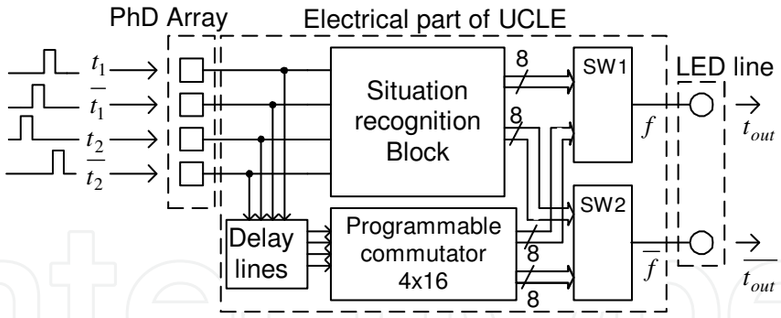


Fig. 4b. Scheme's variant with electronic unit of digital signals delay - two outputs: $f(x_1, x_2) \Rightarrow t_{out}(t_1, t_2)$ and $\overline{f}(x_1, x_2) \Rightarrow \overline{t_{out}}(t_1, t_2)$

In this case, as in variant with electronic unit of digital signals delay (Fig. 4b) as well as in variant of optic delay unit (better for picture organization of matrix logic) universal continuous logic element will be completely digital, operating with two level signals, tuning and information inputs are realized on photosensitive elements, distinguishing only two levels of optic power. It is not difficult to create an array of such digital elements. The electrical digital part of the UCLE can be realized on programmable logic devices (PLD). Simulation results of the scheme Fig. 4a by Altera MAX-PLUS II v.10 software are shown in Fig. 5. The scheme successfully fits into device EPM7032LC44-6 from MAX7000 family. The simulation results are shown for the realization of 16-valued functions (Fig. 2b). The *L*

matrix of connections (Fig. 3d) is used. At the cycle 1 at input pins we have the set of phase-modulated pulses that corresponds to the situation 1 and so at the output pin (Out_f) at the cycle 2 we have a pulse that corresponds to x_2 (see table in Fig. 2b) and so on. For 100 distinguishable time positions and 10ns input pulse width the processing time will be 1μs and can be less if faster PLD is used. Hence, the electronic part of the UCLE does not limit the processing speed in contrast to PPM, which, as it is shown below, is a slower device.
Thus, proceeding from the above-mentioned study of picture type universal elements with programmable tuning of continuous and discrete logics it is necessary to develop arrays of time-pulse, and especially pulse-phase photoconverters if time-pulse coding is used and comparators of analog optic signals if amplitude coding for continuous logic is used.

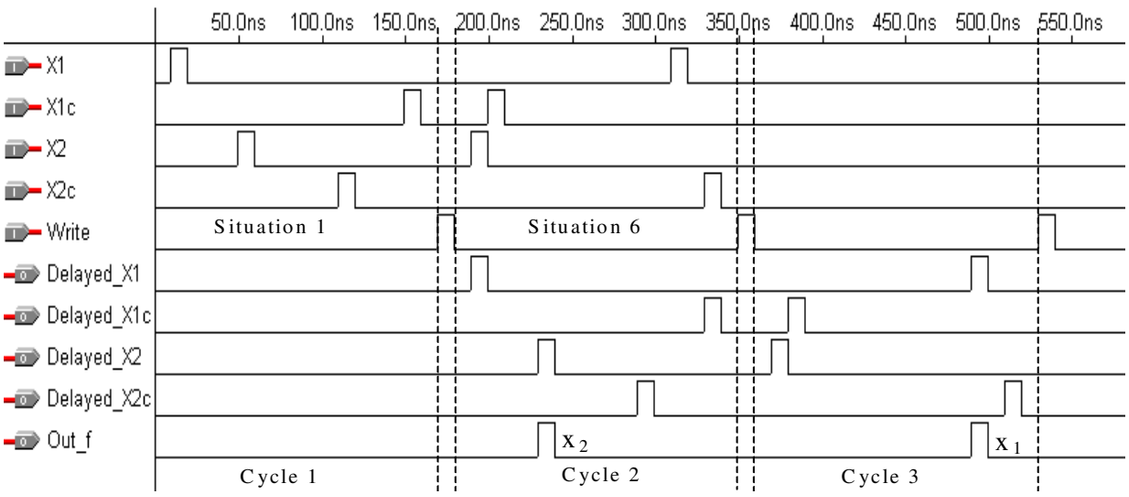


Fig. 5. Simulation results of digital part of UCLE (Fig. 4a)

3.3 Picture continuous logic elements (PCLE)

Fig. 6 shows the structural diagram of picture neural element (PNE) for computation of all basic matrix-continuous-logic (MCL) operations in matrix quasiboolean algebra **C=((A,B),∨, ∧ -)**(Krasilenko et al., 1995, a) for which in any set of MCL arguments matrix continuous logic function (MCLF) **F** takes the value of a subregion of one of the arguments or its supplement. PE of MTL, performing MTL operations over matrix temporal functions $O^i_t(t)$ (in point of fact two-valued 2D-operands) realize MCLF over continuous logic variables (CLV) O^i_t. The time-pulse coding of a grayscale picture is shown in Fig. 7. As it is seen from Fig. 8 at each point of picture output of PNE, MCL can be performed over continuous logic variables (CLV) $O^1_{ijT},\ldots O^{n=2}_{ijT}$, presented by $t^1_{ij},\ldots t^n_{ij}$ durations of time pulse signals, during each interval T one of the following operations of CL : min(a,b), max(a,b), mod(a-b), $\overline{\mathrm{mod}(a-b)}$, complementary $\bar{a}=1-a$, equivalence, etc. (Krasilenko et al., 1995, a; Levin , 1990, a; Krasilenko, 1988,b). The duration of MTL formed at the output, and as a result of PNE, signal $f^{NE}_{ij}(t)=f^{NE}_{ij}\left(O^1_{ij}(t),O^2_{ij}(t)\right)$, is CL function of input binary temporal variables durations. Thus, as it is seen from Fig. 8, almost all basic operations of continuous logic, neuro-fuzzy logic, that are shown in work (Krasilenko et al., 2002, a), can be realized with the help of a time-pulse coding of variables $\mathbf{X}_1,\ldots,\mathbf{X}_n$ and universal picture element (UPE)

of array two-level logic (ATL). But for that PWM PT are needed. It is not needed to form contrast-conversion (complementary operand) image for analog picture optic inputs if PWMs PT have complementary outputs.

Thus, we have shown, that the basic unit of components considered above is width- pulse or phase-pulse matrix (multichannel) photoconverters, and main characteristics of basic macrounits of future advanced systems of 2D-data processing optical computers and neural networks greatly depend on the parameters of above mentioned components, especially, such parameters as linearity, accuracy and transformation rate.

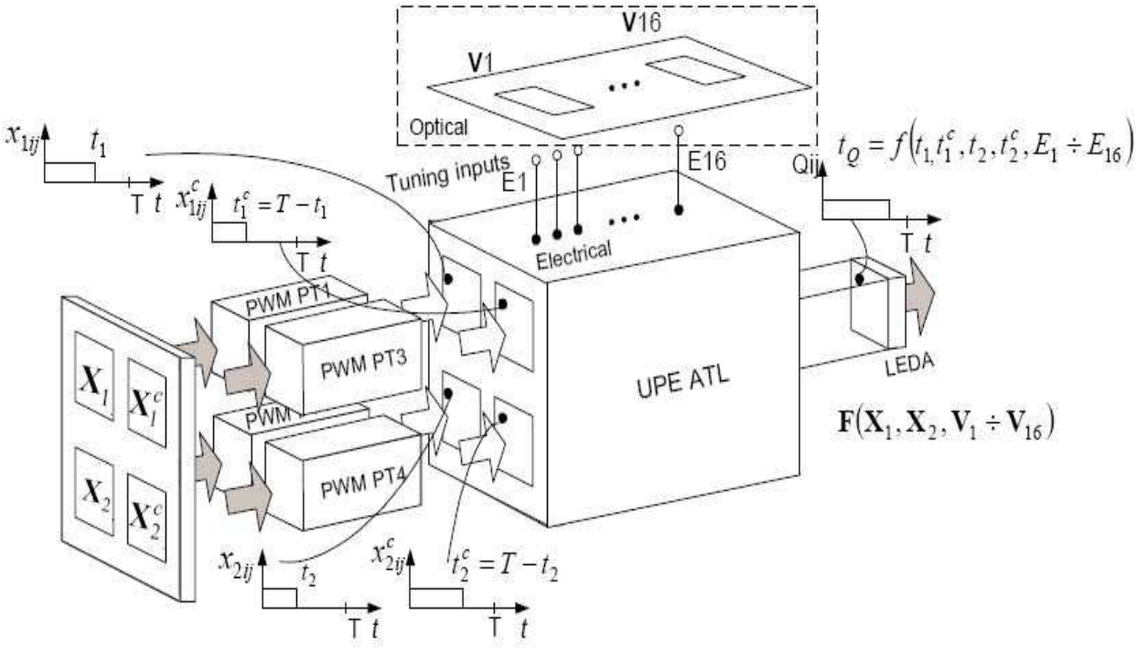
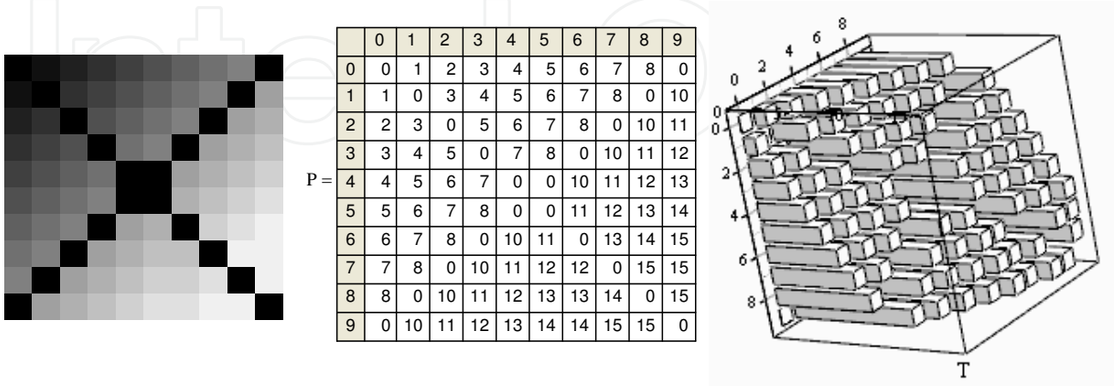


Fig. 6. PNE ANL based on PWM PT with programmable tuning



P =

	0	1	2	3	4	5	6	7	8	9
0	0	1	2	3	4	5	6	7	8	0
1	1	0	3	4	5	6	7	8	0	10
2	2	3	0	5	6	7	8	0	10	11
3	3	4	5	0	7	8	0	10	11	12
4	4	5	6	7	0	0	10	11	12	13
5	5	6	7	8	0	0	11	12	13	14
6	6	7	8	0	10	11	0	13	14	15
7	7	8	0	10	11	12	12	0	15	15
8	8	0	10	11	12	13	13	14	0	15
9	0	10	11	12	13	14	14	15	15	0

a) b) c)

Fig. 7. Time-pulse coding of a grayscale image: a) input grayscale image; b) matrix of light intensities; c) output time-pulse code

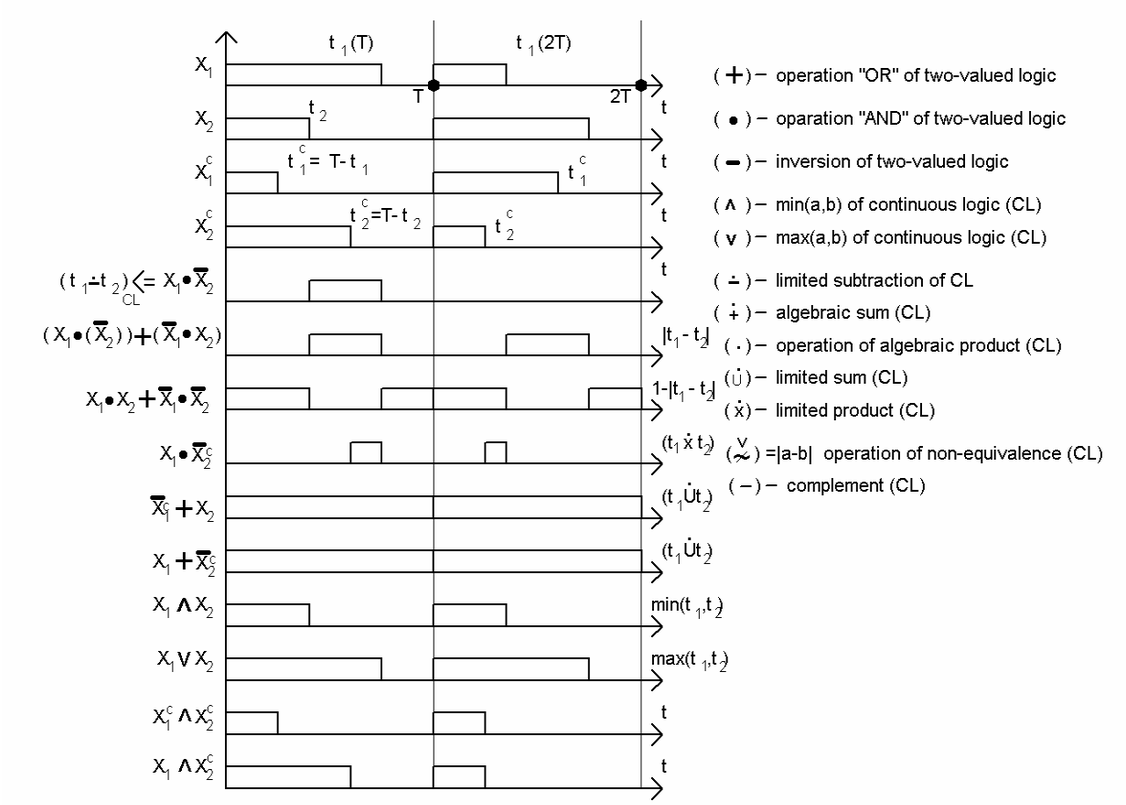


Fig. 8. Time diagrams of CL operation fulfillment by means of time CL variables

3.4 Time-pulse coding photoconverters

3.4.1 Optic signals comparators

The suggested time-pulse coding photoconverters are realized on the basis of optic signals comparators, that is why first we will consider the principle of construction and operation of optic radiation power comparator with potential output. The circuit of suggested comparator with potential output is shown in Fig 9 and consist of two photodiodes, intended for transportation of power of input optic radiation into corresponding value of input current, and of current comparator, realized on two current mirrors, on CMOS-transistors. Power of input optic radiation P1 and P2 are transformed into corresponding input currents I1 and I2 by means of photodiodes VD1, VD2. Further these currents pass to the input of the first current mirror, realized on transistors VT1, VT3 and second current mirror, realized on transistors VT2, VT4. At the output of comparator (Out), the voltage of logic "1" is formed, if current I1>I2 (power P1>P2), and voltage of logic "0", if current I1<I2 (power P1<P2).

The results of this circuit simulation by means of OrCad PSpice software are shown in Fig 10. 1.5μm CMOS-transistors technology (AMIS 1.50) is used, the parameters of transistors models are taken from the website of MOSIS company (www.mosis.org). For transistors, the length L and width W of channel is: for NMOS L=1.6μm, W=4μm; for PMOS L=1.6μm, W=8μm. The model of CMOS-photodiode is used (Swe & Yeo, 2001). The range of input currents is 100nA...100μA. Supply voltage is 3...15V. Time delay of voltage setting at the output of comparator is in inverse proportion to input currents difference. In case of

Δ=10μA time delay is t_d≈40ns, in case of Δ=1μA, t_d≈100ns. Fig. 11 shows the transfer characteristics of comparator for two values of input current I2=20μA and I2=60uA for input current I1 changes from 0 to 100μA. The transfer characteristics of the comparator can be improved if we put a key-inverter (Fig. 12) at the output. In this case, we obtain transfer characteristics that are shown in Fig. 13. At the output we have voltage of logic level "1", if current 11<12 and output voltage of logic level "0" if current I1>I2. The voltage of logic "1" corresponds to supply voltage. The accuracy of comparison is 0.5nA, if input currents are 100nA, and 40nA, if input currents are 10μA, i.e. the relative error is <0.5%. If we put a driver circuit (Ahadian & Fonstad, 1998) and a light-emitting diode or a semiconductor laser at the output, then we obtain the comparator with optic output (Fig. 12).

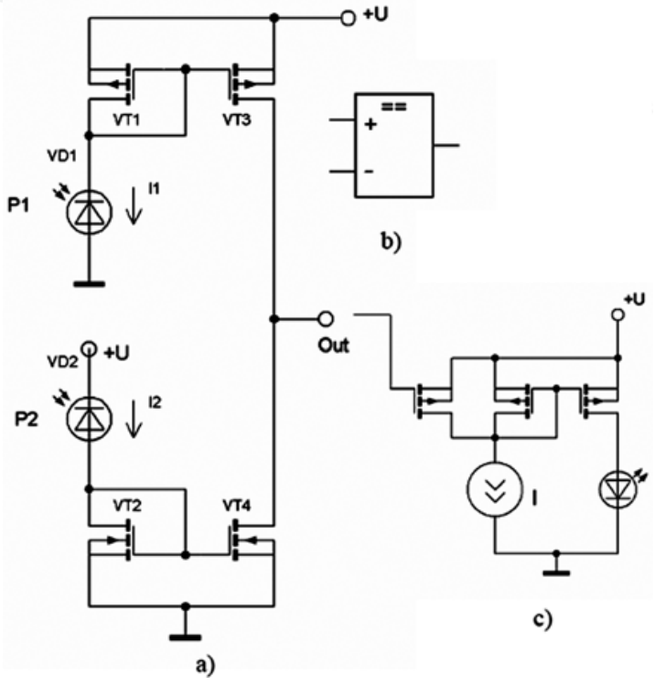


Fig. 9. Comparator of photocurrent with potential output (a), conventional graphical symbol (b), circuit of optical output (c)

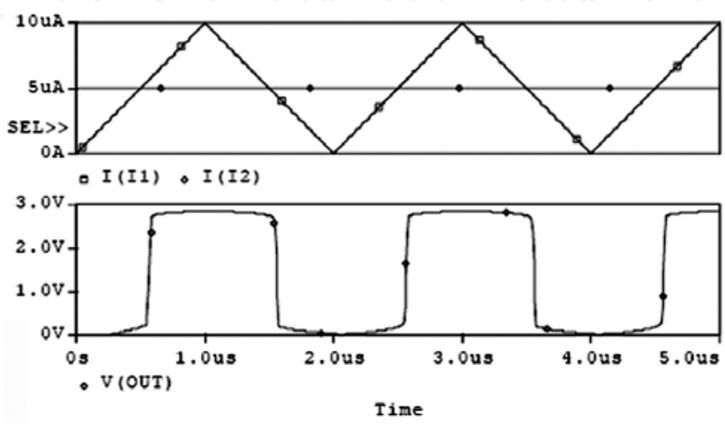


Fig. 10. Time diagram of comparator operation

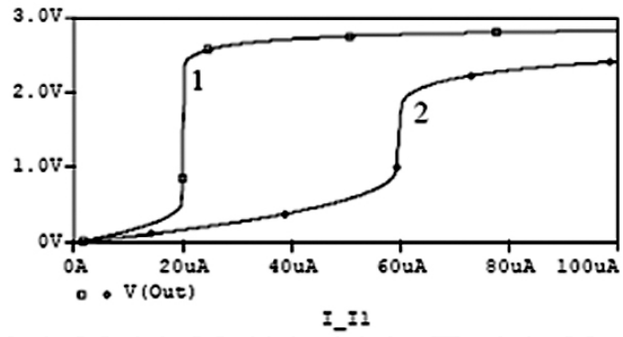


Fig. 11. Transfer characteristic of the comparator: 1 – threshold current I2=20μA; 2 – threshold current I2=60μA

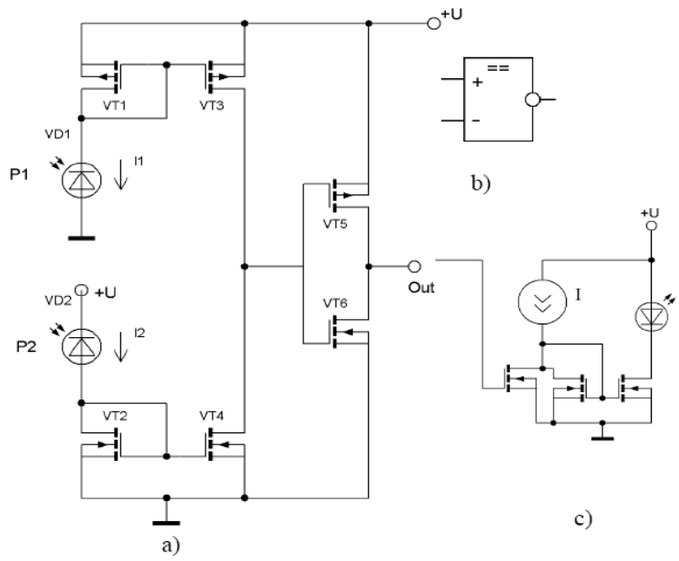


Fig. 12. Circuit of photocurrent comparator with inverter at the output (a), conventional graphical symbol (b), optical output circuit (c)

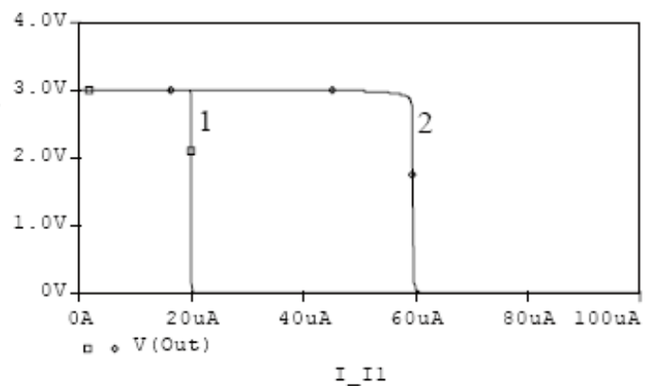


Fig. 13. Transfer characteristic of the comparator: 1 – threshold current I2=20μA; 2 – threshold current I2=60μA

3.4.2 Optoelectronic PWM

Having replaced photodiode VD1 in the circuit, present in Fig 12, by a saw-type current generator, we obtain width-pulse modulator. Voltage pulse duration on its output is directly proportional to the value of the input current I2. The results of simulation of the given circuit for three values of input current I2=(1μA, 4μA, 8μA) are shown in Fig 14. Pulse duration delay of output voltage for value of the input current I2=1μA is 350ns, that leads to rather big relative error at small currents. Fig 15 shows the diagram of relative error of transformation for the range of input current 1.....100μA, and period of transformation is 100μs. In order to decrease the error it is necessary to use transistors that are faster or increase the conversion coefficient. If the transistors of TSMC 0.25μm technology are used the delay of output voltage pulse duration is 180ns at the input current I2=1μA, that reduces the relative error to 18% at small input currents. If we increase the conversion period to 1ms than the relative error can be reduced to 7% at small inputs currents and be less than 1% at input currents more than 5μA. The transition on GaAs technology allows to increase the conversion speed and scale of integration. Power consumed by modulator is 155μW if the value of the input current is 1μA, and 605μW if the value of the input current is 100μA, and supply voltage is 3V. The application of 0.25μm technology transistors allows decreasing the supply voltage to 1.5 V, and hence reducing the consumed power. The average consumed power by one cell is about 0.5mW, and it is about 1mW with LED. So the average consumed power by 1000 of such cell is about 1W that allows to carry out their integration in arrays of 32×32, 64x64 elements and more.

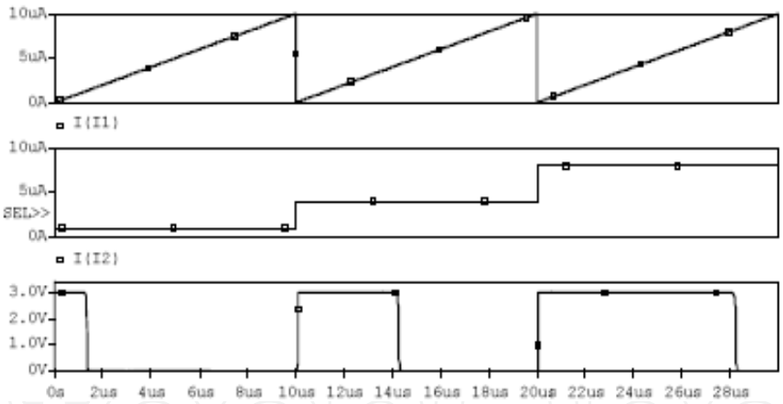


Fig. 14. Time diagrams of PWM operation

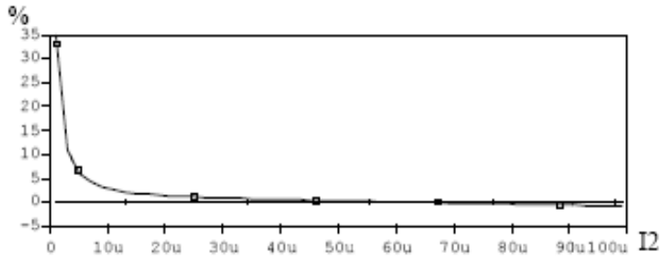


Fig. 15. Relative error of current I2 to output voltage pulse-width conversion for 100μs period

Earlier we have considered PWM with optic inputs based on λ-diodes (Krasilenko et.al., 2003). That modulator provides non-linearity of not more than 0.1% at transformation period of 1ms in the range of input currents 1uA…1mA and satisfactory parameters at frequencies up to 1MHz. But the drawback of the circuit is the realization of λ-diodes on field transistors with controlling p-n junction, that are not used in standard digital CMOS IC technology, and the necessity to use reset current signals with two times more amplitude than the λ- diodes threshold.

3.4.3 PWM with complementary outputs

In order to construct a various devices of continuous, neural, multilevel and other logics it is often needed to have direct and complementary signals. For this purpose we suggest to consider the operation of circuit of width-pulse modulator with complementary time-matched outputs (Fig 16). The sum of durations of voltage pulses at the complementary and direct output equals conversion period *T*. The availability of the complementary output expands functional possibilities of UPE ANL. The circuit is obtained on the base of the circuit presented in Fig 12. The formation of inverse input current is realized on current mirrors on VT2-VT5 transistors by means of subtraction from base current I3 of input current I2. The resulting current arrives at the input of comparator, realized on VT1, VT8-VT10 transistors, at the output of which the pulse of complementary time-matching voltage is formed. Fig 17 presents the results of circuit operation simulation. Current I1 of saw-shaped form with the period of 100μs and amplitude of 100μs. Reference current I3=100μA. Input optic flow is sent to the photodiode VD3, where it is transformed into input current I2, in our case of simulation the current I2=20μA. At the direct output Out1 the voltage pulse with duration of 20μs is formed, voltage pulse with duration of 80μs is formed at complementary output Out2.

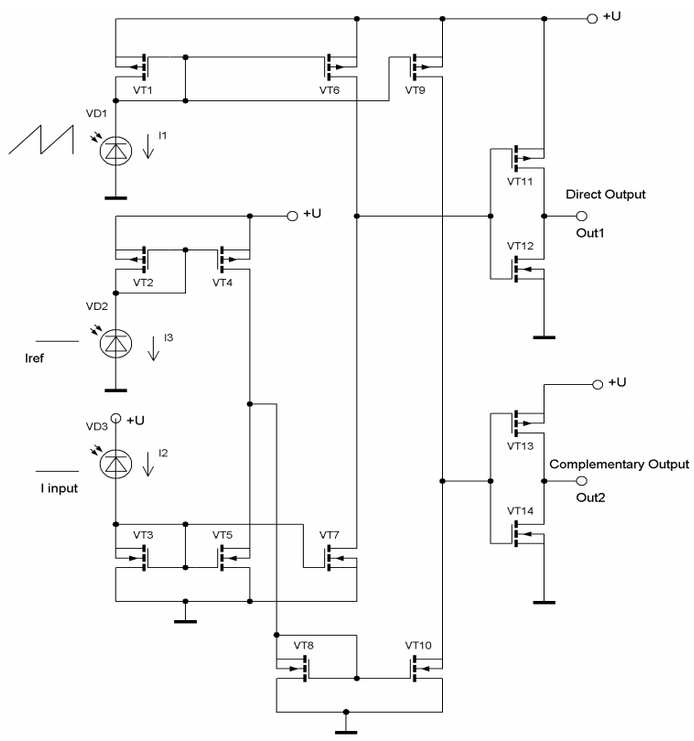


Fig. 16. Circuit of PWM with complementary outputs

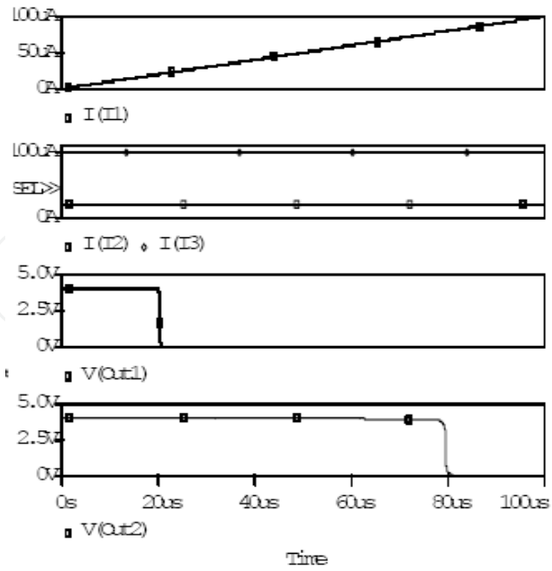


Fig. 17. Time diagram of operation of PWM with complementary outputs (I_{input} =20μA)

3.4.4 Designs and simulation of optoelectronic pulse-phase modulators

There are different ways to build PPM on different devices, particularly for optoelectronic applications (Krasilenko et al., 1995, a; Krasilenko et.al , 1995, c; Krasilenko et.al., 2003; Krasilenko et.al., 2001, h). We consider realization of PPM on CMOS transistor current mirrors and CMOS digital elements. The operation of phase-pulse photoconverter can be based on the two-threshold current comparator, at which output the voltage of logic "1" is formed, if the value of input signal is within the range of two thresholds values and the circuit consists of two current comparators, realized on current mirrors, and XOR gate. We considered current comparator on basis of current mirrors in work (Krasilenko et.al, 2004, b). PPM can be built in several ways. The first way assumes that saw-shaped currents of the same amplitude and period, but biased relatively each other by certain phase, are threshold currents. The drawback of the given approach is the necessity to use two saw-shaped current generators of high linearity. The linearity of the saw-shaped current generator in considered modulators will mainly determine the linearity of the modulators. The second approach is to use one generator of saw-shaped current $I1$, which will serve as the input current for two-threshold comparator. Input optic signal is converted by photodiode VD1 into the input photocurrent, which serves as the first threshold current $I2$, from which the current $I3$ of the second threshold is obtained by means of adding of small current ΔI, $I3=I2+\Delta I$ (Fig. 18).

The simulation results of the circuit by OrCad PSpice software are shown in Fig. 19. AMIS 1.5 μm technology CMOS transistors with minimal channel length and width (L=1.6μm, W=4μm) are used. The saw-shaped current $I1$ of 10μA amplitude and 10μs period arrives at the input of the first and second comparators, realized on VT4-VT10 transistors. The current ΔI=20nA and correspondingly duration of output voltage pulses equals 20ns. The range of input current is 100nA…10μA that corresponds to input optic power of 200nW…20μW if the photodiode responsivity is 0.5A/W. The PPM has ramp conversion law. As shown from simulation results, there is a big relative conversion error at small input currents because of

output pulse time delay. To reduce the error faster CMOS transistors or greater conversion period or input bias current must be used. The PPM power consumption is 83μW for 3V supply and does not depends on the period value (for values 10μs, 100μs, 1ms). Another variant of PPM on pulse-width modulator (PWM) is shown in Fig. 20. The PWM is realized on current comparator on transistors VT1-VT4, which form up and down current mirrors. Inverters on transistors VT7-VT10 form time-delay line that ensures 30ns delay if C1=1pF. When a saw-shaped current value becomes greater than an input current value the logic "1" voltage (3V for 3V supply voltage) is established at output Out1 and in 30ns at Out2. These signals come to XOR gate that extracts the output phase modulated pulse signal. Simulation results of the circuit for two values of input photocurrent, *I*2=1μA and 8μA are shown in Fig. 21. To reduce the relative conversion error at small input currents the bias current of 5μA is used. The range of input currents is 100nA…10μA. The full conversion period is 12μs. The relative conversion error is 0.1÷1% with taking into account the constant delay time. The power consumption is 83μW for 3V supply. To reduce input current values a current amplifier based on current mirrors at the circuit input can be used. For example, if the current amplification gain is 10 then the range of input currents will be 10nA…1μA that allows to operate with smaller input optic power (20nW…2μW for 0.5A/W photodiode responsivity). The same way can be used to construct PPM on PWM based on λ-devices, which can work with satisfactory parameters at frequencies up to 1MHz (Krasilenko et.al., 2003). The small power consumption of the considered above PPM enables successfully their integration in 2D-array with size of 128x128 elements and more and productivity equals 1…10Giga continuous logic operations per sec. The considered PPMs are realized on CMOS transistors so an array of such elements can easily be integrated with CMOS digital processing block.

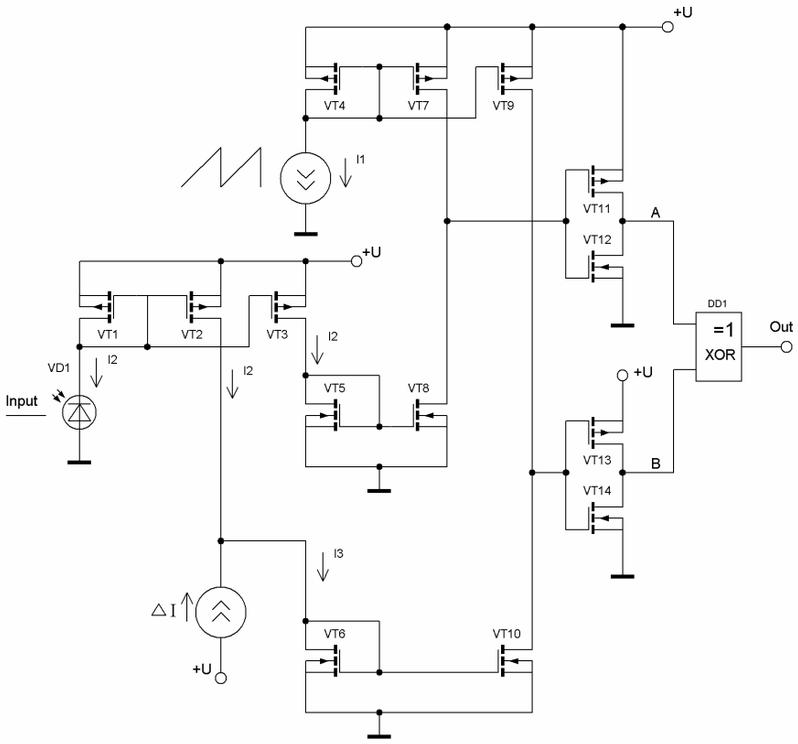


Fig. 18. Circuit of PPM on base of two-threshold comparator

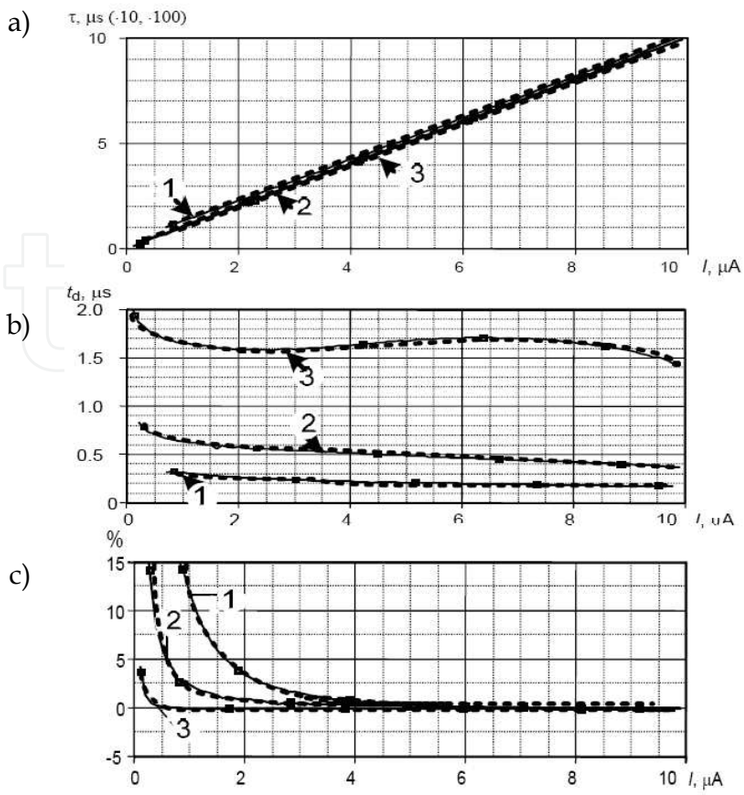


Fig. 19. Dependences of output pulse phase (a), time delay (absolute conversion error) (b) and relative conversion error (c) on input current for three values of conversion period: 1) 10μs, 2) 100μs, 3) 1ms

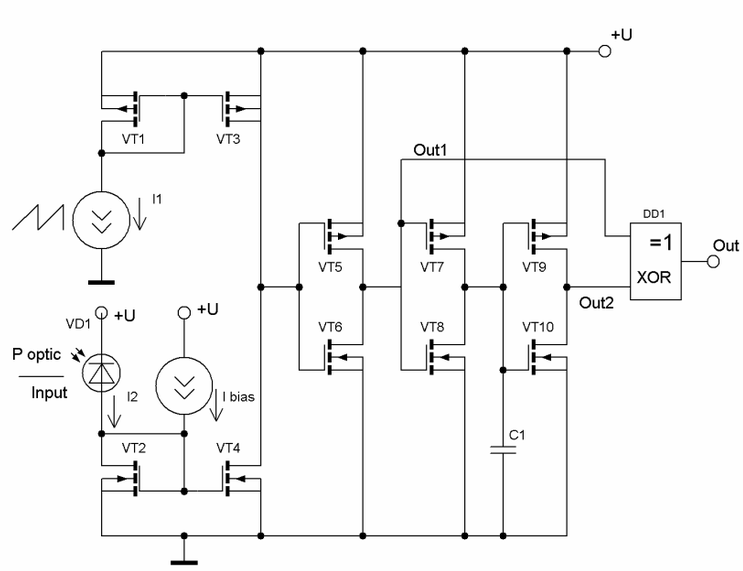


Fig. 20. PPM on base of PWM

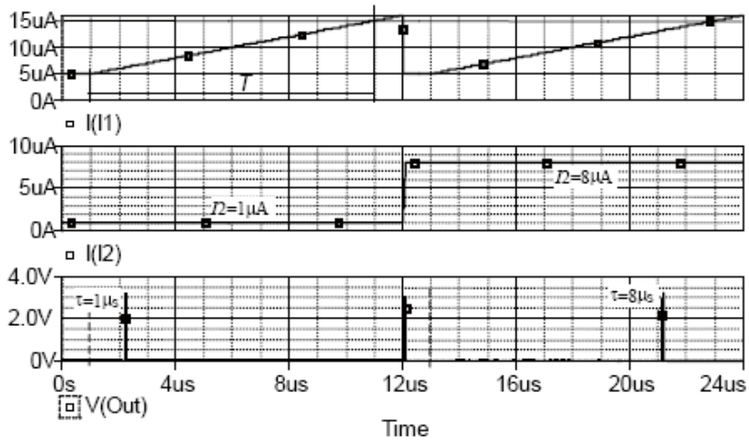


Fig. 21. Simulation results of PPM (Fig. 20)

3.5 Optoelectronic photocurrent logical elements on the basis of current mirror and comparators

3.5.1 Ground of necessity for universal photoreceiver logical elements for scalar-relation vector processors

The use of the mentioned above generalizing operations, among which it is possible to allocate such operations as min, max, restricted product, algebraic product, restricted subtraction and others of analog logics allows to determine not only difference between vectors, but also to discover any other relations between them, including the relations between matrixes. The research and demonstration of design results of optoelectronic scalar-relation vector processors (SRVP) with time-pulse coding are shown in work (Krasilenko et.al., 2005, a). Because the application of the standard bistable electronic logical element technology produces some known problems it is more promising a compromise between optic and electronic. Since at photoreceivers outputs we have current signals it is better to use current logic elements for the signals processing. And so the purpose of the work is design and simulation of current logical elements. At the same time a more wide set of operations ${}^{t,s}e_i$ is probable in such SRVP after elementwise processing over result vector $\vec{E} = \left\{ {}^{t,s}e_1, {}^{t,s}e_2, \ldots, {}^{t,s}e_n \right\}$. Therefore in a general view the SRVP can be described by the following model:

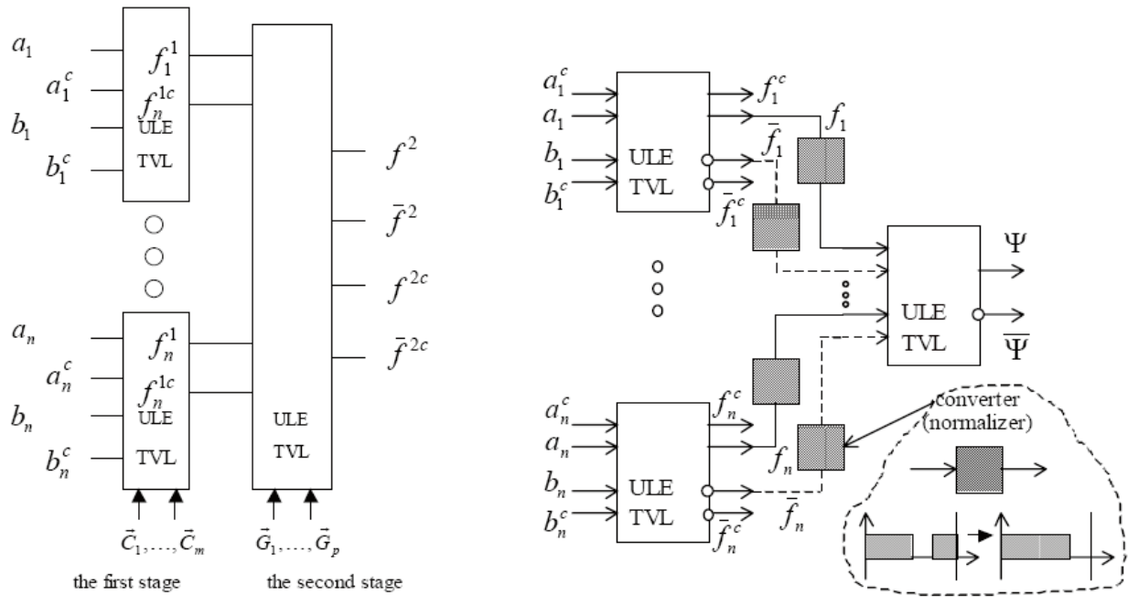
$$\Psi_{SRVP}\left(\vec{A},\vec{B}\right) = f^2\left(\vec{E}\right) = f^2\left(e_1\left(a_1,b_1\right),\ldots,e_n\left(a_n,b_n\right)\right) = f^2\left(f_1^1\left(a_1,b_1\right),\ldots,f_n^1\left(a_n,b_n\right)\right), \quad (9)$$

where f^2 - one of a set of possible functions mapping a vector $\vec{f}^1 = \left\{ f_1^1, \ldots, f_n^1 \right\}$ into Ψ, where Ψ, $f_i \in M = [0,1]$, i.e. $[0,1]\times[0,1]\times\ldots[0,1] \to [0,1]$, and f_i^1 - one of a set of possible functions mapping a vector $\left(a_i, b_i, 1-a_i, b_i\right) \to f_i$.

The scalar-relation vector processors considered in the given paper can be applied for decision of problems on the fuzzy logic basis. For such scalar-relation vector processors in each concrete case it is possible to select those or others *s*-norm and *t*-norm, but then the processor will execute only particular procedure. Such approach is perspective a little. Therefore we want to allot our scalar-relation vector processors by universality (or at least quasiuniversality), therefore requirements to such processors the following: changing type

of operations at algorithmic steps (f^1 at the first step, f^2 at the second step), we can ensure execution of required relations.

The structural diagrams of the scalar-relation vector processor are shown in Fig.22. It consists of a group of elements ULE_1-ULE_n (Fig.22a), which implement f_i^1 operations, and element of second stage, which implements function f^2 (see formula (9)). And, the type of *t*-norm operation (f_i^1) can vary with the help of special adjusting signals $\vec{C}_1 - \vec{C}_m$, and the type of *s*-norm operation (f^2) can vary too with the help of special adjusting signals $\vec{G}_1 - \vec{G}_p$. At the input of the scalar-relation vector processor the operands like vectors $A = \{a_i\}$ and $B = \{b_i\}$, $\left(i = \overline{1,n}\right)$, and also their complements $A^c = \{a^c{}_i\}$ and $B^c = \{b^c{}_i\}$ come. In structural diagram shown in Fig.22b output signals from universal logical element of two-valued logic (ULE TVL) come to a converter (normalizer) that realizes signals temporal integrations. The time diagram that explains the scalar-relation vector processor operation is shown in Fig.23.



a) b)

Fig. 22. The structural diagrams of the scalar-relation vector processor

A variant of two-valued logic universal logical element realization on the basis of current mirrors comparators (current mirror – CM) is shown in Fig.24. The ULE TVL is, as a matter of fact, a quasiuniversal element of time-pulse analogous logic. Changing the output elements functions by the help of adjusting signals C_{1i} - C_{4i} it is possible to evaluate simultaneously some functions. This circuit is, as a matter of fact, an analog-to-digital converter of parallel type. The time-pulse coding is selected for operands representation (Krasilenko et al., 1995, a), because it allows, using universal logic gates of two-valued logic, to implement the majority of continuous logic functions. Therefore at such coding our problem becomes simpler, as we can, tuning two-valued logic universal logic gates to any of possible two-valued operations with the help of signals C_{1i} - C_{4i}, implement the majority of

continuous logic operations and neuro-fuzzy generalizing logic, such as different *s*-norm and *t*-norm.

3.5.2 Designs and simulation results of the logical elements on the basis of current mirrors

Circuits that realize NOT, AND, OR functions with optical inputs-outputs are needed in many cases for max-min image processing. The circuit of an inverter on the bases of current mirrors comparator and its simulation results by PSpice OrCad are shown in Fig.25. The inverter has current (optical) input and current (optical if a proper LED driver will be connected) output. AMIS 1.5μm CMOS transistors MOSIS models were used. The supply voltage is 3V. The circuit shown in Fig.26 can realize both AND and OR functions depending on the reference current value. Both cases simulation results are shown in Fig. 26. Input optical signals and corresponding input currents are discrete and equal to 10μA in the considered case. The number of inputs can be up to 50 and more that is the advantage of the circuit. If the reference current is less than one input discrete than the circuit execute OR function. If the reference current is more than the sum of n-1 input discretes than the circuit executes AND function. If an additional current mirror is connected at the circuit output then we receive the current output. These circuits are based on current mirrors comparator and so their performance depends on the comparators and current mirrors performance. The comparator was considered in our work (Krasilenko et.al, 2004, b) and has the following characteristics: realized on 1.5μm CMOS transistors; the input currents range – 100nA...100μA; the supply voltage – 3...15V; the relative error is less than 0.5%; the output voltage time delays is 10…100ns. The using of more advanced CMOS technologies (0.35μm, 0.13μm and so on) can significantly improve the performance, in particular the operation speed. Time-pulse converters on CMOS current mirrors comparators and on λ-diodes were considered in our previous works (Krasilenko et.al, 2004, b; Krasilenko et.al., 2003). AND, OR and OR-NOT function circuits with current output and its simulation results are shown in fig. 27, 28, 29.

The conception of construction of the family of the offered optoelectronic photocurrent logical elements (OPLE) consists in the use of a few current mirrors realized on 1.5μm technology CMOS transistors. Connection of such mirrors with photodetectors and reference current generators allows also to create circuits realizing the limited difference operations of continuous current logic and current comparators with potential or current outputs. Presence of four – ten transistors, one – two photodetectors makes the offered circuits quite compact and allows their integration in 1D and 2D arrays. The factor of ramification at outputs and the factor of unification at inputs of the offered elements are greatly increased. Further we will consider simulation results of the circuits realizing different Boolean operations including AND, OR, OR-NOT, and others. Thus we will consider two variants of the circuits: 1- circuits with potential outputs; 2-circuits with logical current inputs and current outputs.The simulation results on the 1.5μm technology CMOS transistors showed that the level of logical unit can change from 1 uA to 10 uA for low-power consumption variants and from 10uA to 100uA for high-speed variants. Signals delays, values of fronts and cutoffs at operation with impulse logical signals with 1uA logical unit are not exceed 70-140ns and at operation with impulse logical signals with 100uA logical unit are no more than 4-6ns and the consumption power is 200-400uW.

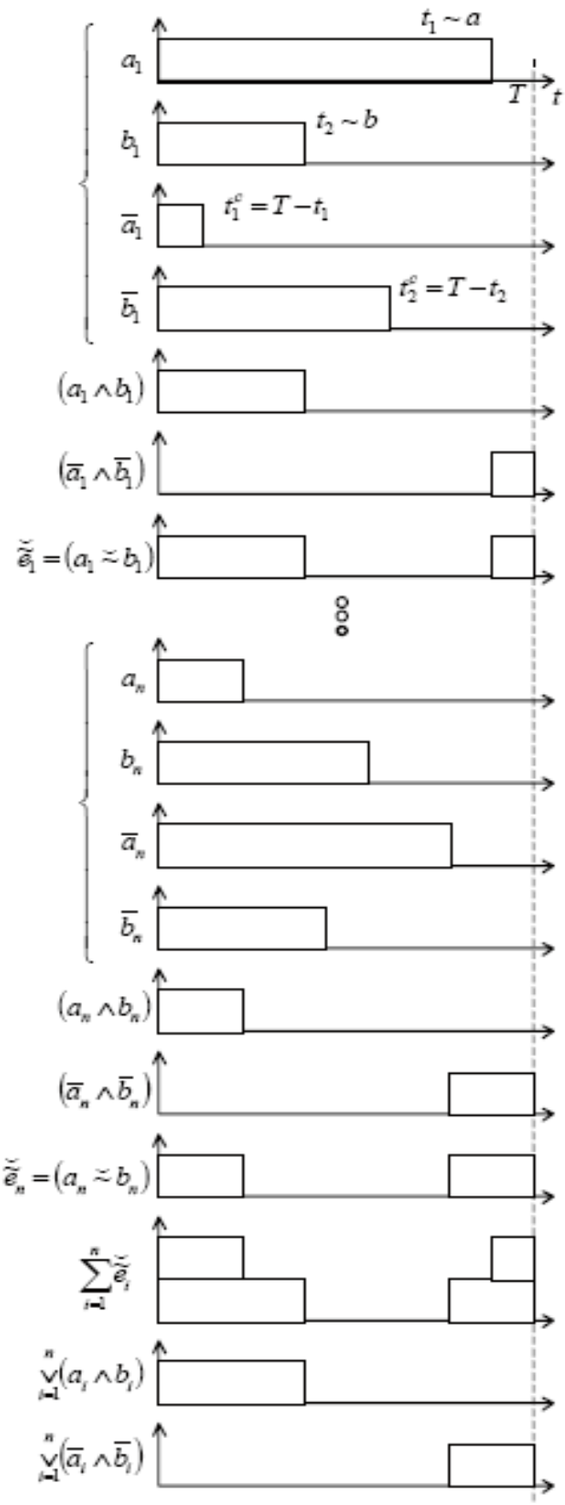


Fig. 23. The time diagram of the scalar-relation vector processor operation

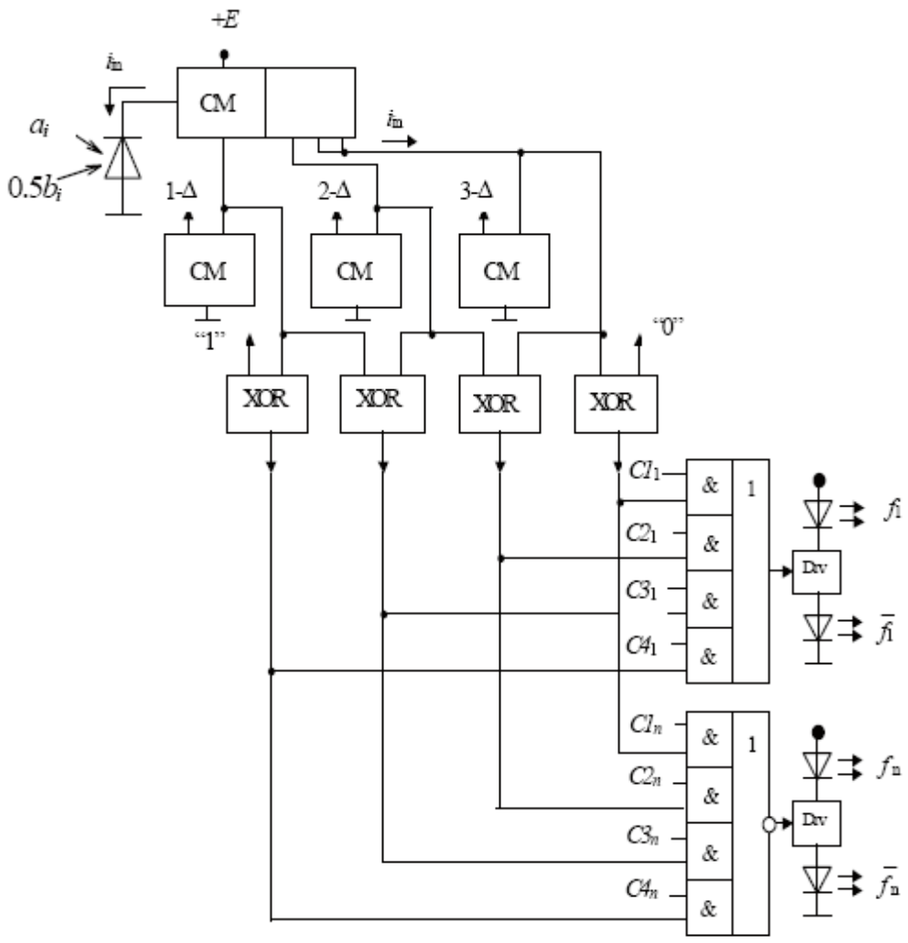


Fig. 24. The universal logical element of two-valued logic

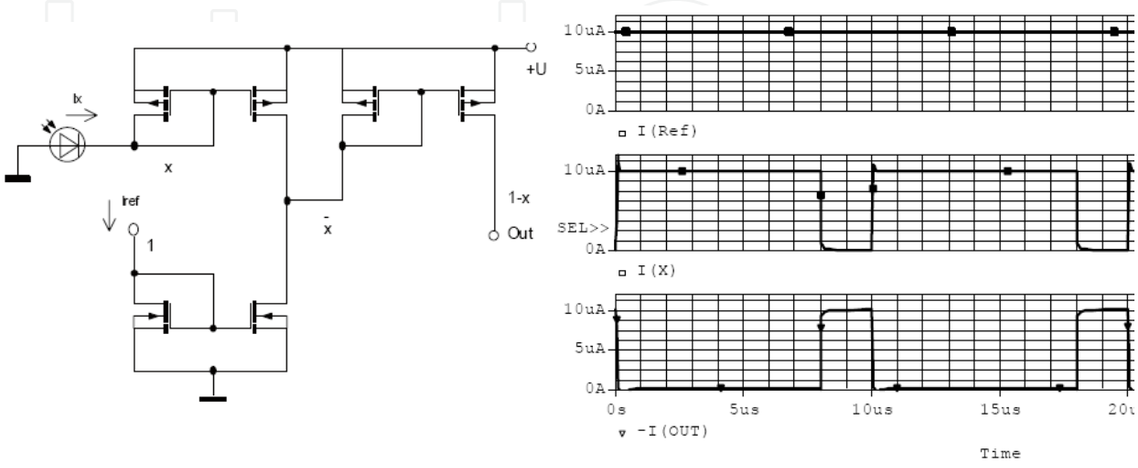
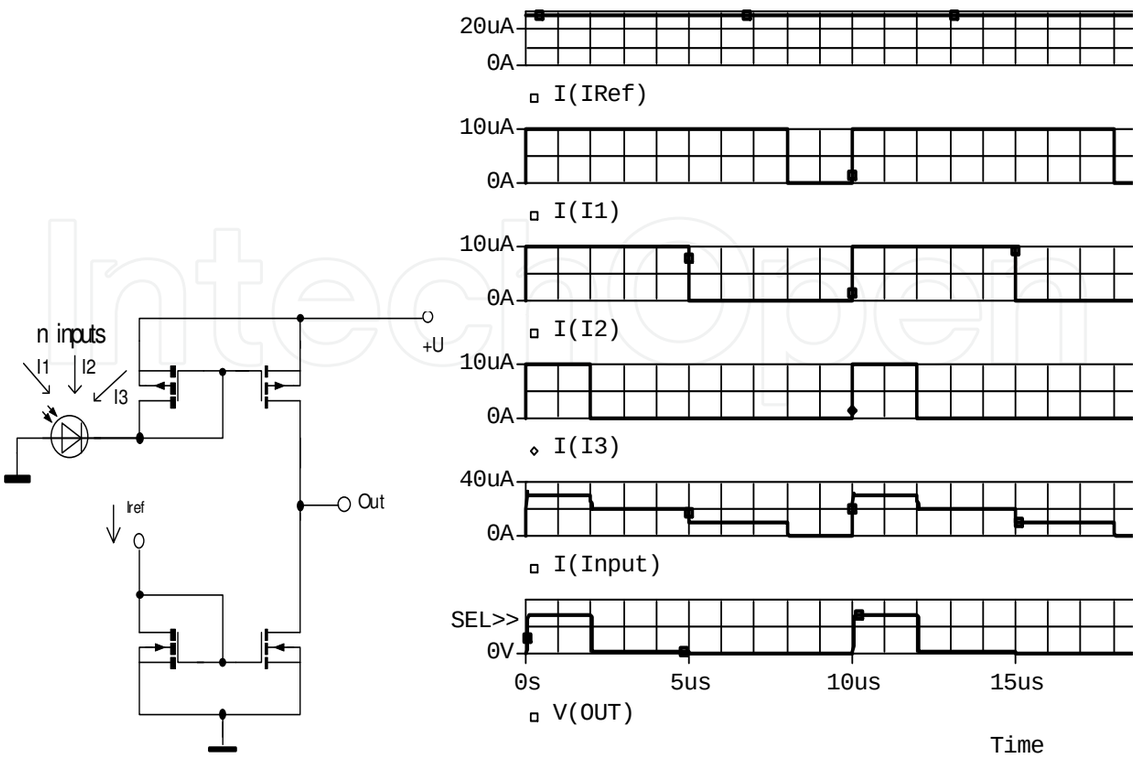
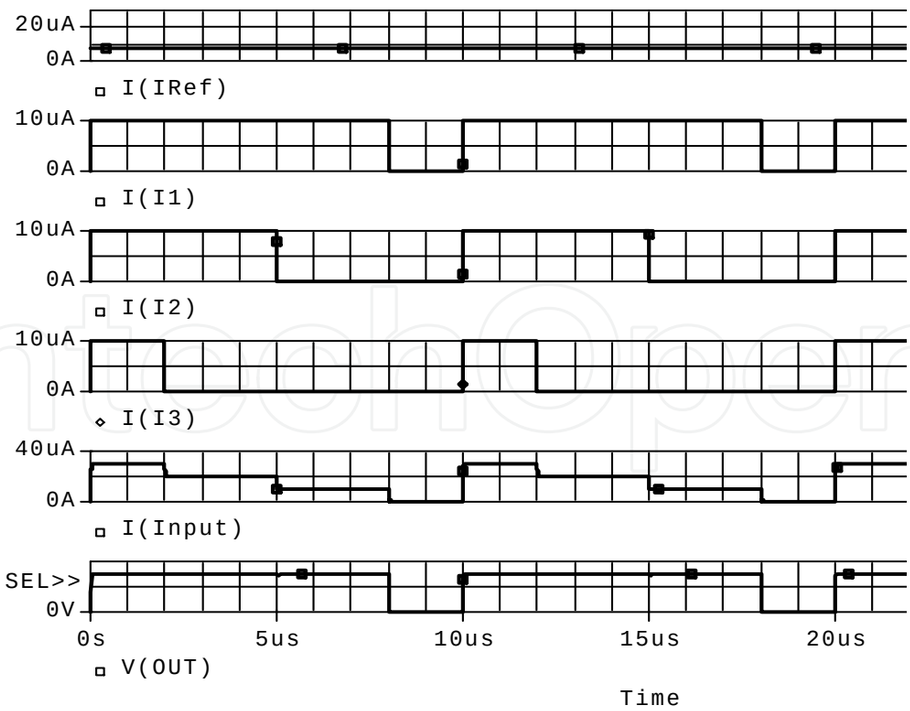


Fig. 25. Inverter circuit on current mirrors and its simulation results



Time diagram of realization of AND function



Time diagram of realization of OR function

Fig. 26. AND (OR) circuit with potential output on current mirrors and its simulation results

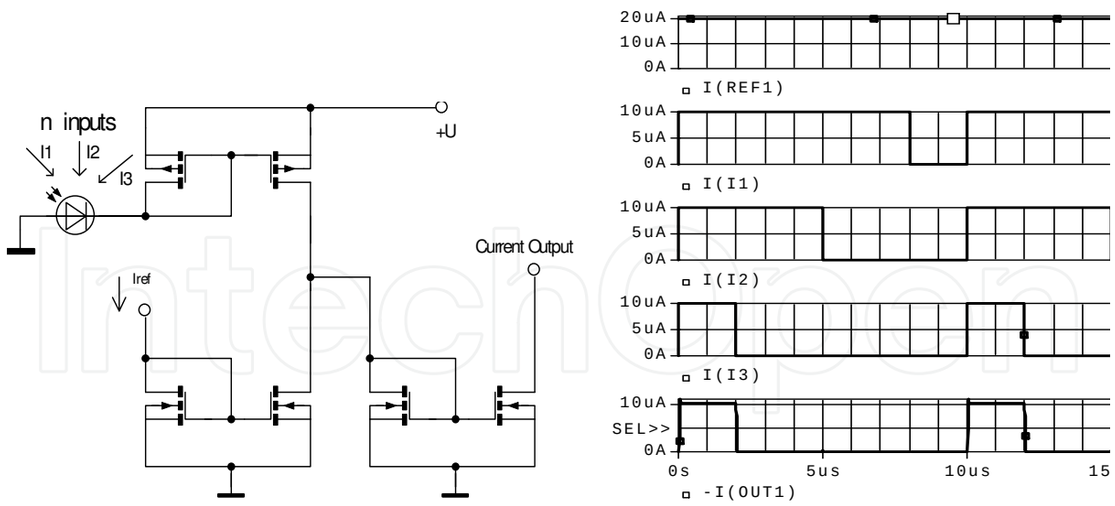


Fig. 27. AND function circuit with current output and its simulation results

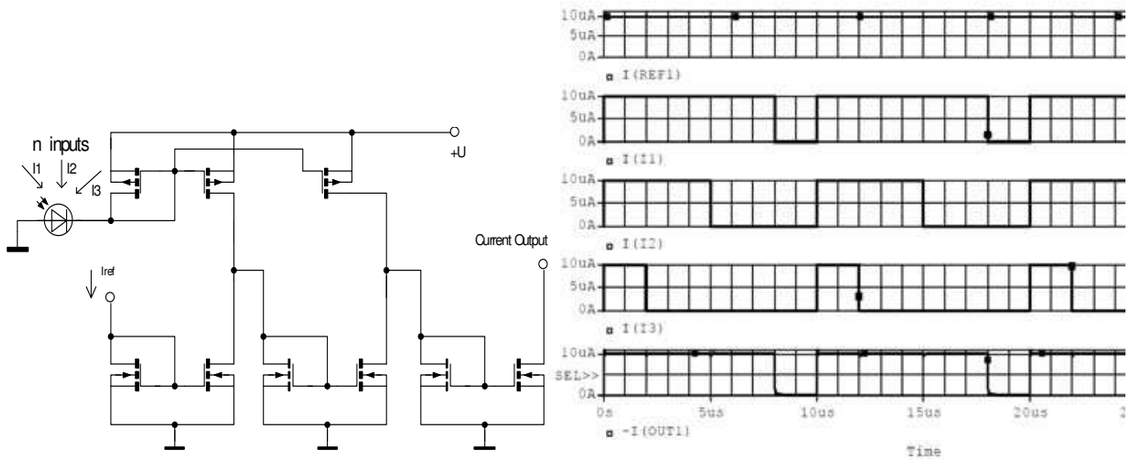


Fig. 28. OR function circuit with current output and its simulation results

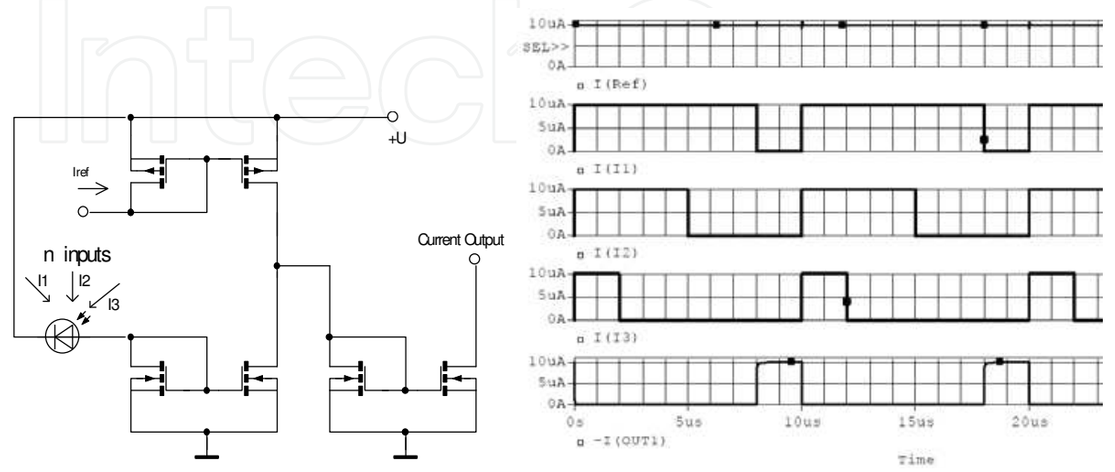


Fig. 29. OR-NOT function circuit with current output and its simulation results

3.6 Spatial-time integrators and equivalence neural elements on their basis

3.6.1 Spatial-time integrators

Realization of integrators on current mirrors on CMOS-transistors is perspective due to their circuit simplicity and compatibility with the well developed CMOS technology of modern integral digital microcircuits. An integrator of the time type consists of two current mirrors (Fig. 30). Transistors VT1 and VT2 are intended for integration (algebraic accumulation) of input signal; VT3, VT4 - for result of integration memorizing. An input optical signal is transformed in photocurrent with photodiode, and the signal controls keys S1 and S2.Then the input signal is on, the key is on. If the signal is off, the key if off. Integration is carried out due to charge of capacities C1 and C2, which hold a value of output current to the end of transformation cycle. Thus the output current value is determined by the sum of input signal pulse durations during the period of integration (Fig. 30,b). For example in Fig. 30 value of input signal pulse duration at the first period of integration is 50μs, at the second period - 100μs, and at the third - 150μs. The output current is proportional to the overall input signal pulse durations, so after the third period the output current value is 5+10+15=30μA. Thus the circuit carried out integration of input signals during three periods. The integration circuit has relative error 1…2 %. Input signals photocurrent range 1-100μA, power consumption 100…500 μW, signal period 0.1…1ms, output current delays – less 1μs Maximal amount of periods, during which the circuit can carry out integration of input signals, is limited to the maximal possible output current. If value of maximal output current is 100μA the maximal amount of periods of integration for this circuit is 10 for 10μA maximal current input signals.

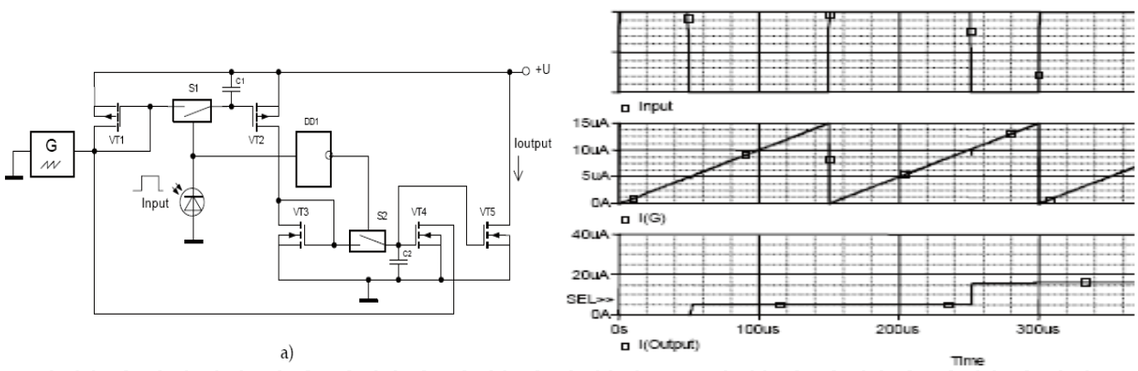


Fig. 30. Integrator circuit (a), time diagrams (b)

In the same way it is simple to provide the spatial integration of optical signals (Fig. 31). Input optical signals are converted in photocurrents with photodiodes and the signals control corresponding keys S1 of selection and storage devices on current mirrors. Accumulative signal of integration is written in the output device at the end of period by the control signal of generator G2. Thus the output current is determined by duration of input signals from every optical channel. For example in Fig. 31 there are three optical channels and input optical signals are 50μs, 20μs, 30μs accordingly. The output current after the first period is determined by the pulse duration sum of input signals and it is equal to 5+2+3=10μA. Maximal amount of input signals is determined by the maximal possible output current. The considered circuits can also perform time integration during some periods, so it performs spatial-time integration. Circuit simplicity and small power

consumption allows to create arrays of such integrators with size 10x10 and more. The range of input photocurrent is 0.1-10μA, transformation time (period) 100-1000μs, supply voltage 1.5V, average consumption power 150μW per channel.

3.6.2 Neural elements circuits for equivalence and non- equivalence functions

The family of new functions "equivalence" and "non-equivalence" of neuro-fuzzy logic, which we have elaborated on the based of such generalized operations of fuzzy-logic as fuzzy negation, t-norm and s-norm are shown in paper (Krasilenko et al., 2002, a). The functions are prospective for neural networks creation with selforganization and artificial intelligence properties. New generalized operation of equivalence (non-equivalence) operation can be written in the following form: $^{t,s}E'(a,b)=(atb)s(a_n tb_n)=(atb)s(\overline{a}t\overline{b})$, and *t*-norm and *s*-norm of any of their variants can be used. The analysis of the whole spectrum of all possible $^{t,s}E'(a,b)$ shows, that the following operations are the most interesting in case of certain *t*- and *s*-norms (Krasilenko et al., 2002, a). New generalized operation of equivalence of II type (non-equivalence) can be written in the following form: $^{s,t}E''(a,b)=(asb)t(\overline{a}s\overline{b})$, or taking into consideration the law of De Morgan so: $^{s,t}E''(a,b)=\left((asb)_n s(\overline{a}s\overline{b})_n\right)_n=\left((\overline{a}t\overline{b})s(atb)\right)_n=\left(^{t,s}E'(a,b)\right)_n=\overline{^{t,s}E'(a,b)}$

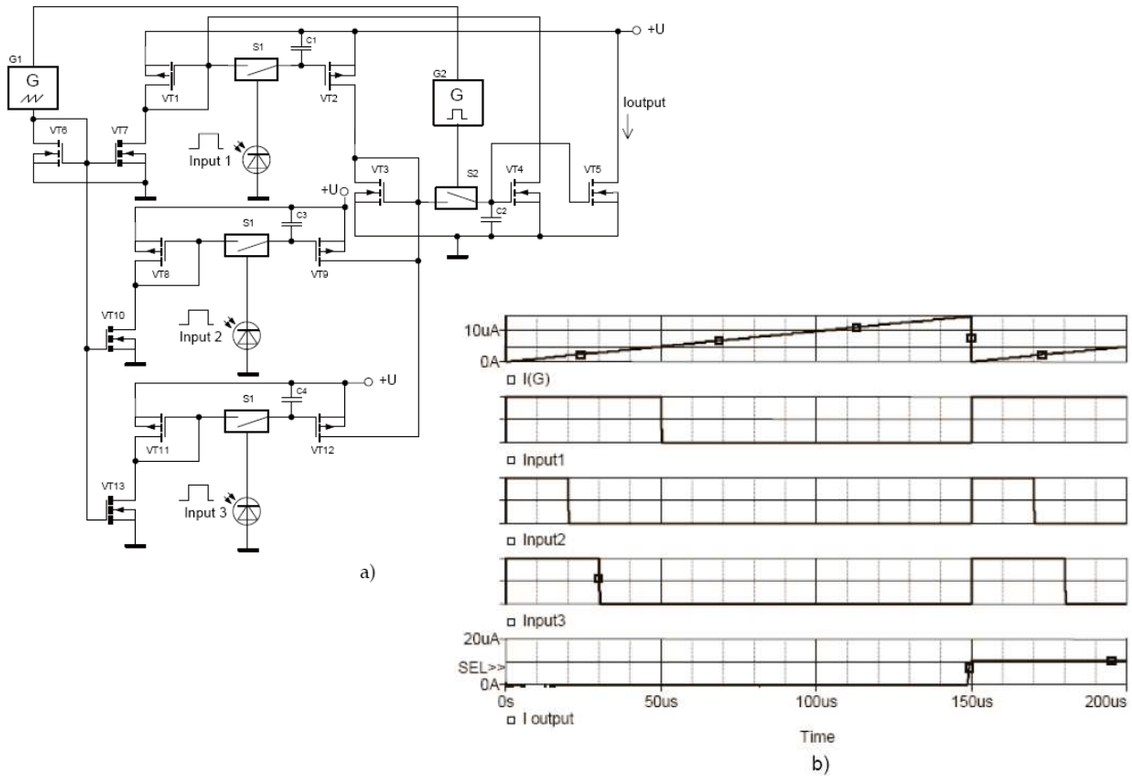


Fig. 31. Spatial-time integrator (a), time diagrams (b)

The II type of operations can be called the operation "non-equivalence" of the I type and designate it as:

$$ {}^{t,s}NE'(a,b) = {}^{s,t}E''(a,b) = \left({}^{t,s}E'(a,b)\right)_n . $$

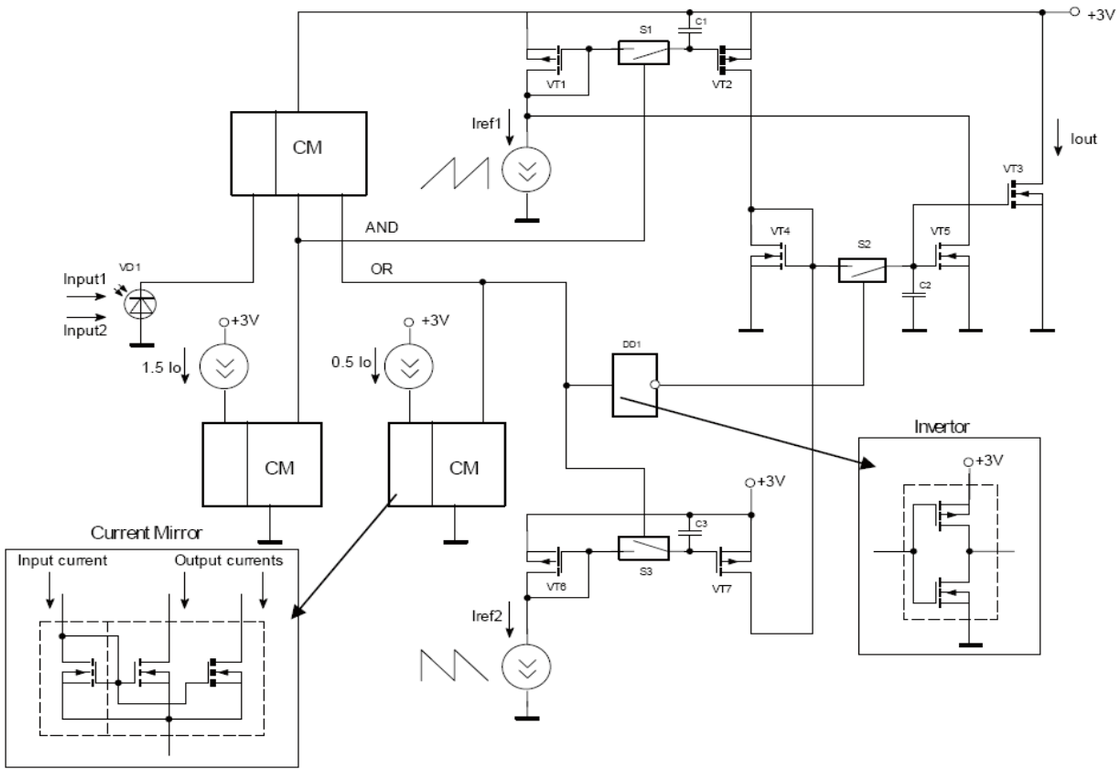


Fig. 32. Equivalence (non-equivalence) function circuit

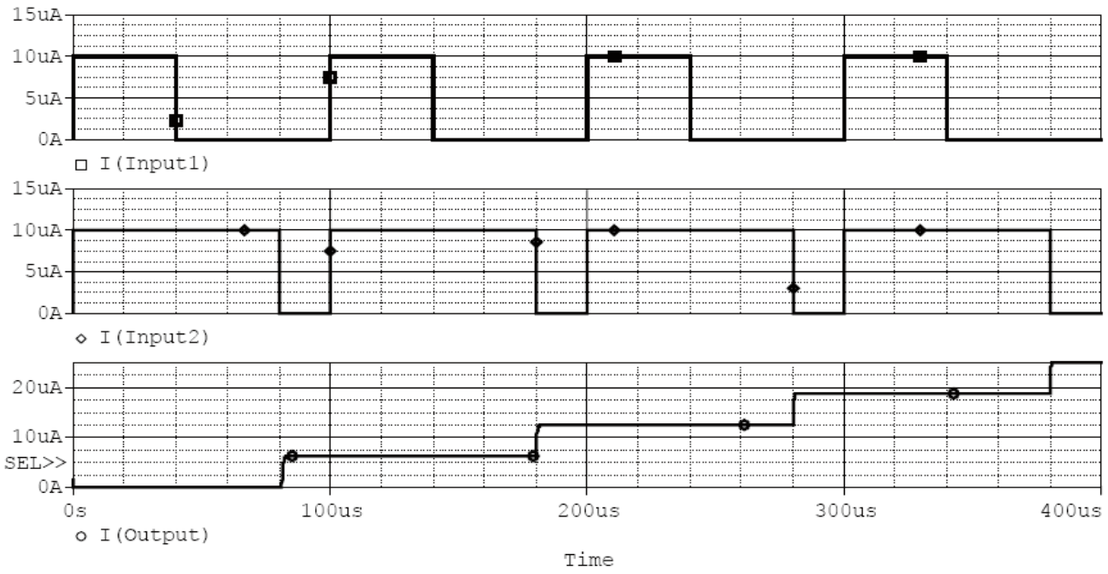


Fig. 33. Time diagrams of the equivalence circuit operation

Thus, the functions determine new generalized operations of comparison (determination of equivalence or non-equivalence).
The equivalence (non-equivalence) functions can be realized on current mirrors and the proposed integrators. Output current value Iout is the equivalence of two input optical signals pulse durations (Fig. 32). In the circuit CMOS current mirrors (CM) with one and two outputs are used. For example in Fig. 33 input signals pulse durations 40μs and 80μs (the equivalence of the input signals is 60μs), period 100μs, Io=10μA, output current after the first period Iout=6uA, after the third period Iout=18μA (Fig. 33), relative error about 3%, as more than one integrators and current mirrors are used and their errors are summed.
To obtain non-equivalence function circuit the reference saw-tooth current generators Iref1 and Iref 2 must be interchanged. For above mentioned input signals the non-equivalence of input signals is 40μs (it is the time then signals are different), so the output current after the first period Iout=4μA, after the third period Iout=12μA.

3.6.3 Weighted and non-linear integration for neural elements circuits for equivalence and non- equivalence functions

The algebraic spatio-temporal weighted integration of optical signals can be realized by the integrator with variable slope angle of saw-tooth current generator G (Fig. 34). For example in Fig. 35, input signal pulse duration 50μs, period 100μs. The saw-tooth current generator G determines integration weight. If maximal saw-tooth current is 10uA than transformation weight is 0.1 μA/μs. So after the first period output current is 5μA. At the second period maximal saw-tooth current is 10μA that corresponds to transformation weight of 0.15 μA/μs. So the transformation weight is in 1.5 times increased. After the second period the output current is 5+7.5=12.5μA. At the third period maximal saw-tooth current is 20μA that corresponds to transformation weight of 0.2 μA/μs. So after the third period the output current is 5+7.5+10=22.5μA. The considered circuit performs only time weighted integration of one input signals. But the circuit in Fig. 31 can perform spatio-temporal weighted integration of multichannel optical input signals if variable angle of slope of saw-tooth current generator G1 is used. The circuits can be used for neural networks adaptations.

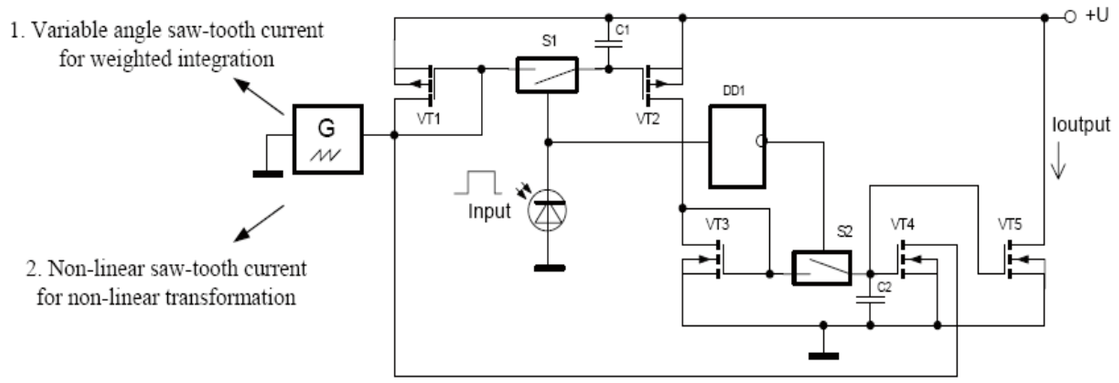


Fig. 34. Weighted or non-linear integrator

Non–linear signal transformation can be realized with the integrator circuit Fig. 34 if a non-linear saw-tooth current generator is used. For example in Fig. 36 input signal pulse durations are 20μs, 50μs, 80μs, and period 100μs. An exponential function for saw-tooth current generator G is used (Fig.36). So we get exponential transformation of input signals.

After the first period the output current is 7.5μA, after the second period the output current is 7.5+9.5=17μA, and after the third period the output current is 7.5+9.5+10=27μA. Thus in spite of identical input signals there are different corresponding output current values. The circuit can be used for non-linear neural networks activation functions. The non-linear transformation signals function is determined by a non-linear function of saw-tooth current generator G.

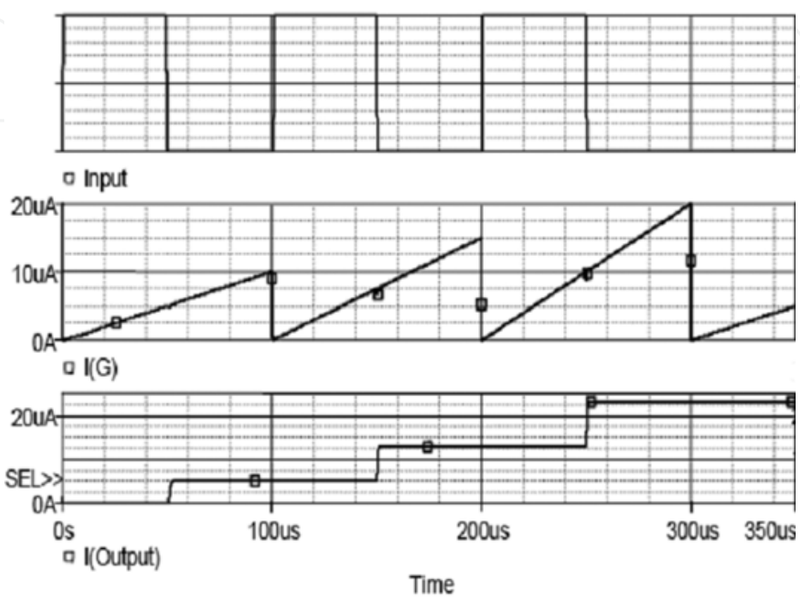


Fig. 35. Time diagrams of weighted integration

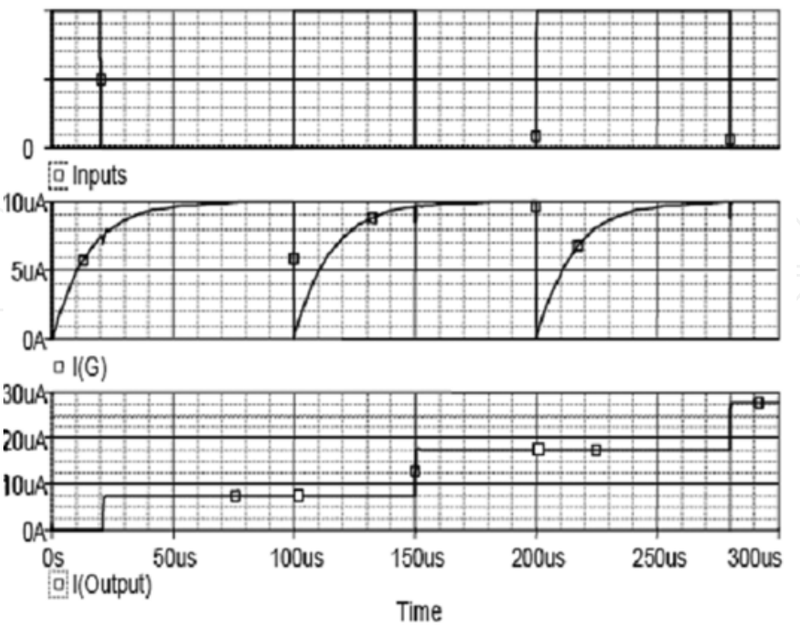


Fig. 36. Time diagrams of non-linear signal transformation

4. Conslusion

We consider design and hardware realizations of optoelectronic logical elements of two-valued logic with current inputs and current outputs on the basis of CMOS current mirrors. In the chapter we consider the whole family of the offered circuits, show the simulation results and possible prospects of application of the circuits in particular for time-pulse coding for multivalued, continuous, neuro-fuzzy and matrix logics. We consider neurons design and simulation results of multichannel spatio-time algebraic accumulation - integration of optical signals. Advantages for nonlinear transformation and integration are shown. The integrator-neuron is based on CMOS current mirrors and comparators. The performance: consumable power – 10…500 μW, signal period– 0.1…5μs, input optical signals power – 0.2… 20 μW; time delays – less 0.01-1μs, the number of input optical signals - 2…64 and more, integration time – 10…100 of signal periods, accuracy or integration error – about 1%-10%. A biologically motivated concept and time pulse encoding principles of continuous logic photocurrent mirrors and sample-storage devices with pulse-width photoconverters have allowed us to design generalized structures for realization of a family of normalized linear vector operations "equivalence"-"nonequivalence".

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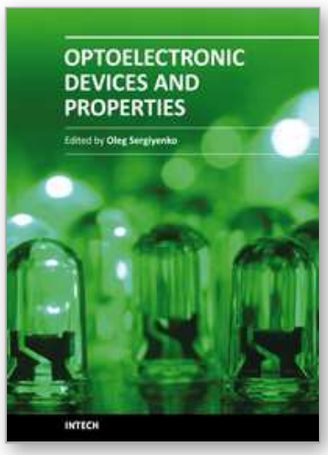

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