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VLSI Implementation of Least Square Channel Estimation and QPSK Modulation Technique for 2×2 MIMO System

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1. Introduction

Future Wireless communication systems have to be designed to integrate features such as high data rates, high quality of service and multimedia in the existing communication framework. Increased demand in wireless communication systems has led to the demand for higher network capacity and performance. Higher bandwidth, optimized modulation offer practically limited potential to increase the spectral efficiency. Hence MIMO systems utilizes space multiplex by using array of antenna's for enhancing the efficiency at particular utilized bandwidth. MIMO use multiple inputs multiple outputs for a single channel. These systems are defined by spectral diversity and spatial multiplexing. MIMO describes the ways to send data from multiple users on the same frequency/time channel using multiple antennas at the transmitter and receiver end.

A transmitter/receiver system uses multiple antennas not only for transmitting data between corresponding antennas but also between adjacent antennas. The data is received in the form of MIMO Channel Matrix. A top level MIMO system (Joseph et al., 2007) is shown in Fig.1.1. MIMO system is used in many applications like WiMax, Wi-Fi, WLANs, and many more applications.

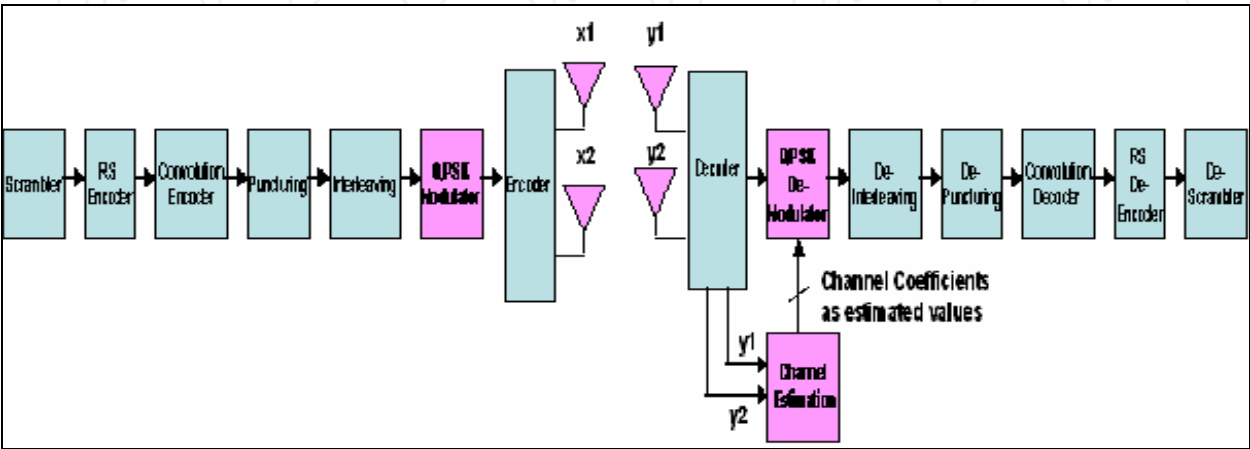


Fig. 1.1. MIMO System

In recent years the telecommunications industry has experiencing a tremendous growth in the area of wireless communication. This growth has been ignited the widespread popularity of mobile telephones and wireless computer networking. But there are limits to growth, and the radio spectrum used for wireless communications. Hence considerable effort has been invested in making more efficient use of the resources. Using the spectrum more efficiently caters for the ever increasing demand for faster communications since more bits per second can be transmitted using the same bandwidth. Recent major industry research focus in this area has been the use of multiple antennas for transmitting and receiving instead of the single antenna systems. The uses of multiple transmit and receive antennas, and efficient coding techniques could increase the performance of wireless communication systems. The implementation carried is for 2x2 MIMO systems with good channel estimation method and better coding techniques for better performance. The design is carried till the backend VLSI flow. The design is to implementing 2x2 MIMO systems with QPSK modulation technique and estimating channel coefficients using LS channel estimation method.

2. Back ground discussion

Due to demand in the wireless products, the high data rates, capacity, accuracy, with less hardware and the reliability of the system is a greater challenge. Hence numerous efficient channel estimation and modulation techniques are to be modified for greater performance of the overall system. In this, literature review is carried for different MIMO architectures for different modulation techniques and the channel estimation methods.

In digital communication system the channel accepts electrical/electromagnetic signals, and the resultant output is smeared or distorted version of the input due to the non-ideal nature of the communication channel. Also the information-bearing signal is corrupted by unpredictable noise. The smearing and noise introduce errors in the information being transmitted and limits the rate at which information is to be communicated from the source to the destination. The probability of incorrectly decoding a message symbol at the receiver is often used as a measure of performance of digital communication systems. The main function of modulator and the demodulator is to combat the degrading effects of the channel on the signal and maximize the information rate and accuracy.

In digital modulation, information signals to be modulated is digital. Therefore, digital information modulates an analog carrier and hence called as "digital modulation". There are basically three types of digital modulation techniques i.e Amplitude Shift Keying (ASK), Phase Shift Keying (PSK) and Frequency Shift Keying (FSK). Phase Shift Keying is a digital modulation technique which is one most used. In PSK modulation, the phase of the carrier is altered in accordance with the input binary coded information. The PSK is further subdivided into BPSK, 8-PSK, 16-PSK, QPSK, DPSK. In binary phase shifting keying the transmitted signal is sinusoid of fixed amplitude. It has one fixed phase.

Chia-Liang Liu (Chia L.L, 1998) explained the impact of I/Q imbalance on QPSK-OFDM-QAM Detection. The in-phase and the quadrature phase components are very important component in QPSK. Any imbalance in these the performance of the whole system crashes down at the detectors. Either the phase or the amplitude imbalances lead to the introduction of ICI, there may be cross-talk between in-phase and quadrature channels.

Wout Joseph, et.al. (Joseph et al., 2007) proposed an algorithm for the performance study on IEEE 802.16-2004 for different conditions like for different channel models and MIMO

system. Different channel models are compared by applying different diversity schemes. The goal is to analyze the performance of WiMax system. Performance study is carried for 2x2 and 2x1 MIMO systems. The configuration of WiMax transmitter and receiver are done for MIMO and SISO. Initially a model was implemented in MATLAB/Simulink.

Yantao Qiao, et al. (Yantao.Q et al., 2005), has made a research on an iterative algorithm of least square channel estimation in MIMO OFDM systems. The main objective of this paper is an iterative channel estimation algorithm for MIMO OFDM. Compared to common least square channel estimation, this has greatly improved estimation accuracy and, low pass filtering in time domain reduces AWGN and ICI significantly. MIMO-OFDM is used in mobile applications. Many techniques have been applied to the MIMO channel both in time and frequency domains which increases the capacity and increase the reliability of wireless link.

Cui.S et al., (Cui.S et al., 2004) proposed channel estimation in MIMO wireless communication systems plays a key role in the performance of the space time decoders that depends on the accuracy of the channel knowledge .In this paper the study of the performance of the MIMO channel estimation using training sequence is carried out. The Least Square, MMSE and new scaled least square approaches to the channel estimation are studied and the optional choice of the training signals is investigated for each of these techniques.

Sarod Yatawatta, et.al,(Yatawatta.S et al.,2005) proposed a solution for minimizing the energy spent on during the channel estimation when subjected to known error and delay when timing symbols are transmitted. The minimization of energy is carried by reducing the hardware, also by using a low rank equalization at the receiver. A scalar energy reduction at channel estimation is explained,

Benoit Le Saux, et.al,(Sanx.B.L, 2006) proposed a MIMO system with OFDM has greater potential like reduction in inter-symbol interference, decrease in fading, increase in bandwidth, and increase in data rates. The performance of MIMO system degrades due to inaccurate channel estimation over frequency selective fast-varying channels. Pilot-aided turbo channel estimation improved by addition of linear algorithm in the iterative process is discussed. This improves the channel estimation and reduction in the use of number of pilots.

Changchuan Yin, et.al,(Changchuan.Y et al.,2006) presents the theoretical and simulation results for LS channel estimation in MIMO-OFDM based on 2 types of pilot structure i.e. block type pilot and the comb-type pilot. The CSI is obtained by blind channel estimation and pilot aided channel estimation. The pilot based channel estimation is based on LS or MMSE criterion. LS channel estimation is more practical then MMSE because LS does not require extra information about channel correlation and noise variance.

Riza Abdolee, et.al,(Reza A et al., 2007) proposed a method to reduce the computational complexity of channel estimation algorithm for MIMO-OFDM. Channel estimation suffer from high computational complexity. Solution for high efficient channel estimation and simplified computational complexity is stated. Normal matrix inversion is solved using QR decomposition method. This method is used to simplify LS method. The results show QR decomposition can greatly reduce the complexity of LS channel estimation.

Deseada Bellido, et.al,(Bellido et al., 2007) proposed LS channel estimation algorithm for MIMO-OFDM. This evaluation has been made using pilot design rules that guarantee a bounded error level for the estimation. This method is used for estimation of the channel matrix. Diversity technique is used for channel matrix. The capacity of channel depends on

the knowledge of the channel matrix gains at the transmitter and receiver. The estimation is carried out by transmission of set of pilot symbols known to transmitter and receiver.

Markus Myllyla, et.al,(Markus M et al., 2006) proposed a method for performance evaluation of FPGA implementation of a LMMSE based detector for radio channels. Complex part of high level 2x2 LMMSE detector blocks which is solved by CORDIC based architectures.

Sudhakar, et al (Sudhakar et al., 2009) proposed a design method and FPGA implementation of channel estimation and Modulation technique for MIMO system.

3. Problem definition/statement

While designing VLSI circuits for very efficient implementations the designer should consider algorithmic and hardware architectures trade-offs. Rapid prototyping for such applications will imply the short designs satisfying all the design constraints, such as timing and silicon area. The wireless systems are operated under harsh and challenging channel conditions. A 2x2 MIMO system is been designed, simulated, implemented, synthesized and physical design is carried in macro level to tape out the design.

The aim of this work is VLSI implementation of LS channel estimation method and QPSK modulation technique for 2x2 MIMO system. The design specifications are verified using MATLAB. The RTL coding is carried for the design to be implemented on Xilinx FPGA. Design synthesis and macro level physical designing is also carried out.

The main Objectives of the present work on MIMO Systems are

- To review literature on MIMO and its architecture, various channel estimation methods and QPSK modulation technique.
- To identify a channel estimation method for MIMO architecture.
- To model and simulate MIMO system with QPSK modulation technique.
- To implement and optimize MIMO System on FPGA.
- To verify MIMO system for its functionality.

The design methodology carried to meet the objectives is as follows. The flowchart is also shown in Fig.3.1 that shows the design methodology followed for developing 2x2 MIMO systems.

4. Least square channel estimation and QPSK modulation for 2x2 MIMO systems

The MIMO system has multiple transmitter antennas and multiple receive antennas so that the data is transmitted in parallel. This work demonstrates simple working of a 2x2 MIMO system carried till backend of the VLSI flow. The MIMO system is designed with least square channel estimation method and QPSK modulation technique.

In communication systems, channels are usually multi-path channels, which cause inter-symbol interference in the received signal. As discussed in literature review various detection algorithms offer a very good receiver performance and reduced computations. Channel estimators require the channel impulse response. The channel estimation is based on the known sequence of bits called training sequence which is unique for each transmitter. Here the known training sequence is transmitted so that the channel coefficients are obtained. There are different standards used for transmitting training sequence like IEEE 802.16 standard.

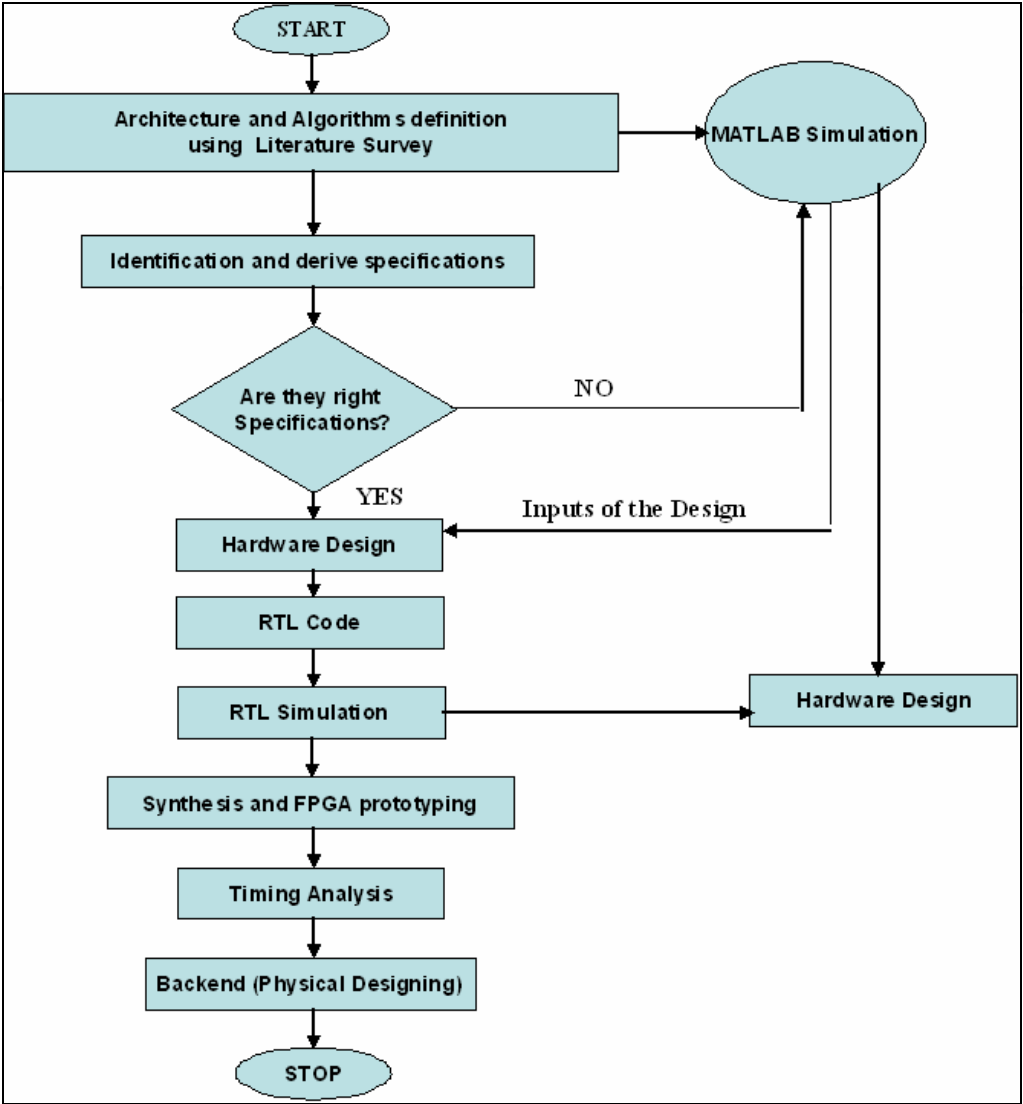


Fig. 3.1. Flow Chart showing methodology carried for Design

4.1 LS Channel estimator for 2x2 channel

2x2 joint channel estimation is considered for the MIMO design. The channel is considered to be ideal wherein noise is not taken in account. The sequence ‘x’ is taken from 2 different transmitters and 4 channel paths are considered as shown in Fig.4.1. From each transmitter unique training sequences are transmitted in concatenation with the QPSK modulated data. The training sequence is transmitted for the identification of the transmitter from which the data is obtained at the receiver end. Here diversity technique is used but the Alamouti encoder and decoder is not used.

The 2x2 channel estimation block diagram is shown in Fig.4.1. Initially the training sequence is transmitted so that the channel coefficients are calculated. First the transmitter is made active and the training sequence is sent. The tx2 is made inactive i.e. nothing is sent from tx2. The h11 and h12 channel coefficients are obtained. Then the tx1 is made inactive and tr2 is sent through tx2. Then the h21 and h22 coefficients obtained by simplifying the equations. The data obtained at the receivers rx1 and rx2 are shown by the equations (1) and (2).

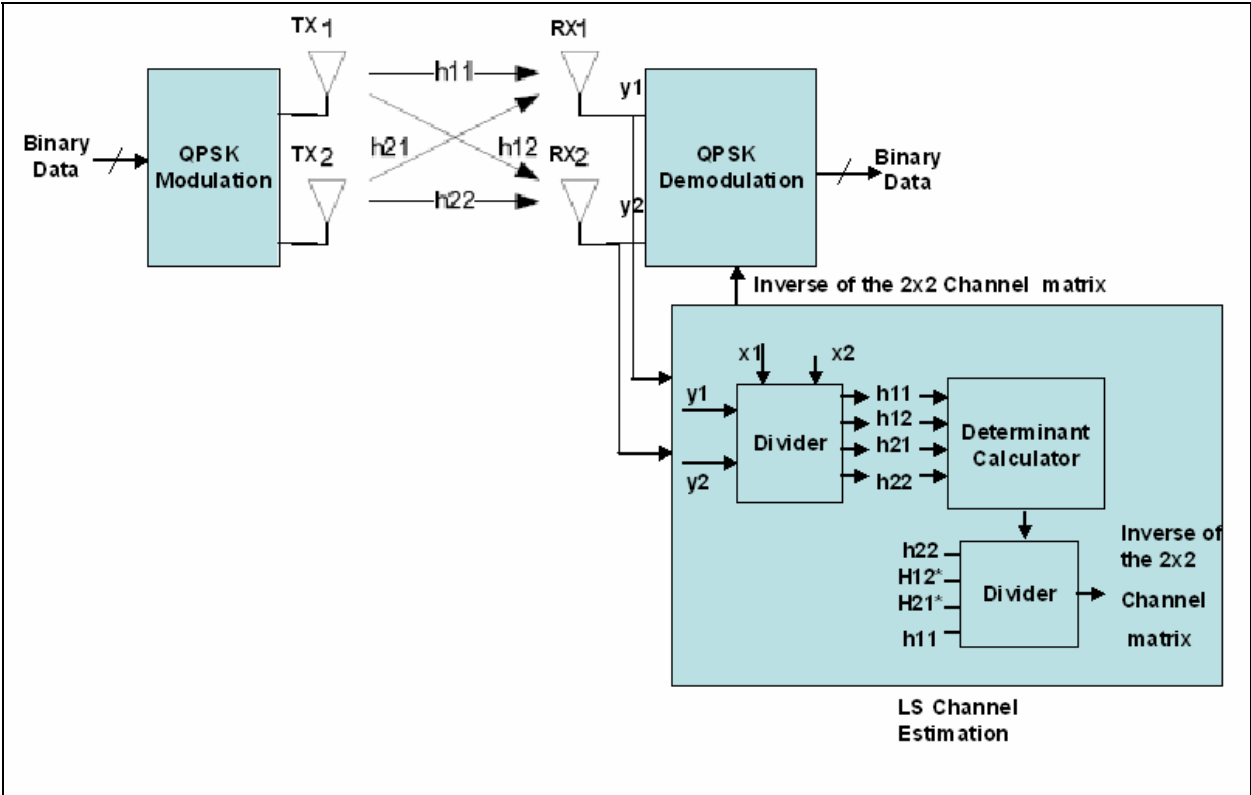


Fig. 4.1. QPSK modulator/demodulator with LS channel estimation

$$y1 = x1 * h11 + x2 * h21 \tag{1}$$

$$y2 = x1 * h12 + x2 * h22 \tag{2}$$

After which the transmitted bits are decoded by multiplying y with the inverse of the 2x2 channel matrix h .

$$h^{-1} = y/x \tag{3}$$

4.2 QPSK Modulation technique for 2x2 channel

Phase shift keying is a digital modulation technique; perhaps one of the most used in today’s digital communication systems. In PSK modulation scheme, the phase of the carrier is altered in accordance with the input binary coded information. The PSK is further subdivided into BPSK, 8-PSK, 16-PSK, QPSK, DPSK. In binary phase shifting keying the transmitted signal is sinusoid of fixed amplitude .It has one fixed phase. The Fig 4.2 shows wave form of phase shift keying. The QPSK is a phase modulation scheme, used in constellation mapping. The constellation map of QPSK modulator is shown in Fig.4.3. Here the input bits stream is converted into complex stream using equation (4) and where I and Q both are in phase with I-out and Q-out respectively are shown in table 4.1. QPSK modulator accepts the binary bits as inputs consider as a symbol and converts them into complex value. QPSK takes only 4 symbols and generate its complex value in this fashion because the bit rate is 1/2.

$$D = (I +jQ)*K_{MOD} \text{ where } K_{MOD} = 1/1.414 \tag{4}$$

Input Bits	I-out	Q-out
00	-1	-1
01	-1	+1
10	+1	-1
11	+1	+1

Table 4.1. The Inputs and Outputs of QPSK Modulator

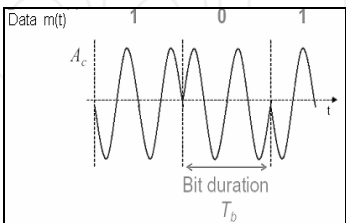


Fig. 4.2. Phase shift keying

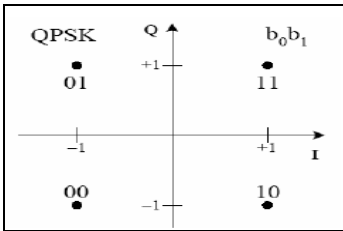


Fig. 4.3. QPSK Constellation Mapping

4.2 Working of 2x2 MIMO system

The 2x2 MIMO systems have different blocks like QPSK modulator, ideal channel, channel estimation block and QPSK demodulation. QPSK modulator takes the binary bits as input. Here the inputs bits are taken as symbols. For example 00, 01, 10, 11 are 4 inputs symbols for QPSK. The symbols are converted into complex values as shown in table 4.1. The complex output of the modulator is appended with the training sequence at 2 transmitters. Here the diversity technique is used to send the same data with different training sequences. The channel coefficients are multiplied with the modulated data. Here 4 paths are considered for 2x2 channels as shown in Fig.4.1.

The channel is an ideal channel i.e. the noise is not considered. The reliability is increased by employing the diversity technique i.e. transmitting the same information across multiple channels. The redundant data is transmitted so that the fading can be reduced. If one of the channel is not used or if the data is lost in space then the information/data can still be recovered from redundant transmission over the channels and hence the reliability of the communication system is improved.

The data transmitted from transmitter tx1 across the channels h11 and h12 and received by both the receiver’s rx1 and rx2. Here the use of the available channels is done to increase the capacity and reliability. Then the received sequence is taken into the channel estimation block to find the estimated channel coefficients. The received data from LS channel estimator block are the given to the decision block in the QPSK demodulator block to get back the sent binary sequence. The transmitted sequence is then checked with the received sequence at the QPSK modulator and the Demodulator block respectively.

5. Simulation results

This section mainly deals with the simulation and VLSI implementation of 2x2 MIMO systems. The results are analyzed and compared with the MATLAB values.

5.1 MATLAB simulation results

The specifications of MIMO system from MATLAB are shown below.

- 1. 2x2 MIMO Technique: 2 transmitters and 2 Receiver antennas
- 2. QPSK modulation technique
- 3. Number of bits transmitted 64bits
- 4. Number of iterations = 100
- 5. Signal to noise ratio SNR = [0:3:9] i.e. 0, 3, 6 , 9 in dB

QPSK modulated output is shown in Fig.5.1. Input binary data is sent through QPSK modulator, the data taken into is in the form of symbols. The in-phase and quadrature waveform and the QPSK modulated data are shown in Fig.5.1. The bit error rate with respect to signal to noise ratio, the error rate goes on reducing as shown in Fig.5.2 (a). The error rate goes on reducing from 10^0 to 10^{-1} as the SNR is increased from 0 to 10dB. As the number of iterations increases the error at the output which is given as the difference between the input and the output signal becomes as zero. The error plot is shown in Fig.5.2 (b) is for 100 iterations. There is a mismatch at 2 points and the difference is plotted. These plots as shown in Fig.5.2 are for LS channel estimation method. As the number of iterations

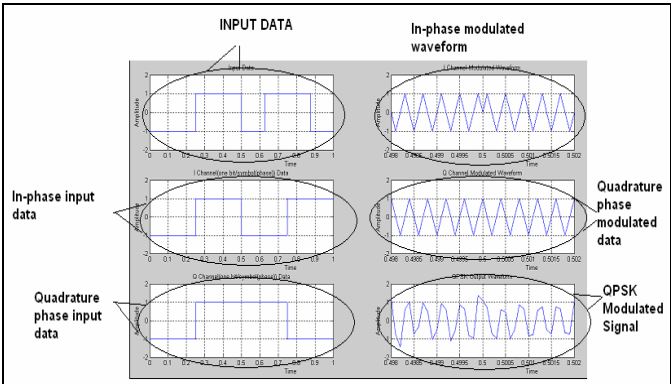


Fig. 5.1. QPSK modulator MATLAB outputs

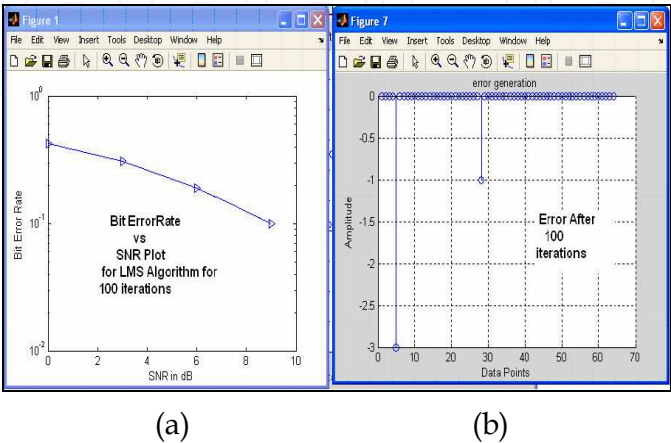


Fig. 5.2. BER vs SNR plot and Error generation after 100 iterations

increase the error reduces so that the BER vs SNR ratio goes on reducing and becomes negligible. Whenever there is a mismatch between the input and the output sequence of MIMO system then the difference is shown as the error.

The plots shown in Fig.5.3 are the input to a system is a random data generated using 'randn' in MATLAB. The random data generated is fed to the QPSK modulator. The data get modulated and then the modulated output is sent through the QPSK demodulator. The demodulated output same as input as shown in Fig.5.3. The plots as shown in Fig.5.3 are from MATLAB. Here the input is taken as 64 symbols.

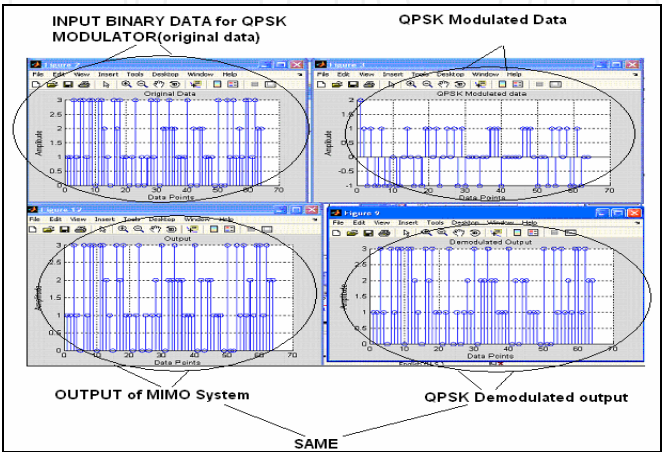


Fig. 5.3. The output of MIMO system and QPSK demodulated output

5.2 Modelsim simulation results

2x2 MIMO system is designed using Verilog-HDL and simulated in Modelsim. Each block is separately verified for its functionality. Each block is synthesized and the integrated output is also verified by implementing Xilinx FPGA. The top block of 2x2 MIMO system block diagram from Xilinx is shown in Fig.5.4. All the blocks in 2x2 MIMO system like QPSK modulator/demodulator, ideal channel and the LS channel estimation blocks are integrated and the connections are shown in Fig.5.4, with inputs and the outputs.

The output of integrated 2x2 MIMO system design is as shown in Fig.5.5. The waveform shows the 2x2 MIMO system output. Here the clock is applied and the reset is high then the

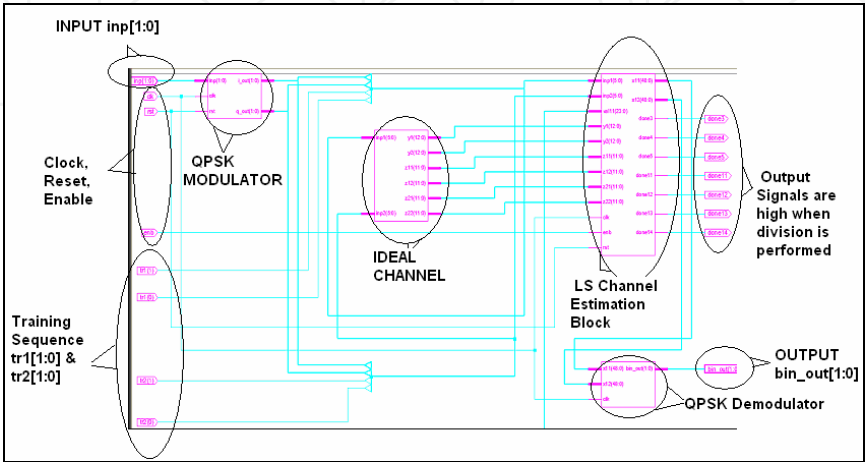


Fig. 5.4. 2x2 MIMO System in Xilinx

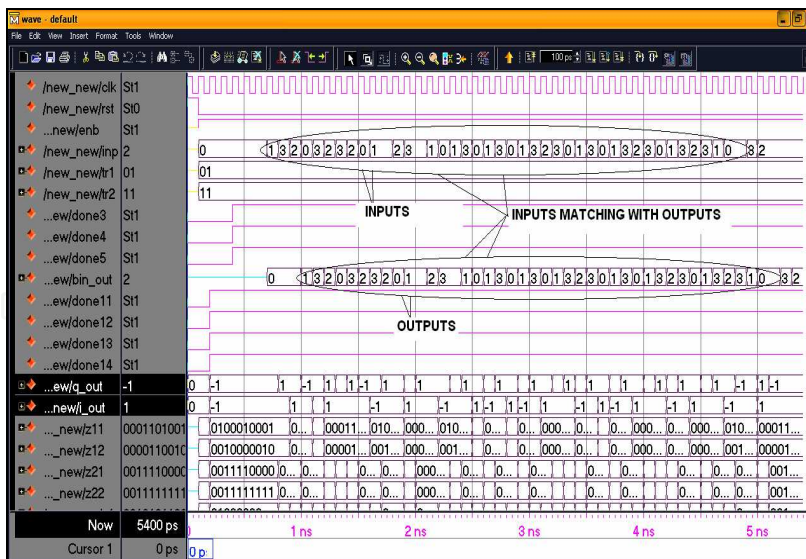


Fig. 5.5. The 2x2 MIMO System output

system is made reset. Then the reset signal is made low and the enable signal is made high. The inp[1:0] is the given the value as the required symbol to transmit. The training sequence tr1 is given as +1 and training sequence tr2 is given as -1. Then the output bin_out[1:0] is obtained as the input inp[1:0]. In Modelsim simulation the channel coefficients are represented 'z' in terms of 'h'.

5.3 VLSI implementation results

5.3.1 2x2 MIMO system

The design is implemented on Xilinx Virtex II-Pro board. The synthesis report is shown below.

Name of the device	Device utilization
Number of Slices	3999 out of 4928
Number of Slice Flip Flops	343 out of 9856
Number of 4 input LUTs	7603 out of 9856
Number of IOs	18
Number of bonded IOBs	18 out of 396
Number of MULT18X18s	11 out of 44
Number of GCLKs	1 out of 16

Table 5.1. Device utilization summary 2x2 MIMO system target device using 2vp7ff896-6

Timing parameters	Parameter values
Speed Grade	-6
Minimum period	137.548ns
Maximum Frequency	7.270MHz)
Minimum input arrival time before clock	39.872ns
Maximum output required time after clock	3.692ns
Maximum combinational path delay	No path found

Table 5.2. Timing Report of 2x2 MIMO systems

The device utilization report from Xilinx is shown above table 5.1. The timing report is shown below table 5.2 for the 2x2 MIMO system design. The device utilized is 2vp7ff896 with a speed grade of 6 and the slices taken are 3999 with a frequency of 7.2MHz.

5.3.2 QPSK modulator

The device utilization of QPSK modulator is shown in below table 5.3. It utilizes about 1 slice and its operating frequency is about 666.66MHz from DC. The timing report is shown table 5.4.

Name of the Device	Device utilization
Number of Slices	1 out of 4928
Number of Slice Flip Flops	4 out of 9856
Number of 4 input LUTs	2 out of 9856
Number of IOs	8
Number of bonded IOBs	8 out of 396
IOB Flip Flops	4
Number of GCLKs	1 out of 16

Table 5.3. Device utilization summary of QPSK Modulator using 2vp7ff896-6

Timing Parameter	Parameter values
Minimum input arrival time before clock	2.246ns
Maximum output required time after clock	3.615ns
Maximum combinational path delay	No path founds

Table 5.4. Timing Report of QPSK Modulator

5.3.2 Ideal channel

The device utilization of ideal channel is shown in below table 5.5. It utilizes about 10 slices and its operating frequency is about 400MHz from DC. This is a combinational block and hence has maximum combinational delay of 9.05ns. The timing report is shown table 5.6.

Name of the Device	Device utilization
Number of Slices	10 out of 4928
Number of 4 input LUTs	2 out of 9856
Number of IOs	86
Number of bonded IOBs	86 out of 396
Number of MULT18X18s	3 out of 44

Table 5.5. Device utilization summary of ideal channel using 2vp7ff896-6

Timing Parameter	Parameter values
Maximum combinational path delay	9.055ns

Table 5.6. Timing Report of ideal channel

The device utilization of LS Channel Estimation is shown in below table 5.7. It utilizes about 4321 slices and its operating frequency is about 37MHz from DC. The timing report is shown table 5.8.

Name of the Device	Device utilization
Number of Slices	4231 out of 4928
Number of Slice Flip Flops	509 out of 9856
Number of 4 input LUTs	7956 out of 9856
Number of IOs	218
Number of bonded IOBs	218 out of 396
IOB Flip Flops	4
Number of MULT18X18s	18 out of 44
Number of GCLKs	1 out of 16

Table 5.7. Device utilization summary of LS channel estimation using 2vp7ff896-6

Timing Parameter	Parameter values
Minimum period	142.444ns
Maximum Frequency	7.020MHz
Minimum input arrival time before clock	96.582ns
Maximum output required time after clock	9.734ns

Table 5.8. Timing Report of LS channel estimation

The device utilization of QPSK demodulator is shown in below table 5.9. It utilizes about 6 slices and its operating frequency is about 500MHz from DC. The timing report is shown table 5.10.

Name of the Device	Device utilization
Number of Slices	6 out of 4928
Number of 4 input LUTs	10 out of 9856
Number of IOs	101
Number of bonded IOBs	16 out of 396
IOB Flip Flops	2
Number of GCLKs	1 out of 16

Table 5.9. Device utilization summary of QPSK Demodulator

Timing Parameter	Parameter values
Minimum input arrival time before clock	3.708ns
Maximum output required time after clock	3.615ns

Table 5.10. Timing Report of QPSK Demodulator

The Table 5.11 shows the device utilization for each block in 2x2 MIMO systems.

5.4 Synthesis and timing verification of 2x2 MIMO system

The 2x2 MIMO system code is simulated in Modelsim and synthesized using Xilinx before giving to Design Compiler for timing analysis. Design compiler is tools which synthesize the design using the user given constraints, libraries and the RTL code. The clock to be specified as a constraint for which approximately the design work is determined using Xilinx. A clock of 50-60% from Xilinx is created for timing verification. Clock network delay or min latency of 25% of the clock, uncertainty for setup is given as 10% of the clock, for hold 5% of the

Block	QPSK Modulator	Ideal Channel	LS Channel Estimation	QPSK Demodulator	2x2 MIMO S/m	2x2 MIMO for 2vp30ff896 device
No.of Slices Out of 4928	1	10	4321	6	4231	1902 out of 13696
No.of FFs Out of 9856	4	-	509	-	343	273 out of 27392
No.of 4input LUT out of 9856	2	2	7956	10	7956	3595 out of 27392
No.of IOs Out of 39	8	86	218	101	18	27 out of 556
No. of Mux out of 44	-	3	18	-	11	8 out of 136
Frequency of operation in MHz	666	400	7	500	7.2	13

Table 5.11. Block wise Device utilization for 2x2 MIMO System

clock. An external delay is specified as 40-50% of clock specified. Then the compiled results are checked for the setup and hold violations i.e. the slack is met or not. If not met the constraints are again changed as per requirement. The design timing verification is checked again. The libraries used are cb13fs120_tsmc_max.db and cb13io320_tsmc_max.db. These libraries are set as link and target library.

Name of the Device	Value Before Ungrouping	Value After Ungrouping
Number of ports	18	18
Number of nets	170	27550
Number of cells	6	26251
Number of references	5	123
Combinational area	38888.750000	38888.750000
Non combinational area	1902.000000	1902.000000
Net Interconnect area	6541.367676	8807.866211
Total cell area	40790.750000	40790.750000
Total area	47332.117676	49598.616211

Table 5.12. Area report before and after Ungrouping

The total area is changed as the hierarchical design is ungrouped. The area is the constraint which is increased when the design is ungrouped. The area occupied before ungroup is 47332μm² and after ungroup the area is 49598μm². The area report is shown table 5.12. The power is the main constraint in any design. The power obtained from DC is the approximate value. The total dynamic power is the power consumption of the design which is 2.9289mW. Here there are 2 path groups and the timing is met. There is no violation before ungrouping. For setup and hold the timings are met before and after ungrouping. The power report is shown table 5.13.

Type of the Power	Before Ungrouping	After Ungrouping
Cell Internal Power	1.8290 mW	1.8093 mW
Net Switching Power	1.0680 mW	1.1196 mW
Total Dynamic Power	2.8970 mW	2.9289 mW
Cell Leakage Power	224.1040 uW	224.1024 uW

Table 5.13. Power report

Cell	Reference	Library	Area Attributes
U3	bufbd1	cb13fs120_tsmc_max	1.000000
U4	bufbd1	cb13fs120_tsmc_max	1.000000
cha_est1	channel_est	40617.250000	h,n
cv1	channel_virtual	126.250000	h
qd41	qpsk_demod5_1	16.000000	h, n
qmm1	qpskmoddd_1	129.250000	h, n
Total cells		40790.750000	

Table 5.14. The Cell report

The cell report table 5.14 shows the total number of cell in the 2x2 MIMO system i.e. 40790 cells. After all timing verifications the net list, ddc file and constraint file is saved to carry out the timing verification in PT. Then after PT static timing verification is carried out. In PT we get the exact timing report for both setup and hold.

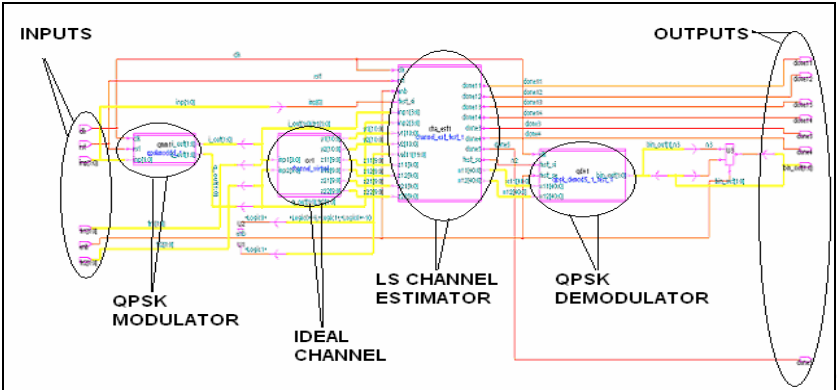


Fig. 5.6. The 2x2 MIMO system Schematic after DFT from DC

Parameters	Design Compiler	After Ungroup in DC	Primetime
Area	47332	49598	-
Maximum Timing	0.97	0.33	0.33
Minimum Timing	0	0.03	0.03
Dynamic Power	2.897mW	29289nW	-
Cell leakage power	224.10μW	224.1024 μW	-

Table 5.15. Area, Timing, Power Reports

The design for testability (DFT) is carried on 2x2 MIMO system. The Fig 5.6 shows schematic view of 2x2 MIMO system.The Table 5.15 shows the area, power and timing reports obtained from DC and PT for 2x2 MIMO system.

5.5 Physical design of 2x2 MIMO system

After synthesis, design is taken to the backend flow to tape out the design. This has inputs generated from the front end ASIC design flow. This involves the floor plan, power plan, timing setup, placement, clock tree synthesis, routing, design rule check, design for manufacturability and GDSII. The Fig.5.7 shows the physical design flow that is to be carried to tape-out the 2x2 MIMO systems.

Physical design flow is the back end flow in a chip design flow. Technology file (cb13_4m_tlu.tf) is a file to be specified when we create a design library. This consists of Layer Definitions, Via Definitions, Process Design Rules, TLU Parasitic capacitance models, Preferred routing directions and units.

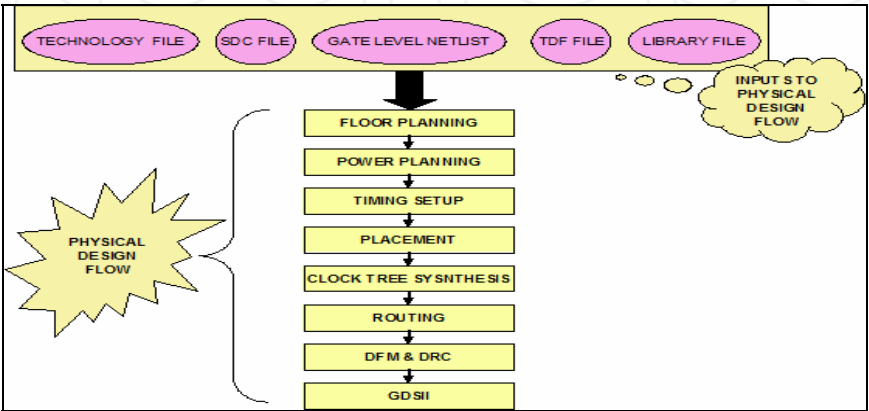


Fig. 5.7. Physical Design Flow

Design Libraries which utilizes the Synopsis database (Milky Way), which has .NETL specify the net views, .EXP specify expanded net list views, .CEL specify the cell views, .FRAM specify frame views and .TIM specify timing views. Gate-level net list consisting of inputs pads, output pads and their logical connectivity. SDC file consisting of the design constraints specified from Design compiler. The design is carried in Macro level. So TDF file is not required which consists of boundary and pads/pins information. Finally, the output of backend physical design flow is the routed net list, parasitic file and GDS. This GDS consists of static timing analysis, simulation, logic equivalence check, and physical verification for final verification. Here 0.13µm technology is used in Astro design flow. Astro is a physical design tool.

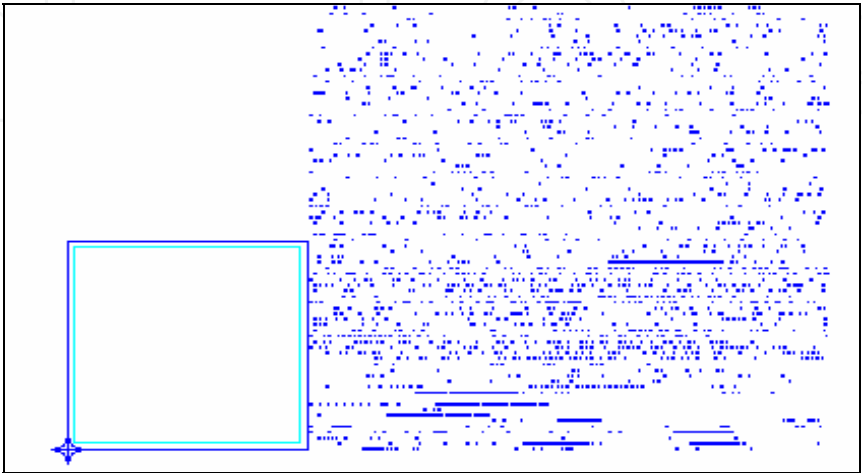


Fig. 5.8. Floor Planning of 2x2 MIMO System from Astro

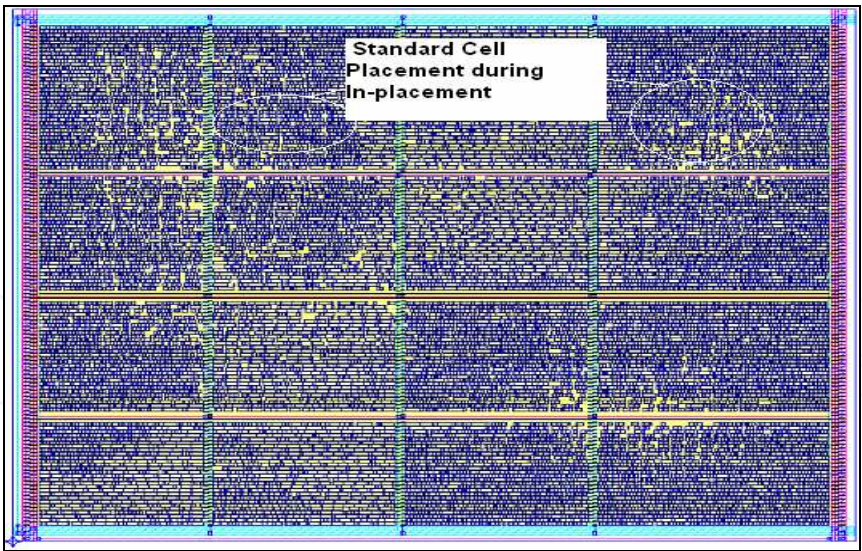


Fig. 5.9. Standard Cell Placement during In-Placement in Astro

Floor planning is first important step in back end design flow. The Fig.5.8 shows the floor planning of the design. To have a good IC to be developed, floor planning should be perfect. This phase consisting of planning and sizing of blocks and interconnects. Inputs of Floor-plan define different control parameters like aspect ratio, core utilization. Placement is the key step in physical design process. Poor placement consumes large areas hence performance gets reduced. Inputs to the placement are set of blocks, number of terminal for each block and net list. Main objectives of placement are to perform Standard cell placement, perform logic and placement optimization, to meet the timing depending on the placement and optimizing of the design and reducing congestion and crosstalk free placement. The Fig 5.9 shows the placement of cell during in-placement. Pre-placement optimization removes all wire load models effects to create a clean state. Perform zero wire load model optimization and logic remapping. This reduces the total cell area by gate downsizing and buffer remove which is introduced to remove the congestion i.e. collapsing high fan-out nets. Also meet the setup timing. The high fan-out buffers are first collapsed and then synthesized for quick placement as shown in Fig.5.10. Here the fan-outs considered are 20. Timing report is

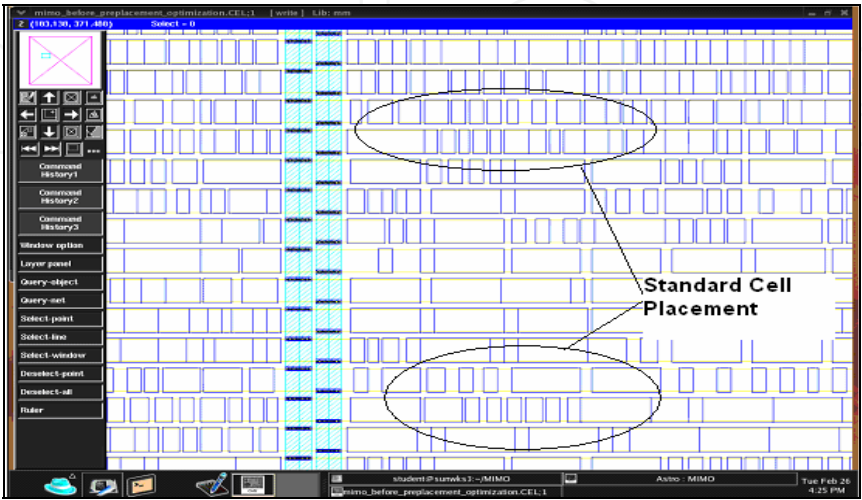


Fig. 5.10. Standard Cell Placement During Pre-Placement in Astro

checked for setup, hold, maximum capacitance, maximum fan-out and nets. The design is carried up to the placement of the cells. The clock tree synthesis and the routing is not carried for physical design. The DRC is also not checked for the design.

2x2 MIMO system results are explained in detail. The RTL code is synthesized implemented on Virtex2Pro Xilinx board. Then design timing verification is performed using DC and PT. The 2x2 MIMO system design is taken to physical design to tape-out.

6. Conclusion

The simple working of a MIMO system is carried till backend of the VLSI flow. The design is simulated in MATLAB to arrive at the specifications. The RTL code is successfully simulated in Modelsim. The design is synthesized and implemented on Virtex2Pro FPGA board. The synthesis and timing is verified and the timing is met for both setup and hold in DC and PT. DFT is also carried without timing violation. The top design takes about 3999 number of slices out of 4928 slices i.e. in Virtex2Pro the device selected is 2vp7ff896 at speed grade of 6 with operating frequency 7.27MHz and minimum period of 137.548ns. Timing verified is all met with positive slack with zero violations.

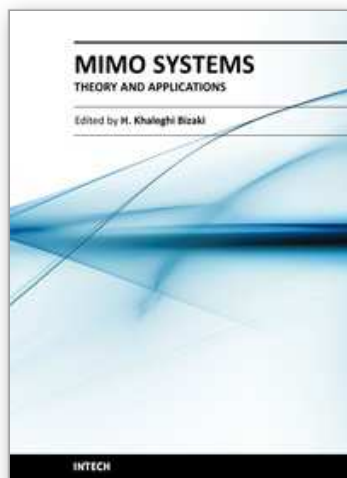
In the design the channel is considered to be ideal. In the future work the noise is to be added and the estimation of channel using different channel models is to be carried. Different channel estimation is to be simulated in MATLAB and then taken to the complete VLSI flow. The frequency of the design is to be optimized. The complete backend flow has to be completed till the tape-out of the design.

- Scope of the future work is to improve the design further for the noise to be included in the channel and use any improved matrix inversion technique for improving the design frequency of operation. This can be done using QRD algorithm.
- Iterative algorithm is applied for the design so as to reduce the effect of noise on data. The iterative algorithms like Recursive LS, Least Mean Square, MMSE, etc. Channel estimation and compensation for different channel models for delays is to be implemented.
- Fixed point implementation of the design is to be carried out by obtaining the floating-point values from MATLAB because the fixed-point representation will be more efficient.
- MIMO performance can be improved by using OFDM. By incorporating OFDM the performance of the overall system can be improved.

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In recent years, it was realized that the MIMO communication systems seems to be inevitable in accelerated evolution of high data rates applications due to their potential to dramatically increase the spectral efficiency and simultaneously sending individual information to the corresponding users in wireless systems. This book, intends to provide highlights of the current research topics in the field of MIMO system, to offer a snapshot of the recent advances and major issues faced today by the researchers in the MIMO related areas. The book is written by specialists working in universities and research centers all over the world to cover the fundamental principles and main advanced topics on high data rates wireless communications systems over MIMO channels. Moreover, the book has the advantage of providing a collection of applications that are completely independent and self-contained; thus, the interested reader can choose any chapter and skip to another without losing continuity.

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