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Design of Thin-Film Lateral SOI PIN Photodiodes with up to Tens of GHz Bandwidth

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1. Introduction

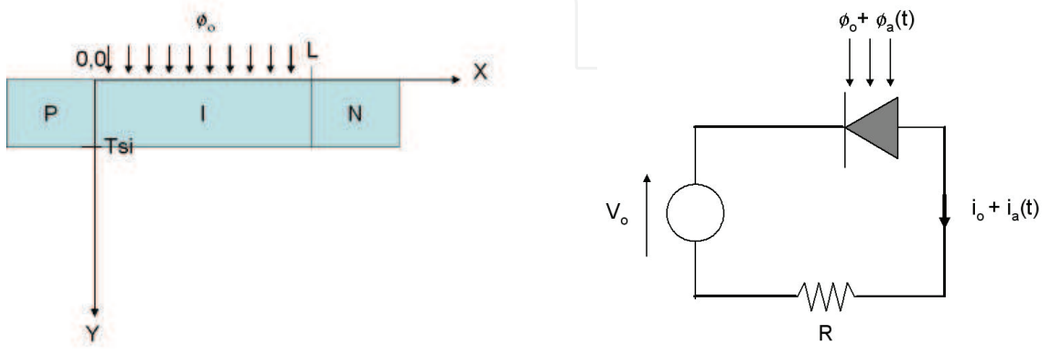
Short-distance optical communications and emerging optical storage (OS) systems increasingly require fast (i.e with Gigahertz to tens of Gigahertz bandwidth) and integrated Si photodetectors (Csutak et al., 2002; Hobenbild et al., 2003; Zimmermann, 2000). Thin-film SOI integrated devices appear as the best candidate to cope with these high-speed requirements, notably for the 10Gb/s Ethernet standard (Afzalian & Flandre, 2005; 2006.a; Csutak et al., 2002). For such bandwidths design trades-off between speed and responsivity are very severe and require a careful optimization (Afzalian & Flandre, 2006.b). In this context, accurate analytical modeling is very important for insight, rapid technology assessment for the given application, and/or rapid system design. There is however a lack of these accurate models in the literature so that time consuming devices simulations are often the only solution. In (Afzalian & Flandre, 2005), we have proposed such an accurate analytical model for the responsivity of thin-film SOI photodiodes. In here, thorough analytical modeling of AC performances of thin-film lateral SOI PIN photodiodes will be addressed. Speed performances depend on a trade-off between transit time of carriers and a RC constant related to the photodiode and readout circuit combined impedances. We will first focus on the transit time limitation of the thin-film SOI PIN diodes (section 2). Then, we will model the complex diode impedance using an equivalent lumped circuit (section 3). For a lateral SOI PIN photodiode indeed, the usual approximation of considering only the depletion capacitance, C_d, reveals insufficient. Our original model, fully validated by Atlas 2D numerical simulations and measurements, allows for predicting and optimizing SOI PIN detectors speed performances for the target applications in function of technological constraints, in particular their intrinsic length, L_i, which is their main design parameter.

2. Transit time limitation of thin-film SOI PIN diodes

To study the transit time limitation of thin-film SOI PIN diodes, we will elaborate an AC analytical model of a lateral PIN diode under illumination assuming full depletion of the intrinsic region. Applying the drift-diffusion set of equations to the SOI lateral photodiode structure and using a few realistic assumptions, we will calculate DC and AC currents using a perturbation model. From there, we will derive an expression of the transit time -3dB frequency. In a first stage we will neglect multiple reflections in computing the incident optical power. Next, we will generalize the model to take these effects into account. Results given

by the analytical model will also be compared to results of numerical simulations and we will derive an expression to calculate the transit time -3dB frequency when the intrinsic length is only partially depleted. Substrate generated charge effects on the transit time frequency will further be investigated and discussed for the first time. These effects are totally neglected in the literature and related to partial AC isolation of the BOX. Specific solutions to this problem adapted to the SOI structure will be proposed.

2.1 General equations



(a) General structure of the lateral PIN photodiode

(b) Equivalent scheme of the PIN diode and the external polarization circuit

Fig. 1

a) We first quickly review the general semiconductors equations applied to the particular geometry of lateral PIN diodes (Fig. 1.a). The photodiode is composed of a lowly doped (intrinsic) Si region of length L_i, sandwiched between two highly P+ and N+ doped regions. The Si film of thickness *tsi* is very thin, (typically a few tens to a few hundred of nm). The width of the device is supposed very thick and invariant by translation such that a 2D model is used. The following system is to be solved inside the device (Sze, 1981):

$$\begin{aligned} \frac{\partial E_x(x,y,t)}{\partial x} + \frac{\partial E_y(x,y,t)}{\partial y} &= -\frac{q}{\varepsilon_s}.(p(x,y,t) - n(x,y,t) + \tau(x)) \\ \frac{\partial n(x,y,t)}{\partial t} &= \frac{1}{q}\nabla.\overline{J_n} + G - R \\ \frac{\partial p(x,y,t)}{\partial t} &= -\frac{1}{q}\nabla.\overline{J_p} + G - R \end{aligned} \tag{1}$$

In system (1), x is the lateral direction while y is the vertical direction; E is the electric field, q the electron charge, n and p the concentrations of free carriers (electrons and holes resp.) in the device, τ is the doping profile obtained as the difference between the positive N_d and the negative N_a fixed charges $N_d(x) - N_a(x)$ and has been assumed to be a function of x only. G and R are the generation and recombination terms, respectively. Since the concentration of dopant impurities is very low compared to the concentration of Si atoms in the Si crystal, the probability of indirect recombination or generation is very low. Therefore we only consider band-to-band mechanisms and G and R are the same for electrons and holes. J_n and J_p

are the current densities of electrons and holes respectively and are given for a device with homogenous temperature by the drift-diffusion equation (Sze, 1981):

$$\begin{aligned} J_n &= qn\mu_n E + qD_n \nabla n \\ J_p &= qp\mu_p E - qD_n \nabla p \end{aligned} \tag{2}$$

In the right part of equations (2), the first terms are the drift current densities due to the electric field, while the second are related to diffusion. μ_n and μ_p are the mobilities, and D_n and D_p are the well-known diffusion coefficients of the electrons and holes respectively. They are related through the Einstein relationship:

$$D_n = \mu_n \frac{kT}{q} \quad D_p = \mu_p \frac{kT}{q} \tag{3}$$

where k is the Boltzmann constant while T is the absolute temperature of the device. For the mobility, we can consider the electric field dependent model of (Caughey& Thomas, 1967):

$$\mu_n(|E|) = \mu_{no}. \left[\frac{1}{1 + (\frac{\mu_{no}.|E|}{v_{sat}})^2} \right]^2 \tag{4}$$

$$\mu_p(|E|) = \mu_{po}. \frac{1}{1 + (\frac{\mu_{po}.|E|}{v_{sat}})} \tag{5}$$

$$v_{sat} = \frac{2.4 * 10^7}{1 + 0.8 * e^{(\frac{T}{600})}} [cm/s] \tag{6}$$

where $|E|$ is the norm of the lateral electric field and μ_{no} and μ_{po} are the low field electron and holes mobilities respectively. These are strongly influenced by impurity concentration and temperature (Zimmermann, 2000). v_{sat} is the saturation velocity.
b) The illumination is supposed to be uniform over the I-layer($\phi_o(t)$) and zero outside. So the generation term in this layer is only a function of the depth y and the time t and is given by:

$$G(y,t) = \alpha \phi_o(t) e^{-\alpha y} \tag{7}$$

where $\phi_o(t)$ is the number of efficient photons by cm^2 impinging on the device. We can relate it to the illumination power by unit of Area W_{ph} by:

$$\phi_o(t) = W_{ph}(t,\lambda). \frac{\lambda}{hc}. \eta_i \tag{8}$$

where λ is the wavelength of the incident light, h is the Planck constant, c is the speed of light in the vacuum and η_i is the internal quantum efficiency, i.e. the probability that an absorbed photon gives rise to an electron-hole pair.

2.2 Simplifying assumptions in lateral fully depleted thin-film diodes

The system to solve is a two-dimensional problem. However, as we shall see, it can be simplified to a 1D one by using a few realistic assumptions.

1) We will assume the electric field to be constant *vs.* the x-position inside the depletion region as τ is very small compared to its value in the P^+ and N^+ regions and the carrier concentrations are very low: the intrinsic region is supposed to be depleted and the influence of photogenerated carriers on the electric field profile in this absorbing layer can be neglected as they are rapidly swept out by the field.

2) In reverse or low forward bias regime in which the photodiode is biased, diffusion currents are neglected within the intrinsic layer as they are very small with respect to the drift photo-generated currents. Equation (2) simplifies to:

$$J_n = qn\mu_n E \quad J_p = qp\mu_p E \tag{9}$$

3) Charge trapping is neglected at the interface. It is equivalent to say that surface recombination velocities at front ($y = 0$) and back interfaces ($y = t_{si}$) are zero.

4) Only light generation is taken into account. Thermal generation indeed determines dark current, which is very small and of no interest here.

As said earlier, under normal reverse bias condition for the photodiode, the intrinsic region is completely depleted. Only photogenerated carriers have therefore to be accounted for and recombination can be neglected. This is valid as long as the illumination is low, i.e. (Torrese, 2002):

$$\phi_o < min(\mu_p, \mu_n) E.ni \tag{10}$$

However, if the illumination is too strong, recombination will increase and a saturation effect will appear.

Because of hypothesis 3), we can assume current densities only following the x-axis. No current is flowing in the y direction. Because of hypothesis 2), neglecting diffusion currents in the I-layer, this, in turn, implies the electric field to be aligned to the x-axis, too.

We therefore obtain a decoupled problem in the intrinsic layer where the photogeneration takes place: electric field and current density follow the x-axis, while, the generation term is only a function of y. Consequently, the set of equations 1 becomes:

$$\begin{aligned} E(t) &= E_x(t)\hat{a}_x \\ \frac{\partial n(x,y,t)}{\partial t} &= \frac{1}{q}\frac{\partial J_n(x,t)}{\partial x} + G(y) \\ \frac{\partial p(x,y,t)}{\partial t} &= -\frac{1}{q}\frac{\partial J_p(x,t)}{\partial x} + G(y) \end{aligned} \tag{11}$$

2.3 Perturbation model

In order to linearize the transport equations and study the small-signal frequency response of the diode to an optical flux, we will assume that the illumination signal is the sum of a DC time-averaged part and an AC or time-dependent part, small compared to the DC part and use perturbation theory. Expanding equations to the first order, we obtain a system of linear equations. Assuming the AC input signal to be a complex sinusoidal perturbation of infinitesimal amplitude, at only one frequency ω, we know by linear system theory that all

other signals will also be complex sinusoidal at frequency ω, i.e. any variables $\psi(x,y,t)$ can be expanded in the form of a dc and ac part:

$$\psi(x,y,t) = \psi_o(x,y) + \psi_a(x,y)e^{j\omega t} \tag{12}$$

where ω is the angular frequency of the modulation.
Note that for the mobilities, we have considered a field dependent model. Since the field is function of time, mobilities will also be function of time. Using a quasi-static model for the mobilities, we find:

$$\begin{aligned} \mu_{p,n}(t) &= \mu_{po,no} + \mu_{pa,na}e^{j\omega t} \\ \mu_{po,no} = \mu_{p,n}(E_o) \qquad \mu_{pa,na} &= \frac{d\mu_{p,n}}{dE}|_{E=(E_o)}.E_a \end{aligned} \tag{13}$$

Combining all together back in equations 11, we can separate these into two distinct sets. One is time-independent, yielding the DC work point, while the other is time-dependent.
The DC set of equations within the depletion region is:

$$\begin{aligned} \overrightarrow{E_o} &= E_o\hat{a}_x \\ (\frac{\partial n_o(x,y)}{\partial x}).\mu_{no}E_o + G_o(y) &= 0 \\ (\frac{\partial p_o(x,y)}{\partial x}).\mu_{po}E_o - G_o(y) &= 0 \end{aligned} \tag{14}$$

while when keeping only the linear terms (small-signal approximation), the AC-system becomes:

$$\begin{aligned} \overrightarrow{E_a} &= E_a\hat{a}_x \\ -(\frac{\partial n_a(x,y)}{\partial x}).\mu_{no}E_o + j\omega n_a(x,y) &= G_a(y) - G_o(y)(\frac{\mu_{na}}{\mu_{no}} + \frac{E_a}{E_o}) \\ (\frac{\partial p_a(x,y)}{\partial x}).\mu_{po}E_o + j\omega p_a(x,y) &= G_a(y) - G_o(y)(\frac{\mu_{pa}}{\mu_{po}} + \frac{E_a}{E_o}) \end{aligned} \tag{15}$$

where generation terms are given by:

$$G_o(y) = \alpha\phi_o e^{-\alpha y} \quad G_a(y) = \alpha\phi_a e^{-\alpha y} \tag{16}$$

2.4 Calculation of the free carriers concentrations

In order to solve this double system of equations we need 2 boundary conditions for each system for the free carriers concentrations. The simplest and quite well accepted conditions in the literature (Torrese, 2002) are to neglect the minority carriers at the edges of the P and N regions (i.e. neglecting diffusion (dark) current. In order to analytically predict the dark current, a third set of equation without generation, but with diffusion and recombination in the intrinsic layer and with the Maxwell-Boltzman boundary conditions can be used (Afzalian & Flandre, 2005)):

$$p_o(L_i) = n_o(0) = 0 \quad p_a(L_i) = n_a(0) = 0 \tag{17}$$

Solving the DC system, we find the following solutions for the free carriers concentrations:

$$n_o = -\frac{\alpha\phi_o e^{-\alpha y}}{\mu_{no}E_o}x \quad p_o = -\frac{\alpha\phi_o e^{-\alpha y}}{\mu_{po}E_o}(L_i - x) \tag{18}$$

The negative sign can surprise at first glance but in fact, the diode being reverse biased, the Electric field is negative (see below). Thus carrier concentrations remain positive everywhere. The negative sign will however imply a negative current, i.e. flowing opposite to the x-axis, as can be expected.
Solving the AC system, we derive:

$$\begin{aligned} n_a(x,y,\omega) &= \frac{G_a(y) - G_o(y)(\frac{\mu_{na}}{\mu_{no}} + \frac{E_a}{E_o})}{j\omega}.(1 - e^{\frac{j\omega}{\mu_{no}E_o}x}) \\ p_a(x,y,\omega) &= \frac{G_a(y) - G_o(y)(\frac{\mu_{pa}}{\mu_{po}} + \frac{E_a}{E_o})}{j\omega}.(1 - e^{\frac{(L_i-x)}{\mu_{po}E_o}}) \end{aligned} \tag{19}$$

2.5 Current

From DC and first order AC carriers concentration analytical expressions, expressions for current densities can be derived. From there, currents themselves can be obtained.
The total density of conduction current across the device is the sum of electron density current J_n, hole density current J_p and displacement current density J_d:

$$J = J_n + J_p + J_d \tag{20}$$

The displacement component is proportional to the time variation of the electric field:

$$J_d = \varepsilon_s \frac{\partial}{\partial t}E(x,t) = -\frac{1}{S}C_j\frac{\partial}{\partial t}V_j(x,t) \tag{21}$$

where C_j is the junction capacitance, S its area, and V_j the potential across the junction. The displacement density current is time-dependent and is only significant during transients and at high frequencies (Torrese, 2002). By introducing the perturbation in the continuity equations (9) and then using expressions (18), we get the O^{th}-order (DC) current. As can be expected, the current density is independent of x:

$$J_o(x,y) = qE_o(n_o(x,y)\mu_{no} + p_o(x,y)\mu_{po}) = -q.L_i\alpha\phi_o e^{-\alpha y} \tag{22}$$

Similarly, but using (19) instead of (18), we get the total 1^{st}-order current density expression:

$$\begin{aligned} J_a(x,y,\omega) &= q[\frac{J_o(x,y).E_a}{qE_o} + E_o(n_a(x,y)\mu_{no} + n_o(x,y)\mu_{na} + p_a(x,y)\mu_{po} + p_o(x,y)\mu_{pa})] + j\omega\varepsilon_s E_a \\ &= j\omega\varepsilon_s E_a + q\alpha e^{-\alpha y}[-\frac{L_i\phi_o E_a}{E_o} + \frac{E_o}{j\omega}.\langle\mu_{no}.\{\phi_a - \phi_o(\frac{\mu_{na}}{\mu_{no}} + \frac{E_a}{E_o})\}.(1 - e^{\frac{j\omega}{\mu_{no}E_o}x}) \\ &+ \mu_{po}.\{\phi_a - \phi_o(\frac{\mu_{pa}}{\mu_{po}} + \frac{E_a}{E_o})\}.(1 - e^{\frac{j\omega}{\mu_{po}E_o}(L_i-x)})\rangle + \phi_o\{\frac{\mu_{na}}{\mu_{no}}x + \frac{\mu_{pa}}{\mu_{po}}(L_i - x)\}] \end{aligned} \tag{23}$$

The DC electric field in the I-part of the diode is due to the external applied voltage, V_{ext} and to the internal P^+N^+ contact potential, ϕ_{PN}. The AC electric field is simply due to the variation of the potential related to the AC photocurrent through the resistor R. According to figure 6.b, we have:

$$V_{ext} = V_o + Ri_o \quad \phi_{PN} = U_t.ln(\frac{N_a.N_d}{n_i^2})$$
$$-\int_O^{L_i} E_o(x)dx = V_{ext} + \phi_{PN} \quad -\int_O^{L_i} E_a(x)dx = Ri_a \tag{24}$$

R is the total equivalent series resistance seen by the diode and can include contributions from diffusion zones, contacts, bias circuit source and the input resistance of the optical circuit front-end stage.
The direction of the positive current has been drawn in order to be related to the sign used in the equations.
E_o is in fact constant in the depleted I region only if $\tau = 0$. In practice this is never the case ($\tau = -N_{a_I} \approx 10^{15} cm^{-3}$, the residual I-doping) and the electric field has a linear profile. In this case, we can use a mean value for E_o given by:

$$E_{o_{cat}} = -\frac{V_{ext} + \phi_{PN}}{L_i} \quad E_o = E_{o_{cat}} + \frac{q.N_{a_I}}{\epsilon_{si}}.\frac{L_i}{2} \tag{25}$$

The DC and AC photo-currents of the device by unit of width (along the Z axis) are obtained by integrating the densities of current along the y-axis and taking them at the limit of the depletion area ($x = 0$ or $x = L_i$):

$$I_o(x) = \int_0^{t_{si}} J_o(x,y)dy \quad i_a(x,\omega) = \int_0^{t_{si}} J_a(x,y)dy \tag{26}$$

Performing the integration we find:

$$I_o(x) = I_o = -q.L_i\phi_o(1 - e^{-\alpha t_{si}}) \tag{27}$$

$$i_a(x,\omega) = j\omega\varepsilon_s E_a.t_{si} + q(1 - e^{-\alpha t_{si}})[-\frac{L_i\phi_o E_a}{E_o} + \frac{E_o}{j\omega}.\langle\mu_{no}.\{\phi_a - \phi_o(\frac{\mu_{na}}{\mu_{no}} + \frac{E_a}{E_o})\}.(1 - e^{\frac{j\omega}{\mu_{no}E_o}x})$$
$$+\mu_{po}.\{\phi_a - \phi_o(\frac{\mu_{pa}}{\mu_{po}} + \frac{E_a}{E_o})\}.(1 - e^{\frac{j\omega}{\mu_{po}E_o}(L_i - x)})\rangle + \phi_o\{\frac{\mu_{na}}{\mu_{no}}x + \frac{\mu_{pa}}{\mu_{po}}(L_i - x)\}] \tag{28}$$

DC photocurrent, I_o, and static electric field E_o are not related and can be calculated directly using Eq. (27), and Eq. (24). To calculate i_a an iterative method seems best suited, as it depends on E_a, which itself depends on i_a Eq. (24). Starting from E_a equal zero, which also implies the terms describing small-signal mobility equal to zero, we get the small signal photocurrent term directly generated by the variation of flux:

$$i_{ao}(x,\omega) = qE_o\frac{\phi_a}{j\omega}(1 - e^{-\alpha t_{si}})[\mu_{no}(1 - e^{\frac{j\omega}{\mu_{no}E_o}x}) + \mu_{po}(1 - e^{\frac{j\omega}{\mu_{po}E_o}(L_i - x)})] \tag{29}$$

Note that for low frequencies, i.e. frequencies such that the first order expansion of the exponential function is valid, we have a similar expression that for the dc photocurrent:

$$i_{ao_{lf}}(j\omega) = -q\phi_a(1 - e^{-\alpha t_{si}})L_i \quad \omega < \frac{\mu_{po}|E_o|}{L_i} \tag{30}$$

We then calculate the related variation of electric field:

$$E_{ao} = -\frac{R.i_{ao}}{L_i} \tag{31}$$

and iterate this process in Eq. (28) until the required precision is reached. Note that if the equivalent series resistor, R, is very low (ideally zero) equation (29) yields the solution directly without the need for iterative calculations.
Expression (30) also allows us to generalize our model to take into account the multiple reflections in the film by relating AC to DC photocurrent (for wich we have already developped such a model (Afzalian & Flandre, 2005)). Knowing dc photocurrent and modulation ratio k_m between ϕ_0 and ϕ_a, we write:

$$\begin{aligned} i_{ao_{lf}}(j\omega) &= \frac{phi_a}{phi_o}.I_o = k_m.I_o \\ i_{ao}(x,\omega) &= -\frac{i_{ao_{lf}}}{j\omega}.\frac{E_o}{L_i}[\mu_{no}(1 - e^{\frac{j\omega}{\mu_{no}E_o}x}) + \mu_{po}(1 - e^{\frac{j\omega}{\mu_{po}E_o}(L_i - x)})] \end{aligned} \tag{32}$$

We can then rewrite (28) using equation (29) and equation (27):

$$\begin{aligned} i_a(x,\omega) = j\omega\varepsilon_s E_a.L_i.t_{si} + i_{ao}(x,\omega) + i_o.\{\frac{E_a}{E_o} + (\frac{\mu_{na}}{\mu_{no}} + \frac{E_a}{E_o}).\frac{1 - e^{\frac{j\omega}{\mu_{no}E_o}x}}{\frac{j\omega}{\mu_{no}E_o}L_i} \\ + (\frac{\mu_{pa}}{\mu_{po}} + \frac{E_a}{E_o}).\frac{(1 - e^{\frac{j\omega}{\mu_{po}E_o}(L_i - x)})}{\frac{j\omega}{\mu_{po}E_o}L_i} - \frac{1}{L_i}[\frac{\mu_{pa}}{\mu_{po}}(L_i - x) + \frac{\mu_{na}}{\mu_{no}}x]\} \end{aligned} \tag{33}$$

We have implemented the model on Matlab. We first observed that in Si, with typical value of L_i on the order of μm and illumination power densities of a few mW/cm^2, electric field and mobilities variations only make i_a starting to differ from i_{ao} with huge load resistor values, typically larger than about $1M\Omega$. In this case, however, the frequency response of the detector will be limited by its RC constant, such that in most practical case in Si the calculation of i_{ao} is sufficient to model the transit time behaviour of the lateral PIN diodes.

2.6 Transition frequency

We will now extract a simple analytical expression of the -3dB transition frequency, f_{tr}, from the expression of i_{ao} for $x = L_i$ (cathode electron current). By definition of f_{tr}, we have:

$$\|i_{ao}(j\omega_o)\| = \frac{1}{\sqrt{2}}\|i_{ao_{lf}}\| \quad \omega_o = 2.\pi.f_{tr} \tag{34}$$

For $x = L_i$, expression (32) simplifies to an electron current only:

$$i_{ao}(L_i,\omega) = -\frac{i_{ao_{lf}}}{j\omega}.\frac{\mu_{no}E_o}{L_i}.(1-e^{\frac{j\omega}{\mu_{no}E_o}L_i}) \tag{35}$$

Injecting equation (35) into eq. (34), we have:

$$\| -\frac{\mu_{no}E_o}{L_i}\frac{1-cos(\frac{L_i}{\mu_{no}E_o}.\omega_o)-j.sin(\frac{L_i}{\mu_{no}E_o}.\omega_o)}{j\omega_o}\| = \frac{1}{\sqrt{2}} \tag{36}$$

which yields:

$$\omega_o = \frac{\mu_{no}E_o}{L_i}.\sqrt{4.[1-cos(\frac{L_i}{\mu_{no}E_o}.\omega_o)]} \tag{37}$$

Because the cosine function has a value which range between -1 and 1, we can note:

$$\omega_o = k.\frac{\mu_{no}E_o}{L_i} \quad 0 \leq k \leq 2.\sqrt{2} \tag{38}$$

and solve (38) for:

$$k = \sqrt{4.[1-cos(k)]} = 2.78 \tag{39}$$

$$f_{tr_n} = f_{tr}(x = L_i) = \frac{k}{2.\pi}.\frac{\mu_{no}E_o}{L_i} \tag{40}$$

We get good agreement when comparing cathode model (eq. (39)) to simulations of both anode and cathode currents as long as the intrinsic length is laterally depleted (i.e. for intrinsic length shorter than about $2\mu m$). Otherwise, carrier diffusion has to be taken into account.

2.7 Carrier diffusion

In our model, we have assumed that the photodiode was laterally depleted, i.e. $L_i < L_{zd}$ and the transit time limit was due to fast drift. L_{zd} is the depletion length and is related to doping and bias voltage (Sze, 1981) The related -3dB frequency, f_{tr}, decreases as L_i^2. However, if L_i becomes greater than L_{zd}, around $2\mu m$ for P_- doping and low voltage operation of actual processes, carriers transit is dominated by a slower diffusion mechanism and the related -3dB frequency, f_{tr}, decreases faster with L_i. On fig. 2, this f_{tr} reduction is observed on the Atlas simulation curve for L_i greater than $2\mu m$, when compared to the fast drift modeled curve that assumes full depletion of the I-region.

In order to estimate the time t_{diff} for the diffusion of electrons through a P region of thickness $L = L_i - L_{zd}$, we can use the equation derived for a time-dependent sinusoidal electron density due to photogeneration in the P layer from the electron diffusion equation (Sarto& Zeghbroeck, 1997; Zimmermann, 2000) and, from there, derive the related -3dB frequency, f_{diff}:

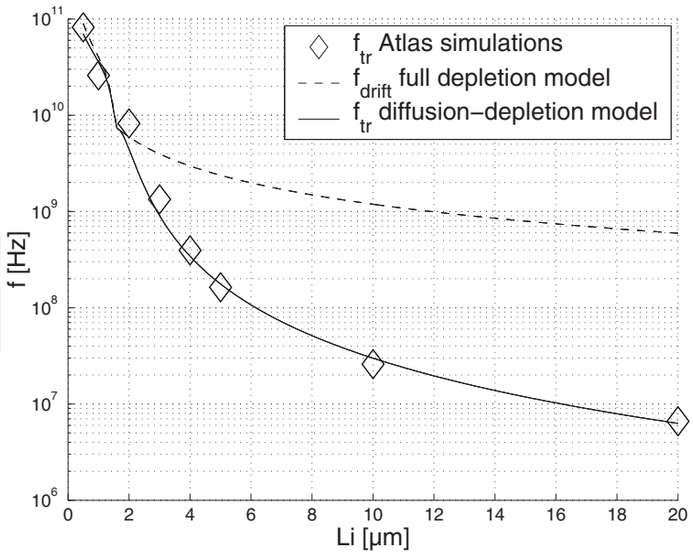


Fig. 2. Comparison of the PIN diode transition frequency given by Atlas simulations, by our model assuming drift only (full depletion hypothesis)(eq. 39), and by our model assuming both drift and diffusion mechanism (eq. 42).

$$t_{diff} = \frac{q.L^2}{2\mu_n.k_B.T} \quad f_{diff} = \frac{k_{diff}}{2\pi.t_{diff}} \tag{41}$$

where k_{diff} is a fitting coefficient.
The -3dB frequency related to the total transit time (drift+diffusion) is then obtained as:

$$f_{tr_{dd}} = (\frac{1}{f_{tr}} + \frac{1}{f_{diff}})^{-1} \tag{42}$$

A value of 2 was obtained for the coefficient k_{diff} by fitting model to numerical simulations (fig. 2).

2.8 Influence of the substrate

Until now in our modeling and numerical simulations we have ignored the effect of the substrate, assuming a perfect or ideal isolation through the buried oxide between the thin-Si film and the Si substrate. This assumption is used in the literature, where it is said that in SOI, unlike in Bulk Si, owing to the BOX, we can avoid the slow vertical diffusion of carriers generated under the depletion region in the substrate.
From an AC point of view, however, the BOX is a capacitor so that at high frequency, carriers photogenerated in the substrate could be mirrored at the front electrodes. In order to investigate this effect we have performed 2D-numerical Atlas simulations of the whole PIN structure, including a $500\mu m$-thick substrate. In current SOI submicron processes, two substrate doping concentrations are most often used. One of them is highly resistive (hr) and has a low substrate P-doping of around $2.10^{12}/cm^3$. The other, the standard resistivity (sr), is P-doped at around $1.10^{15}/cm^3$.
To get an idea of the insulation the BOX can provide we first compare AC photocurrents of a thin-film lateral PIN diode without substrate (SOI ideal case), with a 400nm buried oxide

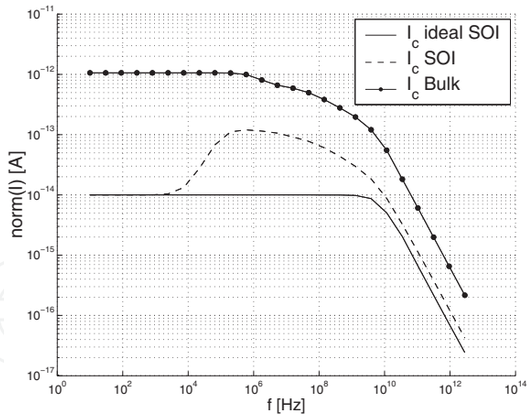
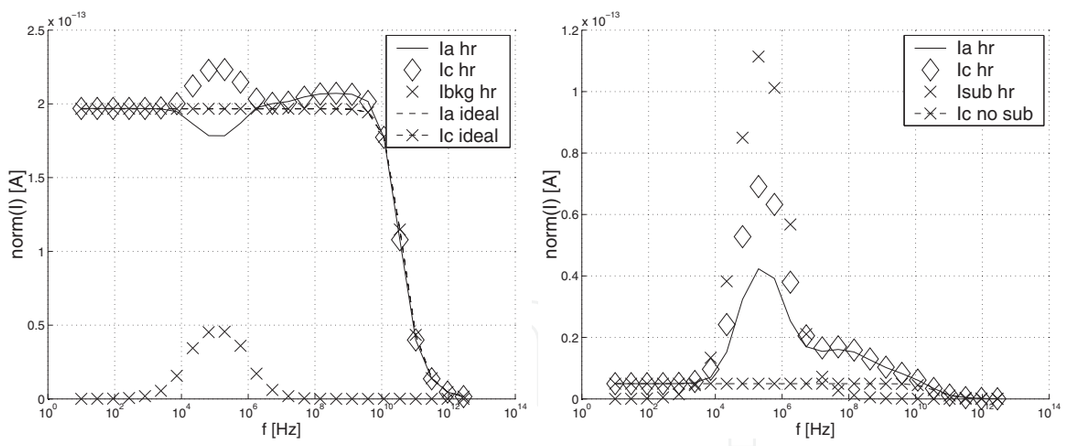


Fig. 3. Comparison of the currents vs. frequency of the PIN diode without substrate (ideal SOI case), with $500\mu m$ thick high resistivity substrate (SOI case) and with with $500\mu m$ thick high resistivity substrate but without a BOX ("Bulk" case) given by Atlas simulations. $L_i = 2\mu m$, $\lambda = 800nm$, P_{in} dc=$1mW/cm^2$ ac=$0.1mW/cm^2$, t_{si}=80nm.

and a $500\mu m$ hr Si-substrate (SOI case), and with a $500\mu m$ hr Si-substrate but without a buried oxide ("Bulk" case) obtained by numerical simulations (fig. 3). For frequency above a few kHz the BOX does not provide perfect insulation. The worst attenuation factor compared to the bulk case is about a factor 10 in the MHz range. This factor of attenuation, which may be sufficient for practical isolation of thicker SOI materials (t_{si} of few μms) with higher quantum efficiency, seems insufficient for insulating thin film SOI diodes in near IR wavelengths, where their quantum efficiency is only of a few percents.



(a) $\lambda = 400nm$ (b) $\lambda = 800nm$

Fig. 4. Comparison of the currents vs. frequency of the PIN diode with hr substrate and without substrate (ideal case) given by Atlas simulations. $L_i = 1\mu m$, P_{in} dc=$1mW/cm^2$ ac=$0.1mW/cm^2$

When comparing now AC simulations of PIN diodes with and without substrate, we see that at low frequencies, there is no difference (see fig. 4). The BOX isolates the active thin-film part of the diodes from the charges photogenerated in the substrate by the modulated light source. At higher frequency however, the BOX appears more and more like a short and

a capacitive photocurrent originating from the substrate (I_{bkg}) can reach the thin-film. The anode (I_a) and cathode (I_c) currents are influenced by the substrate photogenerated charges. Although this can increase the amplitude of the output photocurrent, this extra photocurrent is a slow diffusive current which will degrade the speed performances of the diodes. At still higher frequency, the number of substrate photogenerated charges that can follow the ac light source signal and diffuse to the thin film on time decreases. This is the cut-off frequency of the substrate generated charges and anode and cathode currents decrease toward the values of the ideal diode case.

The importance of the substrate photogenerated charges depends of course of the wavelength. For wavelength shorter than around 400 nm (see fig. 4.a), this influence can be neglected as most of the light is absorbed in the thin-film region. For higher wavelength (see fig. 4.b), importance of substrate generated charges compared to thin-film generated carriers increases. Simulations show that at a wavelength of 800 nm, the frequency response is strongly influenced.

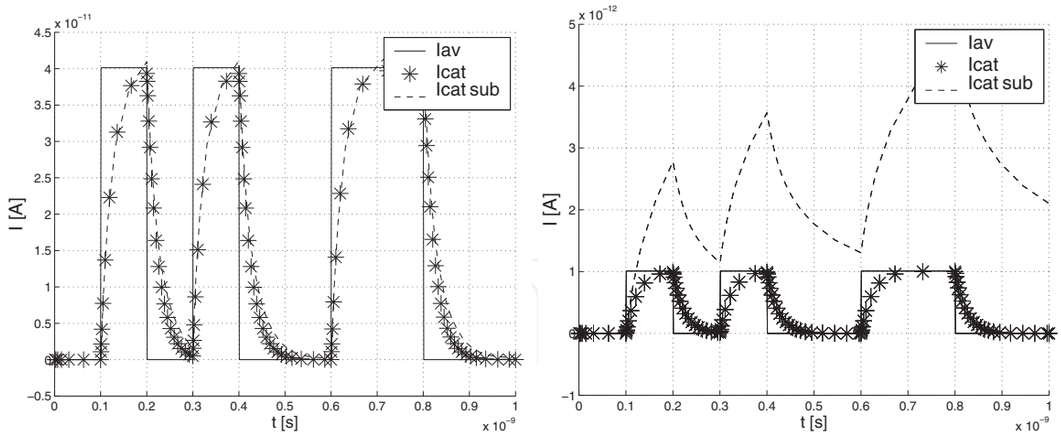
The peak value and frequency location of the backgate current are influenced by the substrate resistivity. For hr substrate the peak is higher and at a lower frequency which seems worse for high speed application. We explain this as if charges generated in the substrate see two paths to the ground: one impedance through the substrate to the backgate and one impedance through the BOX to the front electrodes. If the resistive impedance through the substrate is lower (sr substrate), the frequency at which the charges can cross the BOX will be higher. The appearance of the backgate current at mid frequency can then be explained by assuming that holes generated in the substrate see a higher impedance through the anode than that electrons undergoes through the cathode, so that the frequency at which holes will flow through the thin-film is higher.

In order to quantify the influence of the substrate photogenerated charges on the temporal response of the SOI photodiodes, we have simulated transient response of PIN diodes with and without substrate for an intrinsic length of $2\mu m$. From our model, these diodes should exibit a transit time frequency of a little less than 10 GHz and then to be available for 10 GBps optical data communication (which is the actual challenge for Si based optical communication).

If the ideal diode shows sufficiently fast temporal behaviour both at 400 and 800nm wavelengths for data train of 0.1 ns (fig. 5.a and 5.b), we can see that the diode with substrate can only be used at short wavelengths, for example 400nm. At this wavelength, as can be expected from the AC simulations, the effect of the substrate is very weak and do not degrade much the speed performance of the diode (fig. 5.a). At 800nm, on the contrary, the slow substrate diffusion current overlap between the adjacent bits and dominates over the photocurrent generated in the thin-film (fig. 5.b) which can make the distinction between zero and one impossible. The so-called long tail response effect is observed.

SOI, owing to its unique structure, can provide specific solutions on top of that available in Bulk to get rid of the slow substrate photogenerated diffusion current at high wavelength.

- The use of PIN SOI diodes on a membrane. This consists in removing the substrate under the PIN diodes by a etching post process which is stopped on the BOX (Laconte et al., 2004). After this removal, as the thin silicon film is now sandwiched between two oxides (front and buried oxide) which both induce compressive stress to the Si film, the Si film can start to buckle. This has been observed on a 500x500μm^2 lateral PIN diode fabricated in the UCL technology. In (Laconte et al., 2004), to avoid this effect they proposed to use a nitride layer



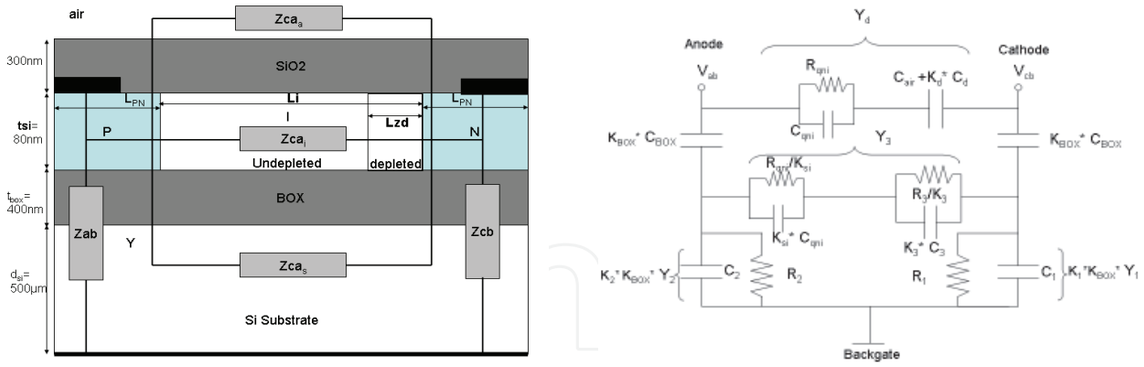
(a) $\lambda = 400nm$ (b) $\lambda = 800nm$

Fig. 5. Comparison between Atlas simulated transient response of the PIN diode with and without substrate to a '0101001100' optical data bit train of 10GBps. $L_i = 2\mu m$, P_{in}'1'=10mW/cm^2, P_{in}'0'=0mW/cm^2

which add a tensile stress to compensate. We note that this nitride layer can also be used as an anti-reflexion coating.
- Similarly a variant of the SOI technology, the SOS (Silicon on Sapphire) technology in which the Si substrate is replaced by a transparent Sapphire substrate (Apsel& Andreou, 2005) can be used.
- Finally a very promosing solution at high wavelength is to use Germanium on SOI Lateral PIN photodiodes (Koester et al., 2007). Ge is quite compatible with Si integration and is more and more present in MOSFET process for strain silicon devices. The use of ultrathin SOI as substrate for the growing of the Ge layer minimizes the problem of Si diffusion into Ge during thermal annealing steps and allows for an easy co-integration of Ge photodetector with Si circuits. As the absorption length of Ge is only a few hundred of nanometers at 850nm (roughly 50 times less than in Si) owing to its direct bandgap, thin-film (400 nm Ge layer) lateral PIN photodiodes can be fabricated which features similar bandwidth than thin-film SOI photodiodes but with high quantum efficiency. A 10x10 μm with a finger spacing of 0.4μm had a bandwidth of 27GHz at a bias voltage of -0.5V and a quantum efficiency of 30%. The dark current however higher than in a comparable SOI photodetector was still less than 10nA.

3. RC frequency

The diode also exhibits an impedance which combined with the input impedance of the readout circuit leads to a RC -3dB frequency, f_{RC}. In this section we will model the thin-film lateral SOI PIN diode impedance which is mainly capacitive. In what follows, we will first give the complete equivalent lumped circuit we derived in order to model the diode impedance. Then, we will explain the different elements of the circuit and focus on the elements which represent the anode to cathode impedance via the thin film impedance or the ideal diode case, the anode or cathode-to-substrate impedance and the MOS capacitor related to, and finally the coupling impedance between the anode and cathode via the substrate and via the air.



(a) Schematic view of our PIN diode structure and simplified equivalent impedance model

(b) Equivalent model for the calculation of the PIN diode capacitances

Fig. 6

In the general case, when there is a BOX and substrate underneath the thin active Si film, the total cathode or anode impedance Z_{cc} or Z_{aa} of the diode involved in f_{RC} is due to the cathode to anode impedance, Z_{ca}, from which the thin film impedance is just a part, and to the impedance of the N^+ (cathode) or P^+ (anode) region to the substrate, Z_{cb} or Z_{ab} resp. (fig. 6.a). The full impedance behaviour of the diode has to be modeled by the equivalent circuit of fig. 6.b. The different components will be explained in the forthcoming sections. Coefficients K_i are used to take into account the fringing effects which become more and more dominant with down scaling, whereas the admittance cross-sections become smaller and smaller compared to their length.

The value of these fringing factors K_i depends on geometrical dimensions as the length of the diffusion areas, the distance between them, the substrate thickness... Semi-empirical formulation can be derived from microstrip line theory (Garg& Bahl, 1979), (Kirschning&Jansen, 1984).

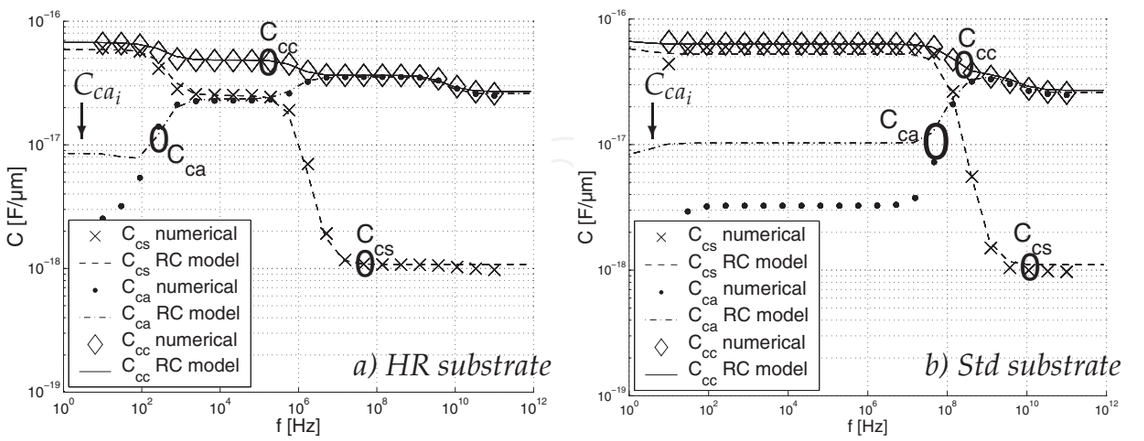


Fig. 7. Comparison of modeled and simulated capacitance by μm width vs. frequency of a) high resistivity (hr) and b) standard resistivity substrates. ST 0.13 μm thin-film SOI diodes. $L_i = 5\mu m$, m=2.

In our case we obtained the K_i factors by fitting model and numerical simulations (see table 1). The 2D numerical simulations were made with the ISE software. We simulated a 2 finger diode (PINIP structure) with full substrate thickness (d_{si}=500μm) and 500μm air layer on top of it to obtain a realistic fringing effect. As can be seen in figure 7.a for highly resistive (hr) substrate (P-doping of $2.10^{12}/cm^3$), the modeled value of the total cathode capacitance C_{cc} between C_{ca} and C_{cb} fairly matches the related simulated curves for frequencies as low as 100Hz. In the case of the standard resistivity (hr) substrate (P-doping of $6.10^{14}/cm^3$) (see figure 7.b) the agreement between modeled and simulated C_{ca} or C_{cb} curves is good only above 100MHz. This can be explained as the low frequency value of C_{ca} tends towards the thin-film capacitance C_{ca_i} (see fig. 7), which depends on the backgate voltage, V_b, and the film conditions. In our model, we have assumed the film as neutral and didn't take into account the influence of V_b. The simulations were performed with a value of V_b of 0V for which the film is in vertical depletion and where C_{ca_i} is reduced. However, the modeling satisfies our high speed purpose and, more over, modeled and simulated total capacitances, C_{cc}, fit very well for all frequencies, for both high and standard resistivity substrate cases.

3.1 The ideal diode impedance

In the ideal case, the diode impedance is only due to the impedance of the thin film region and is dominated upto high frequency by the capacitance of the depletion region C_d. In fact 3 components only are required to model this impedance behaviour versus frequency: C_d and the capacitance, C_{qni}, and resistance, R_{qni} of the quasi neutral part of the I-region if they exists ($L_i > L_{zd}$).

C_d decreases with L_i as long as the I-region is fully depleted, i.e. $L_i < L_{zd}$ and is also proportional to the junction area and to t_{si}, which results in much lower value for thin film SOI than in Bulk. Noting W the width and m the number of fingers of the PIN diode, we have:

$$C_d = m.\frac{\epsilon_{si}.W.t_{si}}{min(L_i, L_{zd})} \tag{43}$$

C_{qni} and R_{qni} determine the cut off frequency, $f_1 = \frac{1}{2\pi R_{qni} C_{qni}}$ where the diode capacitance falls from C_d to $\frac{C_{qni}.C_d}{C_{qni}+C_d} = m.\frac{\epsilon_{si}.W.t_{si}}{L_i}$. From classical semiconductor and circuits theories, noting σ_{qni} the conductivity of the quasi neutral I region, we have:

$$R_{qni} = \frac{L}{m.\sigma_{qni}W.t_{si}} \; C_{qni} = m.\frac{\epsilon_{si}W.t_{si}}{L} \; f1 = \frac{\sigma_{qni}}{2\pi.\epsilon_{si}} \simeq 10GHz \tag{44}$$

Fig. 8 shows good agreement between this model and numerical 2D simulations of the cathode to anode capacitive part C_{ca_i} of the impedance Z_{ca_i} of a diode without substrate, defined as:

$$\left(j.\omega C_{ca_i} + \frac{1}{R_{ca_i}}\right)^{-1} \tag{45}$$

R_{ca_i} is the resistive part of the ideal diode impedance in parallel with C_{ca_i} and is totally negligible up to f_1. However this simple model is not sufficient to predict or to simulate the capacitance behaviour of the real PIN diode with a BOX and a substrate underneath.

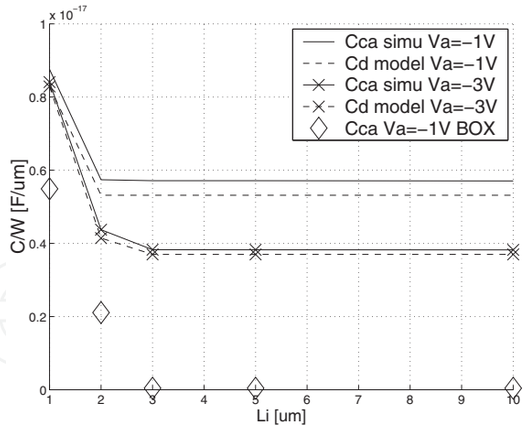
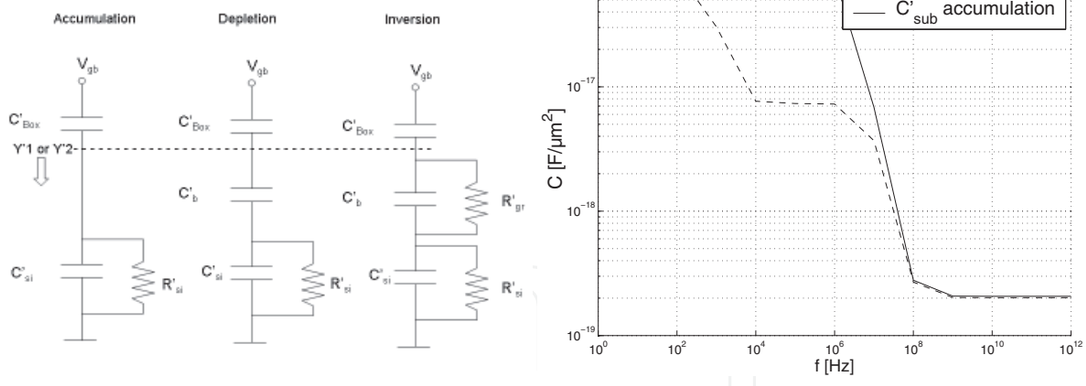


Fig. 8. Comparison of the modeled depletion capacitance Cd with the Atlas simulated cathode to anode capacitance Cca vs. L_i at f=20kHz of thin-film SOI diodes.

3.2 Modeling of the anode or cathode to substrate impedance

We will now focus on the modeling of the terms Y_1 and Y_2 of fig. 6.b related to the impedance of anode or cathode to the substrate. For this purpose we will first study the simpler structure of the N^+ or P^+ region in the Si film and its coupling to the substrate. Model and simulations show that the conclusions we can draw from this simpler structure on the cathode or anode to substrate impedance will stay valid in the general case (i.e. Z_{cb} or Z_{ab}) because the modification of this impedance through the substrate coupling stay negligible when affecting the global anode or cathode impedance (Z_{aa} or Z_{cc} resp.).



(a) C'_{sub} models (b) C'_{sub} vs. frequency

Fig. 9. a) Equivalent model for the calculation of an N^+ or P^+ diffusion to substrate capacitance (C'_{sub}) in accumulation, depletion and inversion regime and the equivalent Y'1 or Y'2 admittance. b) Modeled C'_{sub} vs. frequency behavior of hr substrates thin-film SOI diodes for strong inversion and accumulation regime.

The anode or cathode to substrate impedance of our simpler case Z_{sub} is in SOI mainly due to a MOS capacitor C_{sub}. Therefore, depending on the electrode (we will call it the gate in the following) to substrate equivalent voltage, $V_{gb_{eq}}$, C'_{sub} can cross three main different regimes: accumulation ($V_{gb_{eq}} < 0$ if p-type substrate), depletion and inversion($V_{gb_{eq}} > 0$).

In fig. 9.a and b, we can see the equivalent circuits for each regime and the evolution of the associated capacitance per unit area C'_{sub} with frequency in inversion and accumulation regimes respectively. $V_{gb_{eq}}$ is related to the actual gate to substrate voltage on contacts, V_{gb}, by (Tsividis, 1999):

$$V_{gb_{eq}} = V_{gb} - \phi_{ms} + \frac{Q'_{BOX}}{C'_{BOX}} \tag{46}$$

Q'_{BOX} and C'_{BOX} are the BOX fixed charge density and capacitance per unit area respectively. ϕ_{ms} is the contact potential or work function difference between gate and substrate and is given for the cathode and anode cases respectively by:

$$\phi_{ms_c} = -Ut.log(\frac{N_s.N_d}{ni^2}) \quad \phi_{ms_a} = Ut.log(\frac{N_s}{N_a}) \tag{47}$$

where N_s is the p-type substrate doping, and N_d and N_a are the cathode and anode doping levels respectively.
In actual processes, under normal (low) voltage operation, the trapped charge density (typ. value of $2 \times 10^{10}.q$ $[C/cm^2]$) is usually the dominant term in $V_{gb_{eq}}$ and leads C'_{sub} into the strong inversion regime even for the anode.
In inversion, at very low frequency, any change in the gate-substate voltage V_{gb} (i.e. the cathode- or anode-substrate voltage of the diode) and then in the gate charge, is balanced by a change in the thin inversion charge just underneath the BOX and the capacitance is dominated by the BOX capacitance. Physically, an abundance of electrons exists immediately below the oxide and forms the bottom "plate" of the oxide capacitor, just as an abundance of holes provides that plate in the case of accumulation regime. On the contrary, in the depletion regime, there is no highly conductive inversion or accumulation layer under the BOX, and any change in V_{gb} must be compensated by a change in the depth of the depletion region (X_d) with the surface potential Φ_s and thus V_{gb}. The equivalent capacitance C'_{sub} is then a series combination of the BOX capacitance and the depletion capacitance C'_b and is then lower than C'_{BOX} (Raskin, 1997):

$$X_d = \sqrt{\frac{2\epsilon_{si}.\Phi_s}{q.N_s}} \; C'_b = \frac{\epsilon_{si}}{X_d} \; C'_{sub} = \frac{C'_{BOX}.C'_b}{C'_{BOX} + C'_b} \tag{48}$$

For higher frequencies however, the inversion layer charge cannot keep up with the fast changing δV_{gb} and the required charge changes must be provided by covering or uncovering acceptor atoms at the bottom of the depletion region, just as in the case of depletion operation. Again the equivalent capacitance C'_{sub} becomes a series combination of the BOX capacitance and the depletion capacitance C'_b and is then lower than C'_{BOX}.
The relaxation time of minority carriers expresses the inertia of the inversion layer under the oxide layer. Sah and al (Sah et al., 1957) have demonstrated that the finite generation and recombination within the space charge region is the dominant factor in controlling the frequency response of the inversion layer. Hofstein and Warfield (Hofstein& Warfield, 1965) define for the strong inversion regime layer a resistance (R'_{gr}) associated with this generation-recombination U (see fig. 9.a), as follows:

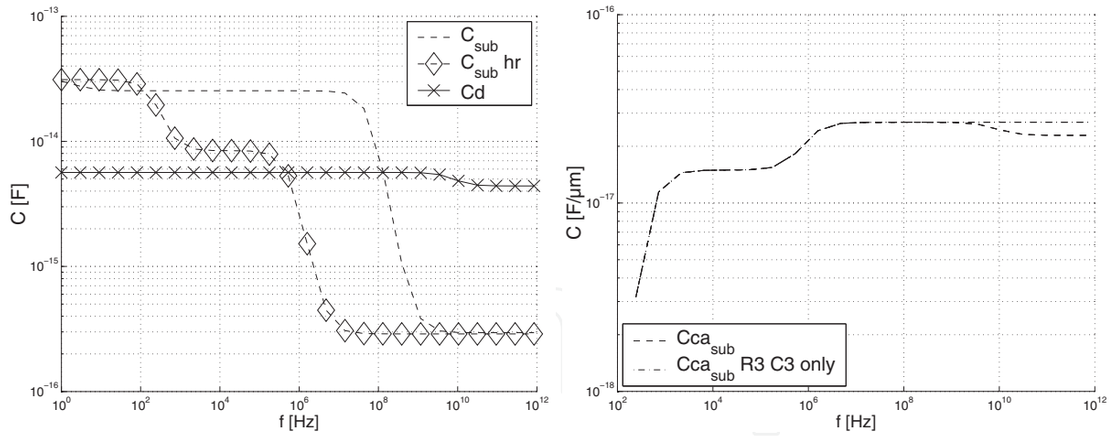
$$R'_{gr} = \frac{\Phi_s}{q.X_d.U} \quad U = \frac{n_i}{\tau_o} \tag{49}$$

where τ_o is the time carrier density fluctuation to decay to its equilibrium concentration by recombination through traps and is typically the order of 10^{-6} sec (Nicollian& Brews, 1982). This equivalent resistance allows one for taking into account the frequency response of the inversion layer in the dark. The relaxation time of the minority carriers is given by $\tau_{rg} = R'_{rg}.C'_b$. For the calculation of X_d in strong inversion, we can consider the classical approximation of Φ_s, the surface potential, pinned to two times the Fermi level (Tsividis, 1999).

For still higher frequencies in the GHz range, the relaxation time of the majority carriers cannot be neglected anymore and can be modeled by a resistance, R'_{si} and a capacitance, C'_{si} which are the substrate silicon resistance and capacitance respectively (Raskin, 1997). Noting d_{si} the Si substrate thickness, we have:

$$R'_{si} = \frac{d_{si}}{\sigma_{si}} \quad C'_{si} = \frac{\epsilon_{si}}{d_{si}} \tag{50}$$

In this range of frequencies, C'_{sub} is then dominated by C'_{si} and is therefore very small which is advantageous for high speed design. The capacitance behaviour of a typical thin film SOI diode in a $0.13\mu m$ PDSOI technology is plotted with standard and high resistive substrate (hr) on fig. 10.a. The diode exhibits total length and width of $50\mu m$ and an intrinsic length of $2\mu m$. The higher the substrate resistivity, the lower the frequency at which this transition happens.



(a) C_{sub} hr and sr vs. C_d (b) Anode to cathode substrate capacitance $C_{ca_{sub}}$

Fig. 10. a) Capacitance vs. frequency behavior of thin-film ST 013 SOI diodes. a) Cathode to substrate capacitance C_{sub}, assumed in the strong inversion regime, for standard and high resistivity (hr) substrates vs. the ideal diode capacitance C_d. ($L_i = 2\mu m$, L_{tot} and W of $50\mu m$ and $L_{PN} = 0.34\mu m$. b) Anode to cathode substrate capacitance by μm width, $C_{ca_{sub}}$, models. hr substrates. $L_i = 5\mu m$,m=2.

If the general behaviour of C_{sub} versus frequency can be now well understood by the model, the plateau values of the model are too low when compared to numerical simulations. This is

also pointed out and explained by (Raskin, 1997) when comparing model to measurements. The higher value of the capacitance is due to a fringing field effect. Indeed the length of the diffusions L_{PN} is very small compared to the thickness of the substrate and then the effective area of the capacitor is higher than just $L_{PN}.W$. We then have to use a correction factor, K_1 or K_2 for Y_1 or Y_2. With deep submicron processes, we even have important fringing field effect for C_{BOX}. A coefficient K_{BOX} has then to be introduced. These three coefficients increase with the intrinsic length showing a field confinement effect of the adjacent electrodes. Values for ST 0.13μm process are shown in table 1.

3.3 Coupling effect

Numerical simulations with Atlas or ISE show that the model of the anode to cathode impedance which only take into account the depletion capacitance C_d is too simple. Simulations, indeed, show that the coupling effect through the substrate is dominant at high frequency and therefore cannot be neglected. It shows the same transition frequencies as the capacitances to substrate (fig. 7) and hence is based on similar phenomena than those discussed above. We have to use a new admittance Y_3 as shown in the equivalent model of fig 6.b and from there we can compute $Y_{ca_{sub}}$, the coupling admittance through the substrate. A model was firstly introduced in (Raskin, 1997) to calculate the coupling between coplanar line on SOI substrate only using R3 and C3. The expressions of R3 and C3 are given using the approximation of two infinite lines on a very thick silicon substrate ($t_{si} <<< d_{si}$) (Raskin, 1997), (Walker, 1990) and K3 is a fringing factor.
However, when the diode is not fully depleted ($L_i > L_d$), simulations show a decrease of $C_{ca_{sub}}$ above 10GHz, while this model only shows a constant value (see fig. 10.b). Our explanation is that part of the electric field induced in the substrate is curved upwards and cross again the buried oxide as well as the quasi neutral region. An exact model is quite complex but as the field always see the BOX and a silicon region by adding $Rqni/K_{qni}$ and $K_{qni}.C_{qni}$ we can model the transition with a very good accuracy (see fig. 7). For the expressions of R3 and C3 we derived:

$$R3 = [m.K3.\frac{\pi\epsilon_0\sigma_{si}}{4ln[\frac{\pi.min(L_i,L_{zd})}{K_{BOX}.L_{PN}+t_{si}}+1]}W]^{-1}[\Omega] \quad C3 = m.K3.\frac{\pi\epsilon_0(\epsilon_{rsi})}{4ln[\frac{\pi.min(L_i,L_{zd})}{K_{BOX}.L_{PN}+t_{si}}+1]}W[F] \tag{51}$$

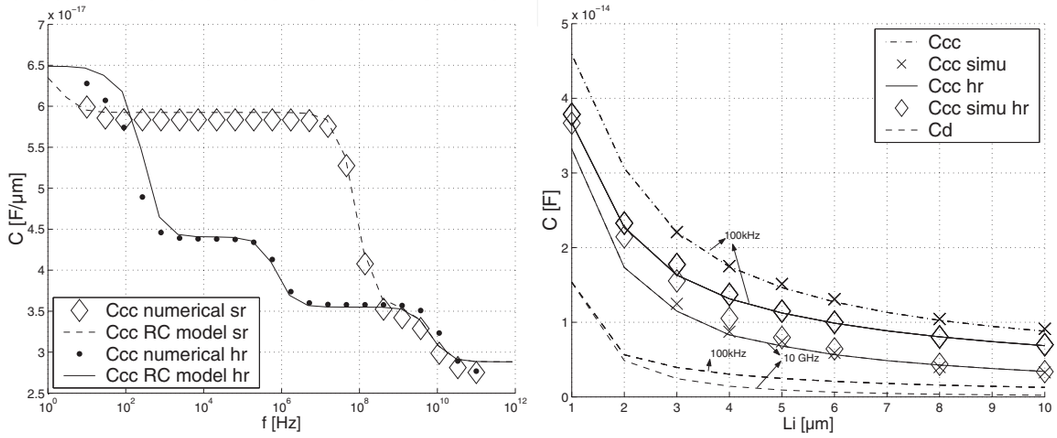
In this formulation, the value of K3 was constant vs. L_i and equal to 5 for L_{PN} of 0.34μm.
For the front coupling through the air, numerical simulations show that the fringing field capacitance through the air, C_{air}, cannot be neglected because the thicknesses of the silicon film and of the electrode, t_{al}, were small compared to L_i. We can assume a formulation to compute this capacitance coupling similar to that used for C3 but with air instead of silicon:

$$C_{air} = m.0.5.\frac{\pi\epsilon_0}{4ln[\frac{\pi.L_i}{L_{PN}+tal}+1]}W[F] \tag{52}$$

We also add the capacitance through the thin film with a fitting coefficient K_d close to unity for L_i small and reducing for increasing values of L_i, for a larger portion of the electric field propagates through the air.
In figure 11.a we see a comparison of the cathode capacitance for standard and high resistive substrates. In the bandwidth of interest for high speed circuits starting from a few hundred of MHz, we see that there is no clear advantages of using a high-resistive substrate.

L_i	K_{BOX}	K_1=K_2	K_3	K_{si}	K_d
1	1.2	3.2	5	0.25	0.9
2	1.8	3.7	5	0.25	0.8
3	1.9	5	5	0.05	0.62
4	1.95	6.5	5	0.05	0.61
5	2	8	5	0.03	0.6
10	2.5	12	5	0.03	0.2

Table 1. Fringing effect coefficients value vs. L_i for ST013 ($L_{PN} = 0.34\mu m$).



(a) C_{cc} vs. frequency (b) C_{cc} vs. L_i

Fig. 11. Comparison of the cathode capacitance of ST013 thin-film SOI diodes for sr and hr substrates a) by μm width vs. frequency. $L_i = 3\mu m$, m=2. b) vs. L_i of a 50x50 μm^2 ST013 thin-film SOI diodes @100kHz and 10GHz. The ideal case, C_d is also plotted.

In figure 11.b, we show modeled and simulated capacitances of a PIN diode of 50x50 μm^2 vs. L_i at 100kHz and 10 GHz for sr and hr substrates. In all cases, this capacitance mainly decreases with L_i because the number of fingers decreases as well. C_{cc} is also bigger than C_d, the ideal diode case, but keeps same order of magnitude. Again, we observe that, if the value of C_{cc} is lower for hr substrates than for sr ones at 100kHz, there are sensibly equal at 10GHz.

3.4 2^{nd} order effects: reduction of the depletion plateau of C_{sub} with light

For a high resistivity substrate in the usual case of strong inversion, the effect of depletion is more pronounced and makes C_{sub} already low compared to C_d at a still lower frequency of 10kHz (the beginning of the depletion plateau). However this is only true if no light illuminates the depletion region in the substrate. This is the case in the dark (part of N+ and P+ regions covered by metal electrodes) or everywhere at low wavelength (typ. $<$ than 400 nm) where all the light is absorbed in the thin Si-film.

If light is absorbed in the depletion region in the substrate, the positive effect of depletion is firstly reduced because it reduces the surface potential Φ_s and therefore X_d (Grosvalet& Jund, 1967). The plateau value of C_{sub} increases with the power absorbed in this area and then with P_{in}.

Secondly if light is absorbed in depletion region in the substrate, the beginning of the depletion plateau happens at higher frequencies because an extra photogeneration process

speeds up the thermal minority carriers process in the depletion region (Grosvalet& Jund, 1967). Equation 49 has then to be modified in the following way:

$$R'_{gr} = \frac{\Phi_s}{q.X_d.U} \quad U = \frac{n_i}{\tau_o} + g \tag{53}$$

where g is the equivalent or mean generation term in the depletion region.

3.5 Substrate losses

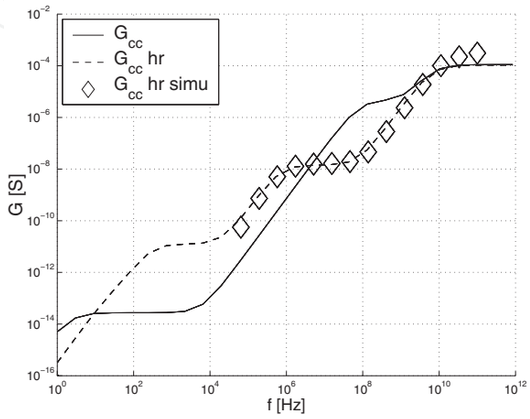


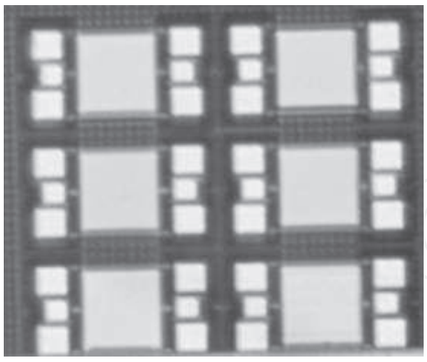
Fig. 12. Comparison of conductance vs. frequency behavior of standard and high resistivity (hr) substrates thin-film SOI diodes ($L_i = 3\mu m$, L_{tot} and W of $50\mu m$ and $L_{PN} = 0.34\mu m$ (ST 013)in strong inversion. For the hr case model is also compared to numerical simulation

The cathode (or anode) impedance has a complex value. If the imaginary part is related to C_{cc}, the real part can be modeled by an equivalent conductance G_{cc} in parallel with C_{cc}. G_{cc} takes into account the signal losses through the substrate. To be negligible, G_{cc}^{-1} has to remain high compared to the next stage equivalent resistor, R, which conditions the current to voltage gain in the bandwidth of interest. For actual SOI processes the bandwidth of interest is in the tens of GHz and R is lower than $1k\Omega$. Fig 12 shows the modeled evolution of G_{cc} for hr and sr SOI substrates. The same transitions than for C_{cc} are appearing. At high frequencies C_{BOX} looks more and more like a short and the losses are increasing. In both cases (hr and sr), however, G_{cc}^{-1} remains at least 10 times larger than R in the 10GHz range. For the hr case, we also compare the modeled G_{cc} curve to that given by the numerical simulations and can note the very good agreement.

3.6 Impedance measurements

In order to further validate our RC model of the PIN photodiodes, on-wafer S parameter measurements were performed. 6 lateral thin-film ungated PIN photodiodes were designed on ST 0.13 μm PD SOI technology with different device parameters (intrinsic length L_i, N^+ and P^+ diffusion lengths L_{pn}, and number of finger m) and with coplanar accesses in order to be able to characterize these devices in a wide range of frequencies. Parameters and a photograph of the realized diodes are shown in Fig. 13.

Most of the diodes were realized using the conservative value of L_{pn}=1.36μm used in the last design rules we receive from ST for lateral photodiodes. One diode was realized using the value of L_{pn}=0.34μm which is the value for the source and drain extension of



L_i (μm)	L_{pn} (μm)	L_{tot} (μm)	m	W (μm)
1	1.36	249.16	105	250
2	1.36	250	75	250
2	0.34	250.72	107	250
5	1.36	249.4	39	250
10	1.36	251.28	22	250
100	1.36	204.08	2	250

Fig. 13. Photograph and parameters of the PIN photodiodes realized in ST 0.13 μm PD SOI technology.

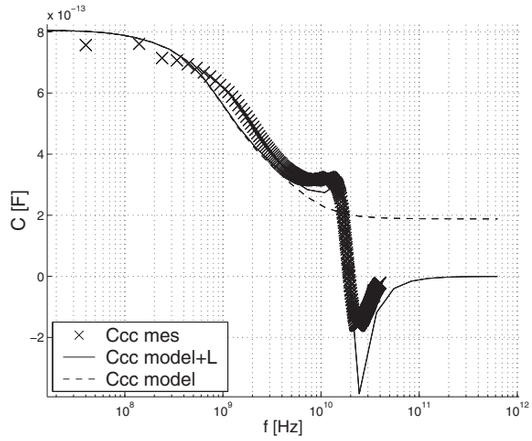
the MOS transistor in this technology. This last diode wasn't working, certainly because of mask misalignments (a gateless device with N^+ and P^+ contacts is more subject to mask misalignments than a MOS transistor).

AC-capacitances given by numerical simulations (using the parameters $L_{pn} = 1.36\mu m$) and by our model (only readjusting the value of L_{pn}, but leaving unchanged the fringing field coefficients obtained for $L_{pn} = 0.34\mu m$) were in good agreement and no further fitting was necessary. We then compared model and measurements. These measurements were obtained after a calibration to remove the impedance effect of the RF probes and cables used to connect the device to the spectrum analyzer. An open substraction was also performed to remove the impedance of the access pad. This was mainly a capacitive impedance (capacitance of about 90fF). It was relatively negligible compared to the diode impedance, except for that with an intrinsic length of $100\mu m$. A metal path of about $50\mu m$ long, which wasn't removed by de-embedding, remains between the device anode and cathode and their related access pad.

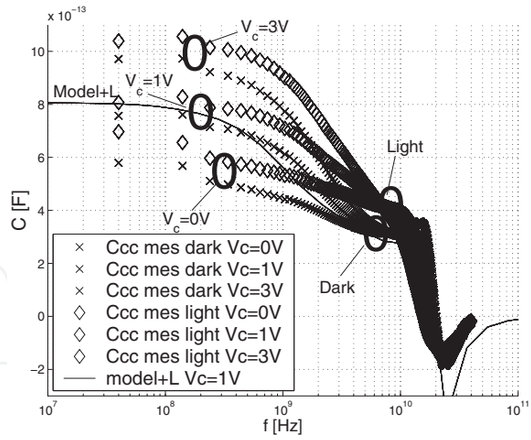
The measurements were done in the 40MHz-40GHz band under illumination or not. For each of these measurements, the DC voltage of the anode was connected to the ground while the DC-voltage of the cathode was successively fixed to 0, 1V and 3V with a bias-T.

In this range of frequency, we observed as expected the transition in the capacitive behavior of C_{cc} between its mid-range value (dominated by the depletion plateau of C_{cb}) to the high range value (dominated by C_{ca} and where C_{cb} is low because the substrate behave like a dielectric) (fig. 14.a). The mid-frequency range plateau value is expected to be influenced by bias, illumination and buried oxide trapped charges since the value of the depletion capacitance which is dominant in this range is strongly dependent on these parameters. This was observed in the measurements as can be seen in fig. 14.b. The high frequency range value is quite unaffected by these parameters as expected since the whole substrate now behaves like a dielectric.

The transition frequency between mid and high range value depends on the substrate doping: The higher the substrate doping, the higher this frequency. From our measurements, we deduce that the substrate doping should be of the order of 1.10^{14} cm^{-3}. This value is, however, higher than the real physical doping of the hr-substrate. This typical effect with SOI hr-substrate (Lederer& Raskin, 2006) is explained by surface conduction in the low resistive



(a) Comparison of measured and modeled Capacitance vs. frequency in the dark



(b) Measured capacitance vs. frequency for different bias and illumination conditions. A modeled curve at Vc=1V in the dark is also shown for comparison

Fig. 14. Thin-film SOI diodes ($L_i = 10\mu m$, L_{tot} and W of about $250\mu m$ and $L_{PN} = 1.36\mu m$. ST 0.13 μm PD SOI technology).

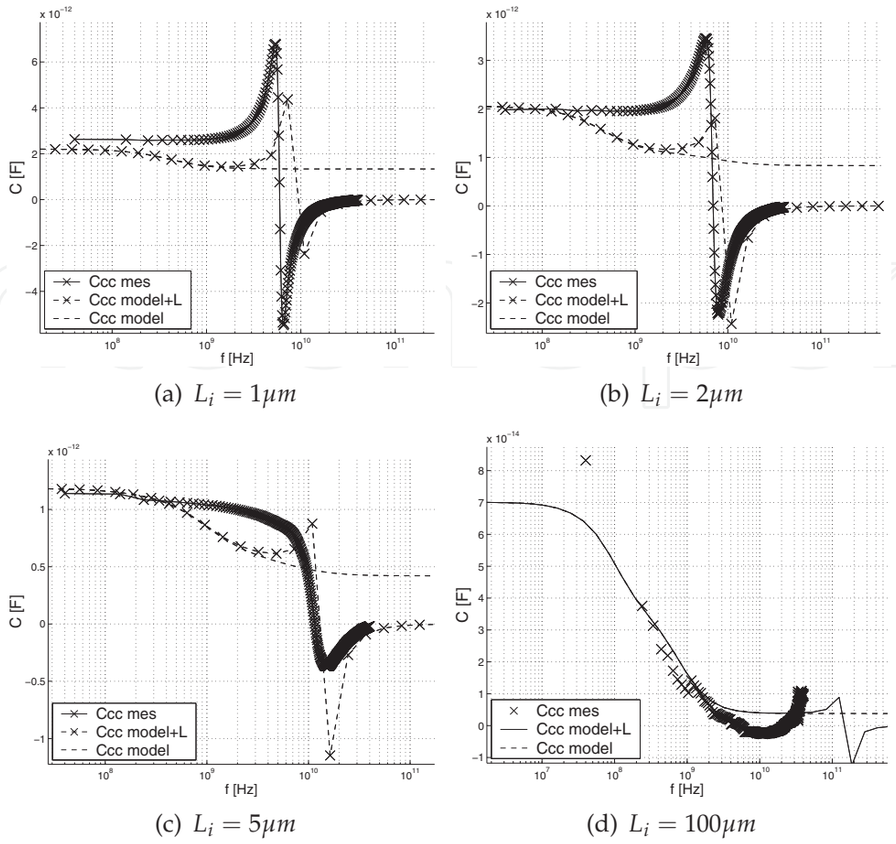
inversion layer that appears just underneath the BOX and the presence of coplanar accesses for the measurements. The impedance of the cathode to the substrate backgate electrode is now in parallel with the impedance of the cathode to the ground plane of the coplanar access via this top substrate inversion layer. It is the latter which dominates the high frequency transition and presents the same kind of RC transition behavior but at a higher frequency because of the lower resistivity of this inversion Si layer.

Finally, a resonance effect appears around the 10GHz range. The imaginary part of Y_{cc} first increases and presents a positive peak, then decreases and presents a negative peak. This is attributed to the self inductance of the metal path between the pads and the electrodes. Indeed by simply adding an inductor of 0.25nH in series with the cathode of the diode, which is a good approximation of having an inductor of 0.125nH in series with the cathode and with the anode if the resonance effect appears in a frequency range where C_{cb} and $C_{ab} < C_{ca}$, our model predicts a very similar behavior (see curves labelled model+L on fig. 14 to fig. 15).

The amplitude of the peak and the frequency at which it happens depend on the capacitor value. It varies, therefore, with L_i and with the inductance value. The higher their LC product, the lower the frequency at which it happens. For usual 50x50μm^2 diodes and shorter metal lines of monolithically integrated diodes and circuits, this effect should not appear. It however have to be kept in mind during the layout phase of the circuits (avoid too long connection lines) and may be checked again and incorporated by simulation after the layout phase. This resonance effect could also be useful, if well controlled, to increase the bandwidth of the system (Gray& Meyer, 1984) as it is done to increase the bandwidth of transimpedance amplifiers (Maxim, 2004).

4. Conclusions

Speed performances of thin-film SOI PIN photodetectors have been investigated in terms of transit time and RC frequency. Our original models, fully validated by 2D numerical simulations and measurements, enable to deeply understand the underlying physical



(a) $L_i = 1\mu m$ (b) $L_i = 2\mu m$

(c) $L_i = 5\mu m$ (d) $L_i = 100\mu m$

Fig. 15. Comparison of measured and modeled capacitance vs. frequency of thin-film SOI diodes ($L_i = 1\mu m$, L_{tot} and W of about $250\mu m$ and $L_{PN} = 1.36\mu m$. ST 0.13 μm PD SOI technology).

phenomena and predict and optimize their speed performances for the target applications. Concerning the transit time frequency, our modeling allows one to simply and accurately select the intrinsic length required for a given bandwidth. We showed that as long as the entire I region is laterally depleted, the transit time limit is due to fast drift and the related -3dB frequency, f_{tr}, decreases as L_i^2. If L_i becomes greater than L_d, carriers transit is dominated by a slower diffusion mechanism and the related -3dB frequency decreases faster with L_i. The effectiveness of BOX insulation from the slow substrate photogenerated current and resulting problem of bandwidth degradation due to partial isolation of the BOX in near IR wavelength have been discussed for the first time and solutions have been presented.
Concerning the modeling of the diode impedance, our physical RC model can be implemented in a circuit simulator and allows the co-design and optimization of the photodiode and the readout circuit as a function of design parameters such as the intrinsic length of the diode, L_i. At low frequency, the total cathode capacitor, C_{cc}, is dominated by the cathode to substrate capacitor, C_{cs} which is a MOS capacitor (Raskin, 1997). At higher frequency, C_{cs} reduces below the value of C_d as carriers in the Si substrate cannot follow the ac-signal and the substrate behaves like a dielectric. C_{cc} then also reduces but cannot reach the ideal lowest value of C_d, as at higher frequency the coupling through the substrate (Y_3) between anode and cathode is increased and then C_{ca} increases. Above about 100MHz, C_{cc} of SOI PIN diodes remains,

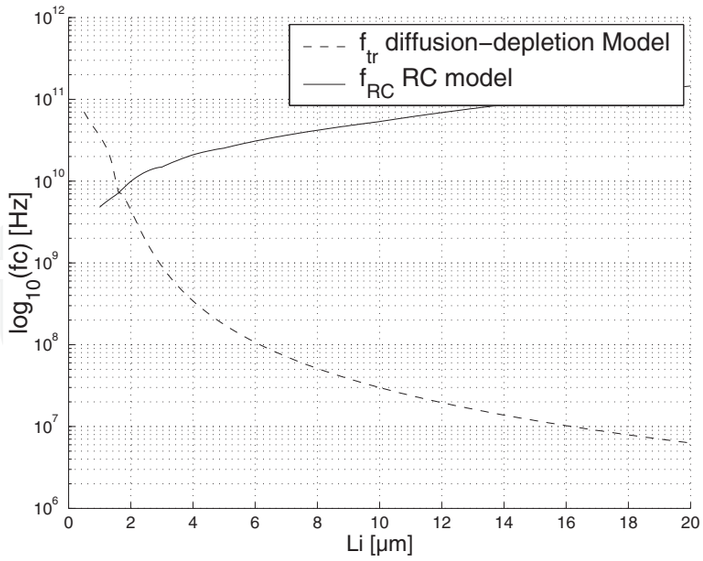


Fig. 16. Evolution of f_{tr} and f_{RC} with Li, bias voltage Vd=-1V, photodiode area A_t=50x50μm^2, typical load resistor of 1$k\Omega$.

however, very low compared to the equivalent capacitor of integrated bulk diodes so that, for identical speed performances, we can increase the load resistor and then increase the overall system sensitivity in SOI compared to bulk.
Consequently, the total -3dB frequency combining f_{tr} and f_{RC} shows an optimum vs. L_i (fig. 16) which in thin SOI diodes can reach a few tens of GHz, while the fastest integrated bulk diodes are typically limited to a few GHz only (Zimmermann, 2000). A SOI diode with L_i of 6μm already fulfills the 250MHz bandwidth requirement for actual Blue DVD specifications under 1V operation, while a 2μm device is suitable for the 10Gb/s Ethernet standard.

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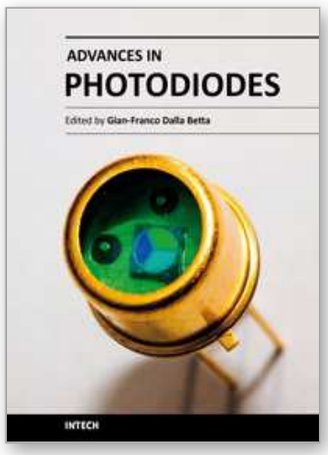

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Photodiodes, the simplest but most versatile optoelectronic devices, are currently used in a variety of applications, including vision systems, optical interconnects, optical storage systems, photometry, particle physics, medical imaging, etc. Advances in Photodiodes addresses the state-of-the-art, latest developments and new trends in the field, covering theoretical aspects, design and simulation issues, processing techniques, experimental results, and applications. Written by internationally renowned experts, with contributions from universities, research institutes and industries, the book is a valuable reference tool for students, scientists, engineers, and researchers.

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