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Operation of Active Front-End Rectifier in Electric Drive under Unbalanced Voltage Supply

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1. Introduction

Non-standard conditions in the power network such as voltage unbalance can negatively affect operation of electric drives. The unbalance can be caused by a failure in the network or by an unbalanced load in the electric vicinity of the affected drive. Unsymmetrical voltages at the input of a voltage source inverter cause pulsations in the DC link voltage when not properly taken care of. This may result in significantly reduced power capabilities and, therefore, limited controllability of the drive. This text deals with the effects of unbalanced voltage supply on the DC-link voltage pulsations, methods to address this problem and the additionally imposed constraints in operating regions of the rectifier.

2. Control method

A simplified scheme of the drive under investigation is shown in Fig. 1. The front-end controlled rectifier is connected to the mains through input filter inductors. The output current of the rectifier supplies the DC current to the output inverter and maintains the voltage across the DC-link capacitors constant at the same time. The value of this current can be controlled by suitable switching of solid-state elements in the front-end stage.

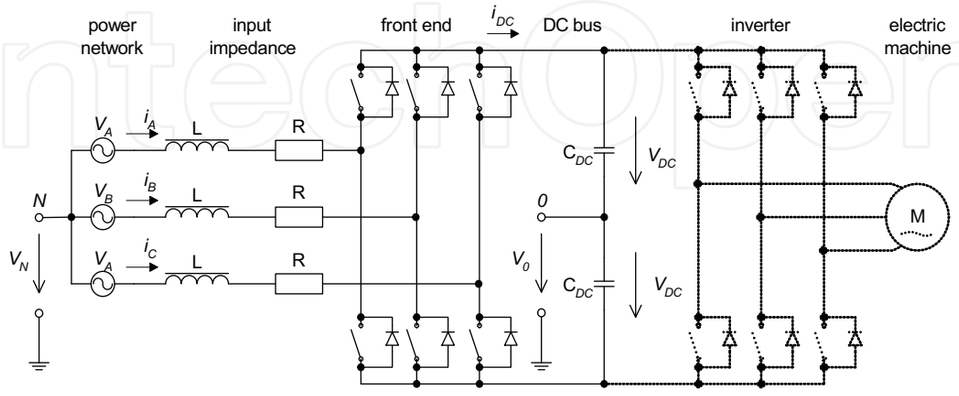

Fig. 1. Scheme of system under investigation.

Suitable control of the front-end AC/DC converter can be employed in order to draw constant input power from the power network even at unbalanced voltage supply

(Stankovic & Lipo, 2001; Lee et al., 2006; Cross et al., 1999; Song & Nam, 1999). The switching functions for the front-end AC/DC converter are generated so that a constant voltage across the DC bus is maintained. Series combinations of inductance and resistance are considered at the input terminals of the inverter.
The system can be electrically described by the following set of ordinary differential equations (Chomat & Schreier, 2005):

$$v_A - L\frac{di_A}{dt} - Ri_A - v_{SA} + v_N - v_0 = 0\,, \tag{1}$$

$$v_B - L\frac{di_B}{dt} - Ri_B - v_{SB} + v_N - v_0 = 0\,, \tag{2}$$

$$v_C - L\frac{di_C}{dt} - Ri_C - v_{SC} + v_N - v_0 = 0\,, \tag{3}$$

where

$$v_{SA} = s_A \cdot V_{DC}\,, \tag{4}$$

$$v_{SB} = s_B \cdot V_{DC}\,, \tag{5}$$

$$v_{SC} = s_C \cdot V_{DC} \tag{6}$$

are the voltages at the input of the inverter. The functions s_A, s_B, and s_C are the corresponding unit switching functions of the particular phases of the front-end stage, which represent the fundamental harmonic components of the pulse width modulated output. Sinusoidal switching functions with the nominal frequency are considered throughout this paper, whereas the higher harmonics that would arise in a real power converter are neglected in the calculation for simplification. V_{DC} represents one half of the overall DC-link voltage here. The voltage v_N is the electric potential of the neutral of the mains and v_0 is the electric potential of the centre point of the capacitor bank in the DC bus.
The DC-link current can be calculated from the phase currents and the switching functions according to

$$i_{DC} = \frac{1}{2}\left(s_A i_A + s_B i_B + s_C i_C\right). \tag{7}$$

The coefficient ½ takes into account the fact that currents in both positive and negative directions that flow through different current paths in the DC bus are produced by the rectifier.
An unbalanced system of phase quantities can advantageously be represented by phasors of positive and negative rotating sequences. It is not necessary to take zero-sequence quantities into account here as no neutral wire is considered in the system and, therefore, no zero-sequence current can develop. The resulting rotating vector of such a quantity may then be written as

$$\mathbf{x} = \mathbf{X_P} e^{j\omega t} + \mathbf{X_N} e^{-j\omega t}\,. \tag{8}$$

The subscripts *P* and *N* denote the positive and negative rotating sequences, respectively. Based on these assumptions, (1) - (3) and (4) – (6) may be rewritten in phasor form as

$$\mathbf{V_P} - (R + j\omega L)\mathbf{I_P} - \mathbf{S_P}V_{DC} = 0\,, \tag{9}$$

$$\mathbf{V_N} - (R - j\omega L)\mathbf{I_N} - \mathbf{S_N}V_{DC} = 0\,. \tag{10}$$

The solution of (9) and (10) for positive and negative sequence currents is

$$\mathbf{I_P} = \frac{\mathbf{V_P} - \mathbf{S_P}V_{DC}}{R + j\omega L}\,, \tag{11}$$

$$\mathbf{I_N} = \frac{\mathbf{V_N} - \mathbf{S_N}V_{DC}}{R - j\omega L} \tag{12}$$

and the corresponding rotating vector of the input currents is therefore

$$\mathbf{i} = \mathbf{I_P}e^{j\omega t} + \mathbf{I_N}e^{-j\omega t}\,. \tag{13}$$

Similarly, we can formally introduce a rotating vector of the switching functions

$$\mathbf{s} = \mathbf{S_P}e^{j\omega t} + \mathbf{S_N}e^{-j\omega t}\,. \tag{14}$$

Then the resulting instantaneous value of the current supplied into the DC link by the front-end converter from (7) can be written in the vector form as

$$i_{DC} = \frac{1}{2}\frac{3}{2}\mathrm{Re}\{\mathbf{i}\cdot\bar{\mathbf{s}}\}\,, \tag{15}$$

where the bar over the symbol denotes the complex conjugate value. The term 3/2 appears in (15) due to the transformation from rotating vector form to instantaneous quantities.
The resulting relation obtained after substituting (13) and (14) into (15) can be written as the sum of two separate current components and given as

$$i_{DC} = i_{DC(avg)} + i_{DC(2\omega t)}\,, \tag{16}$$

where

$$i_{DC(avg)} = \frac{3}{4}\mathrm{Re}\left\{\frac{\mathbf{V_P} - \mathbf{S_P}V_{DC}}{R + j\omega L}\bar{\mathbf{S}}_\mathbf{P} + \frac{\mathbf{V_N} - \mathbf{S_N}V_{DC}}{R - j\omega L}\bar{\mathbf{S}}_\mathbf{N}\right\}, \tag{17}$$

$$i_{DC(2\omega t)} = \frac{3}{4}\mathrm{Re}\left\{\frac{\mathbf{V_P} - \mathbf{S_P}V_{DC}}{R + j\omega L}\bar{\mathbf{S}}_N e^{j2\omega t} + \frac{\mathbf{V_N} - \mathbf{S_N}V_{DC}}{R - j\omega L}\bar{\mathbf{S}}_\mathbf{P} e^{-j2\omega t}\right\}. \tag{18}$$

The first component, (17), represents a DC component and the second, (18), represents a pulsating component with the frequency twice as high as that of the mains. The pulsating component is only produced when the negative sequence of either the input voltages or the switching functions is present.

From (18), a condition for the elimination of the pulsating component in the DC link can be derived

$$\mathrm{Re}\left\{\frac{\mathbf{V_P}-\mathbf{S_P}V_{DC}}{R+j\omega L}\bar{\mathbf{S}}_N e^{j2\omega t}\right\}=-\mathrm{Re}\left\{\frac{\mathbf{V_N}-\mathbf{S_N}V_{DC}}{R-j\omega L}\bar{\mathbf{S}}_{\mathbf{P}} e^{-j2\omega t}\right\}. \tag{19}$$

As the real part of a complex number equals the real part of its conjugate value, (18) can also be written as

$$\mathrm{Re}\left\{\frac{\mathbf{V_P}-\mathbf{S_P}V_{DC}}{R+j\omega L}\bar{\mathbf{S}}_N e^{j2\omega t}\right\}=-\mathrm{Re}\left\{\frac{\bar{\mathbf{V}}_{\mathbf{N}}-\bar{\mathbf{S}}_{\mathbf{N}}V_{DC}}{R+j\omega L}\mathbf{S_P} e^{j2\omega t}\right\}. \tag{20}$$

For the above equation to be satisfied at any time, the following must hold providing that there is non-zero input impedance

$$(\mathbf{V_P}-\mathbf{S_P}V_{DC})\bar{\mathbf{S}}_{\mathbf{N}}=-\left(\bar{\mathbf{V}}_{\mathbf{N}}-\bar{\mathbf{S}}_{\mathbf{N}}V_{DC}\right)\mathbf{S_P}. \tag{21}$$

If the input voltages are known and the control is free to choose the positive sequence component of the switching functions, the negative sequence of the switching functions obtained from (21) is

$$\mathbf{S_N}=\frac{\bar{\mathbf{S}}_{\mathbf{P}}\mathbf{V_N}}{2\bar{\mathbf{S}}_{\mathbf{P}}V_{DC}-\bar{\mathbf{V}}_{\mathbf{P}}}. \tag{22}$$

It should be noted that the relation does not contain values of input resistance and inductance and is, therefore, the same for pure inductance as well as for pure resistance connected to the front end of the inverter.

As the amplitudes of the individual switching functions need to be less than or equal to one, the range of practical combinations of $\mathbf{S_P}$ and $\mathbf{S_N}$ is constrained. A simple, and rather conservative, condition to keep the switching functions in allowable limits can be written as

$$|\mathbf{S_P}|+|\mathbf{S_N}|\le 1. \tag{23}$$

For more precise evaluation of the constraints, we need to evaluate magnitudes of switching vectors in individual phases

$$|\mathbf{S}_A|=\left|\mathbf{S_P}+\bar{\mathbf{S}}_{\mathbf{N}}\right|, \tag{24}$$

$$|\mathbf{S}_B|=\left|\mathbf{S_P}a+\bar{\mathbf{S}}_{\mathbf{N}}a^2\right|, \tag{25}$$

$$|\mathbf{S}_C|=\left|\mathbf{S_P}a^2+\bar{\mathbf{S}}_{\mathbf{N}}a\right| \tag{26}$$

and limit the magnitude of each of them

$$\left(|\mathbf{S}_A|\le 1\right)\wedge\left(|\mathbf{S}_B|\le 1\right)\wedge\left(|\mathbf{S}_C|\le 1\right). \tag{27}$$

For its operation, the above discussed control method requires to monitor the instantaneous values of the input phase voltages and of the DC-link voltage. Based on this information, a convenient combination of values of $\mathbf{S_P}$ and $\mathbf{S_N}$ can be chosen to produce the required value of the DC-link current and to satisfy the conditions in (22) and (23) at the same time. From $\mathbf{S_P}$ and $\mathbf{S_N}$, the switching functions for the individual legs of the rectifier are computed and switching pulses are generated for individual switching devices based on a particular pulse width modulation algorithm. The switching devices are considered to be transistors or thyristors with forced commutation.

3. Operation of drive under unbalanced voltage supply

3.1 Numerical simulation of drive under unbalanced voltage supply

Operation of the described system has been numerically simulated under various types of unbalanced voltage supply in order to investigate the effect of the unbalance on the system behavior and the influence of certain circuit parameters. The reference parameters of the input impedance were chosen to be R = 0.1 Ω and L = 10 mH. The input phase voltages had nominal voltage amplitudes of 230 V, nominal frequency of 50 Hz, and mutual phase shifts of 120° to form a three-phase voltage system in the case of the symmetrical system. The DC-link voltage was set to 560 V and the capacitor of 1000 μF was used in the DC bus (Chomat et al., 2007).

First, operation of the investigated system under symmetrical voltage supply was simulated to obtain the reference case to compare with unbalanced operation. Figure 2 shows input phase voltages and currents and Figure 3 shows the DC-link current and voltage. It can be seen that both electrical quantities in the DC bus are smooth with no visible pulsations.

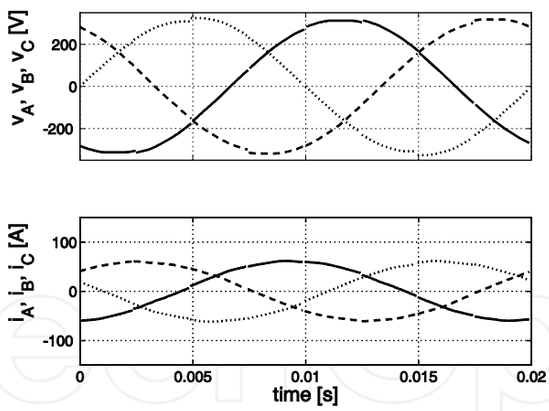

Fig. 2. Phase voltages and currents under symmetrical voltage supply.

Second, the unbalance caused by setting the magnitude of the voltage in phase *A* to 200 V_{RMS} was investigated. Figures 4 and 5 show the corresponding quantities at the input of the rectifier and in the DC bus when no measures are taken to eliminate the pulsations by suitable modification of switching in the active front-end rectifier. The DC-link current and voltage contain significant pulsations that would make control of the drive more complicated. When the switching functions are modified in order to eliminate the effect of the supply voltage unbalance, the pulsations are nearly entirely eliminated, Figures 6 and 7. This has also an effect on the input phase currents compared to the previous case.

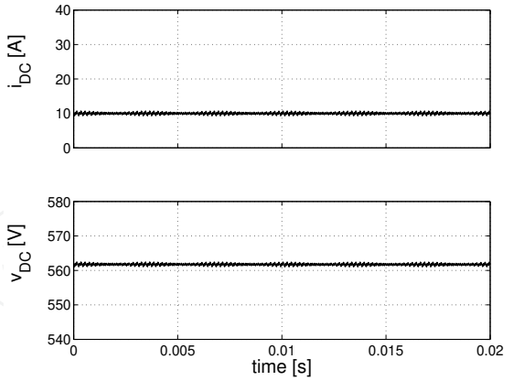

Fig 3. DC-link voltage and current under symmetrical voltage supply.

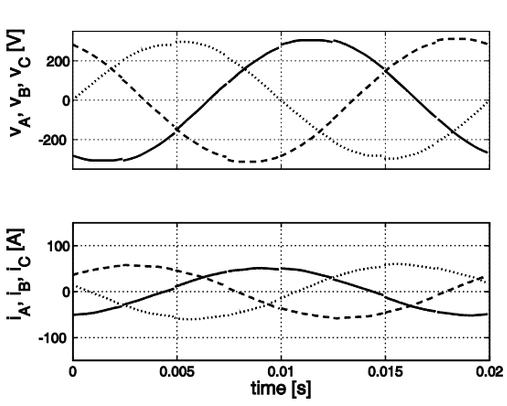

Fig 4. Phase voltages and currents under unbalanced voltage supply without compensation.

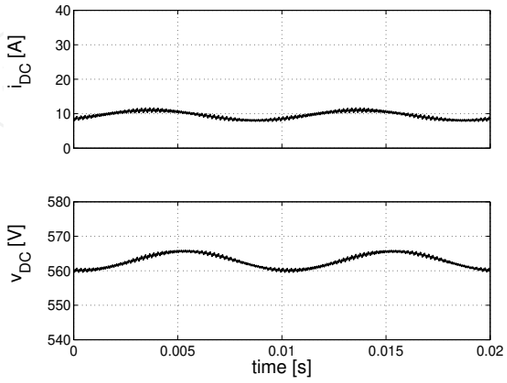

Fig. 5. DC-link voltage and current under unbalanced voltage supply without compensation.

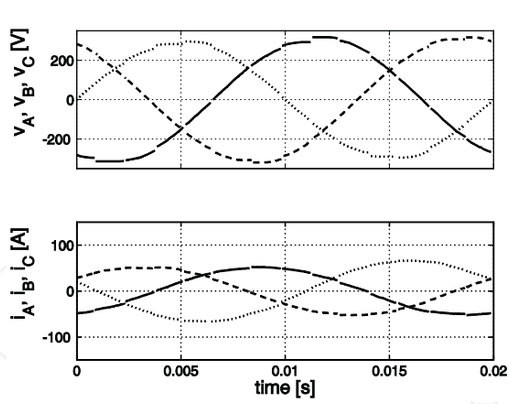

Fig. 6. Phase voltages and currents under unbalanced voltage supply with compensation.

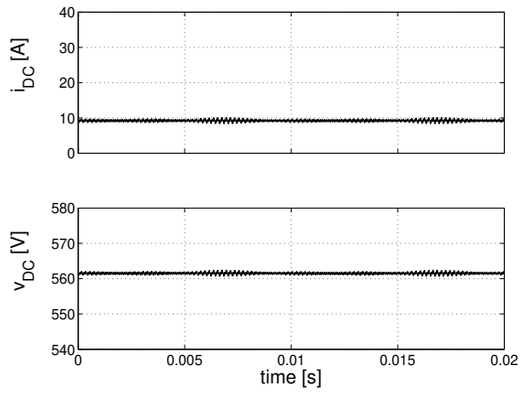

Fig. 7. DC-link voltage and current under unbalanced voltage supply with compensation.

When DC-link capacitor is reduced to have the capacity of only 500 μF instead of 1000 μF, Figures 8 and 9, the DC-link voltage pulsations are increased twice as could be expected in case with no measures to eliminate the effect of the unbalance in the front-end rectifier. No change appears in the case when switching functions are modified to eliminate the effect of the unbalance, Figures 10 and 11.

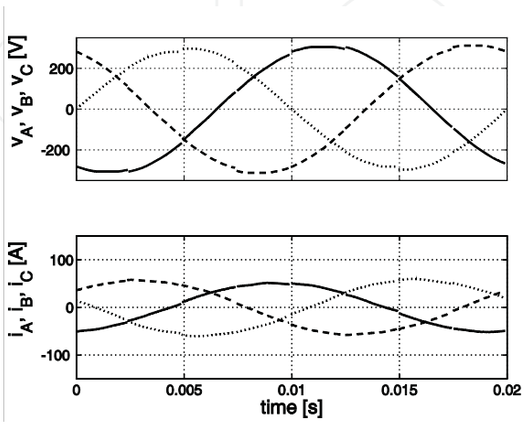

Fig. 8. Phase voltages and currents under unbalanced voltage supply with reduced DC-link capacitance without compensation.

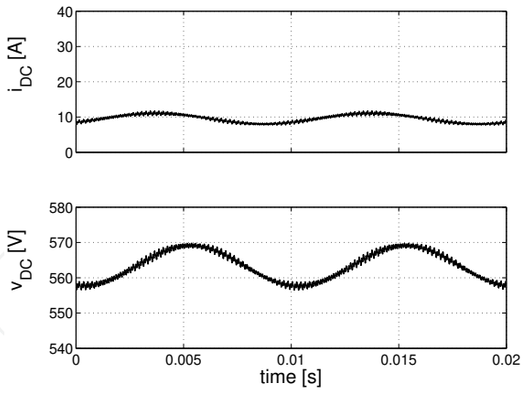

Fig. 9. DC-link voltage and current under unbalanced voltage supply with reduced DC-link capacitance without compensation.

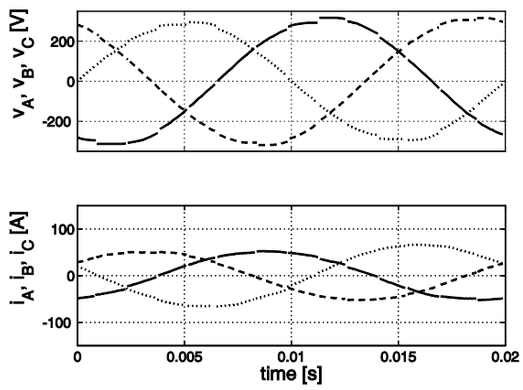

Fig. 10. Phase voltages and currents under unbalanced voltage supply with reduced DC-link capacitance with compensation.

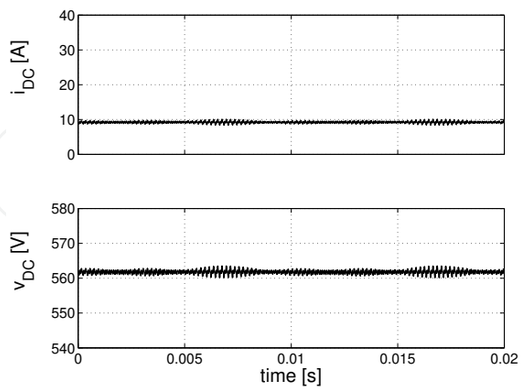

Fig. 11. DC-link voltage and current under unbalanced voltage supply with reduced DC-link capacitance with compensation.

The change of the input inductance from 10 mH to 5 mH leads to an adequate increase in the input phase currents as well as in the DC-link current, Figures 12 to 15. The relative amount of pulsations remain at about the same levels.

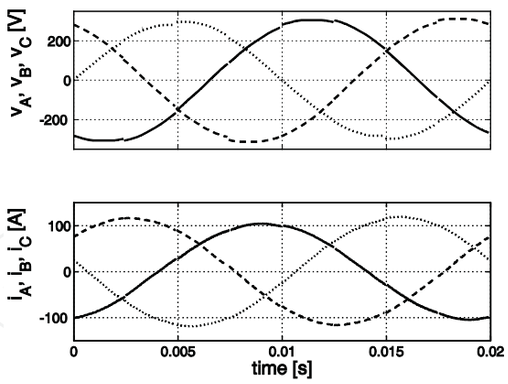

Fig. 12. Phase voltages and currents under unbalanced voltage supply with reduced input inductance without compensation.

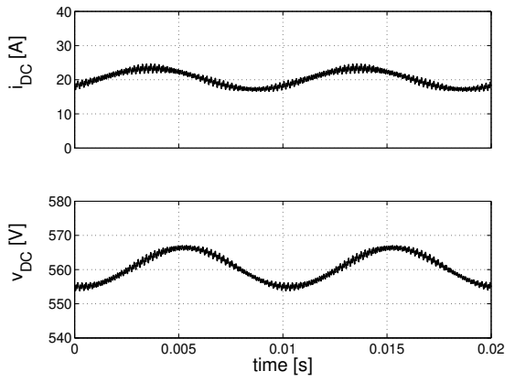

Fig. 13. DC-link voltage and current under unbalanced voltage supply with reduced input inductance without compensation.

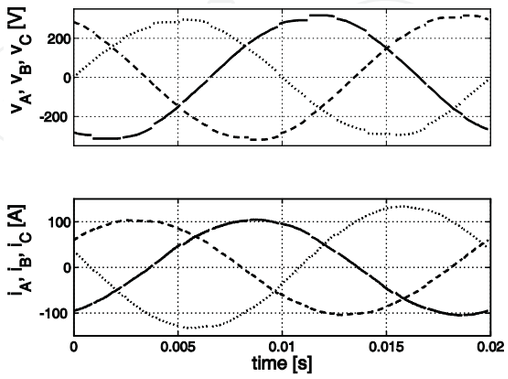

Fig. 14. Phase voltages and currents under unbalanced voltage supply with reduced input inductance with compensation.

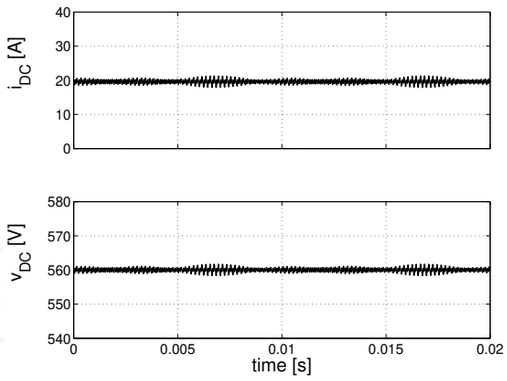

Fig. 15. DC-link voltage and current under unbalanced voltage supply with reduced input inductance with compensation.

Finally, the unbalance caused by shifting the voltage phasor of phase *A* by 10° was investigated. Corresponding results due to the changes in circuit parameters are illustrated in Figures 16 to 27. It can be noted that the effects are similar to the previous case of unbalance.

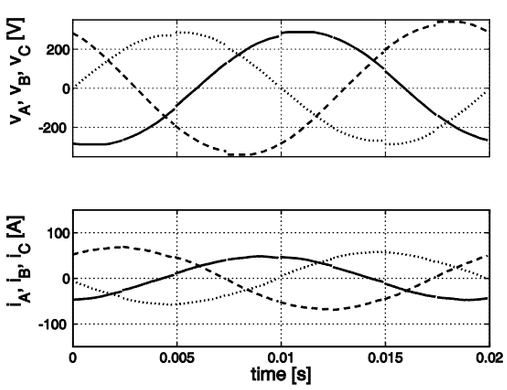

Fig. 16. Phase voltages and currents under unbalanced voltage supply without compensation.

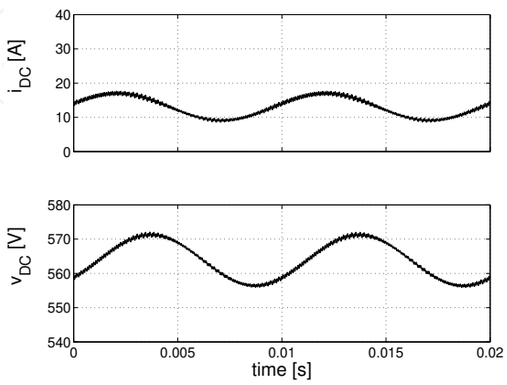

Fig. 17. DC-link voltage and current under unbalanced voltage supply without compensation.

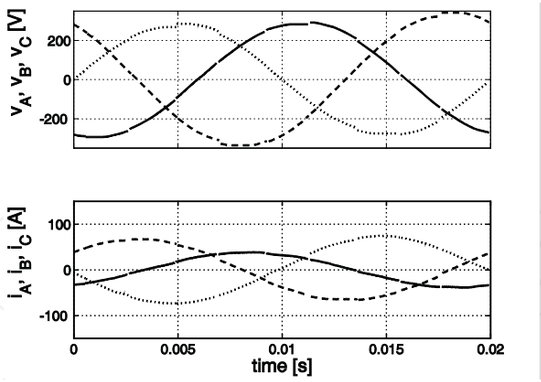

Fig. 18. Phase voltages and currents under unbalanced voltage supply with compensation.

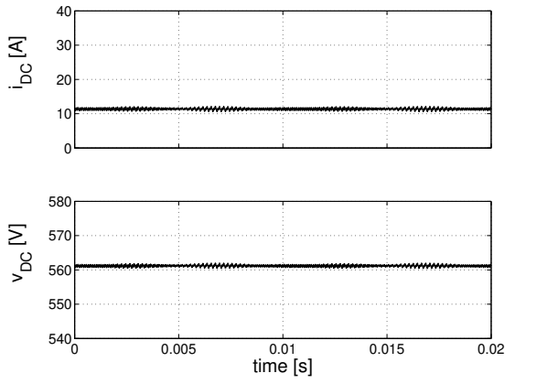

Fig. 19. DC-link voltage and current under unbalanced voltage supply with compensation.

The effect of reduction of the DC-link capacitor from 1000 μF to 500 μF is shown in Figures 20 through 23.

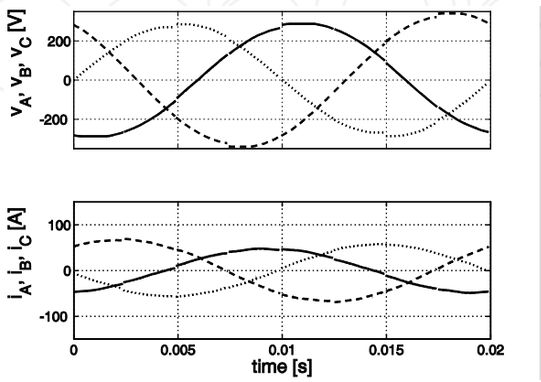

Fig. 20. Phase voltages and currents under unbalanced voltage supply with reduced DC-link capacitance without compensation.

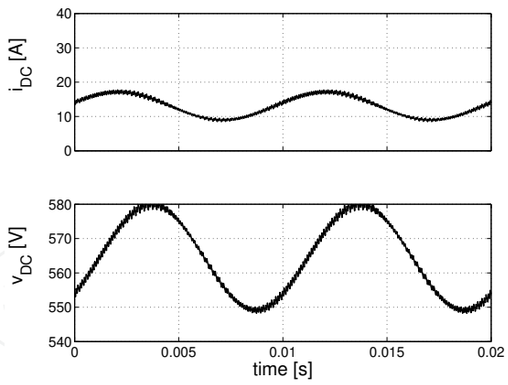

Fig. 21. DC-link voltage and current under unbalanced voltage supply with reduced DC-link capacitance without compensation.

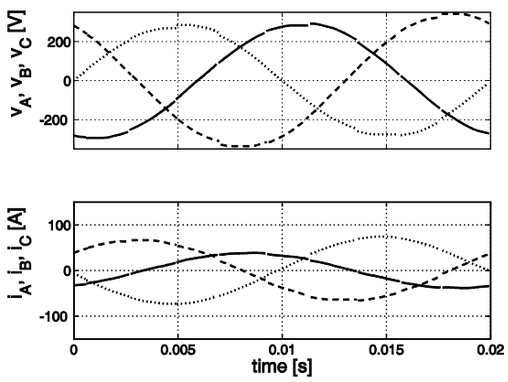

Fig. 22. Phase voltages and currents under unbalanced voltage supply with reduced DC-link capacitance with compensation.

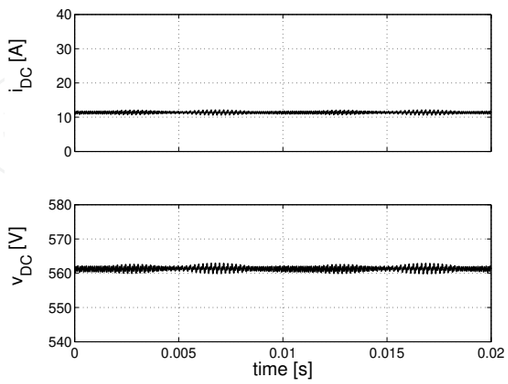

Fig. 23. DC-link voltage and current under unbalanced voltage supply with reduced DC-link capacitance with compensation.

The corresponding situation for reduced input inductance from 10 mH to 5 mH is illustrated in Figures 24 to 27.

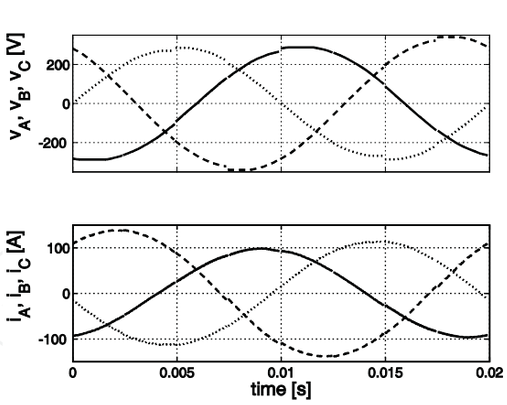

Fig. 24. Phase voltages and currents under unbalanced voltage supply with reduced input inductance without compensation.

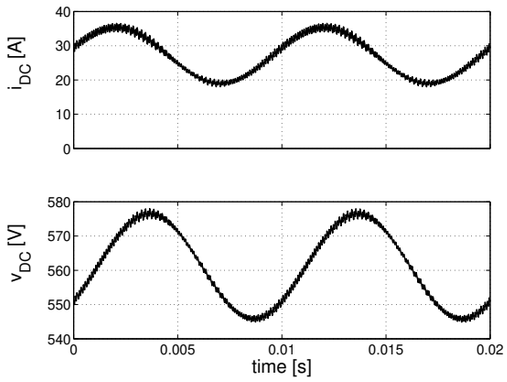

Fig. 25. DC-link voltage and current under unbalanced voltage supply with reduced input inductance without compensation.

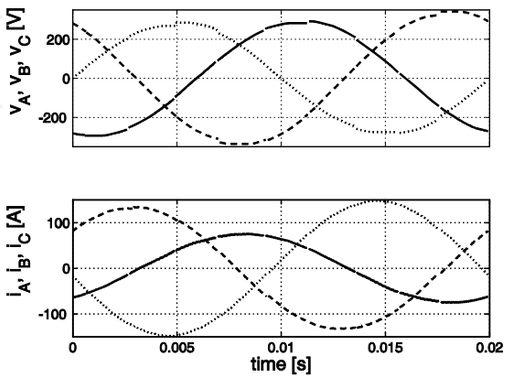

Fig. 26. Phase voltages and currents under unbalanced voltage supply with reduced input inductance with compensation.

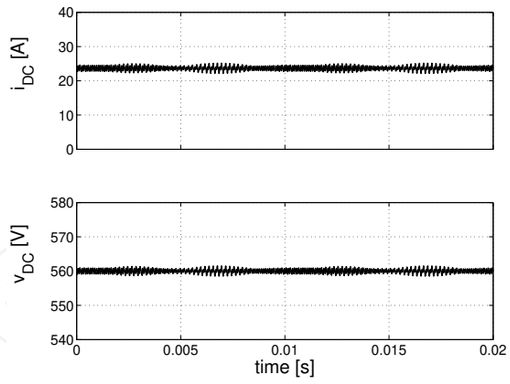

Fig. 27. DC-link voltage and current under unbalanced voltage supply with reduced input inductance with compensation.

3.2 Limitation of control range due to unbalanced voltage supply

The necessity to generate the negative sequence component of the switching functions in order to eliminate the effect of the supply-voltage unbalance on the DC-link voltage pulsations reduces the control range for the positive sequence component of the switching functions (Chomat et al., 2009). This is due to the fact that in individual phases the maximum of the switching function can only reach one at most at any given time. Another constraint results from the current rating of the converter. The resulting constraints depend on the value and type of the unbalance.

Analysis of the limitation corresponding to various types of unbalanced supply voltages has been carried out. The reference parameters of the input impedance were chosen to be R = 0.1 Ω and L = 10 mH. The input phase voltages had nominal voltage amplitudes of 230 V, nominal frequency of 50 Hz, and mutual phase shifts of 120° to form a three-phase voltage system in the case of the symmetrical system. The DC-link voltage was set to 400 V.

The choice of the positive sequence component of the switching functions from the available control range affects both the magnitude of the DC-link current and the currents in individual input phases. Figure 28 shows what magnitudes of the DC-link current correspond to the coordinates from the available control range. The unbalance was formed

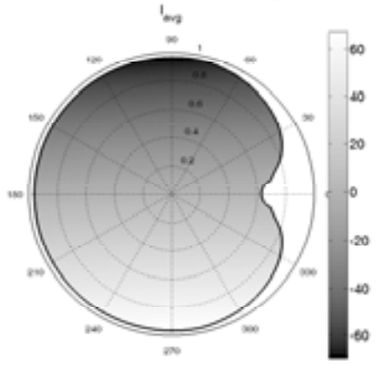

Fig. 28. DC-link current under unbalanced voltage supply (L = 10 mH, R = 0.1 Ω, V_{dc} = 400 V).

by setting the magnitude of the voltage in phase A to 0.75 p.u. The corresponding maximal input phase current magnitude, calculated as the maximum of all the phase currents, is shown in Figure 29. It can be seen from Figure 28 that the resulting DC-link current decreases in the vertical direction of the operating region, whereas the maximal input current in Figure 29 decreases in the horizontal direction. The corresponding measure of the current unbalance is depicted in Figure 30 and the average power factor of all the three input phases is depicted in Figure 31.

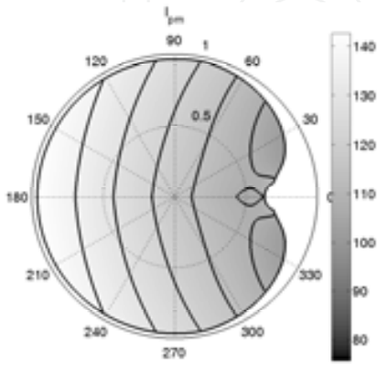

Fig. 29. Maximal input phase current under unbalanced voltage supply (L = 10 mH, R = 0.1 Ω, V_{dc} = 400 V).

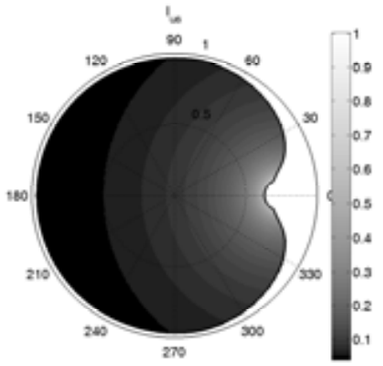

Fig. 30. Input current unbalance under unbalanced voltage supply (L = 10 mH, R = 0.1 Ω, V_{dc} = 400 V).

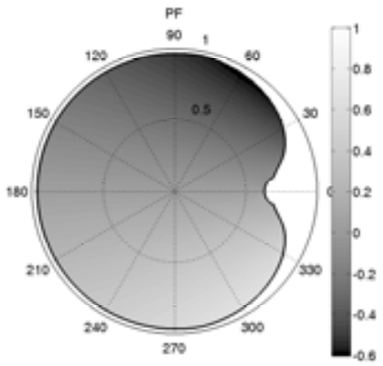

Fig. 31. Power factor under unbalanced voltage supply (L = 10 mH, R = 0.1 Ω, V_{dc} = 400 V).

If we change the value of the input inductance from 10 mH to 1 mH, the constraints caused by the switching functions remain the same as can be seen from Figures 32 through 35. However, both the DC-link current and the input current increased nearly ten times as the input reactance represents the main limiting factor for the currents entering the rectifier. The excessive values of the currents would, in a case of a real rectifier, impose additional restrictions to the operating regions resulting from current stress of electronic components in the bridge. This can also be considered in the shape of new borders of operating regions.

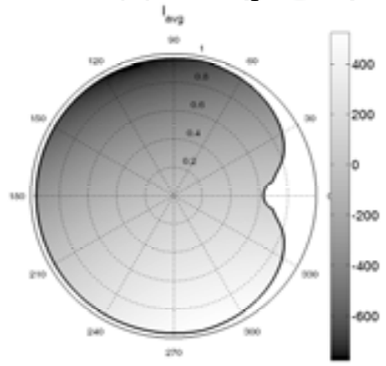

Fig. 32. DC-link current under unbalanced voltage supply (L = 1 mH, R = 0.1 Ω, V_{dc} = 400 V).

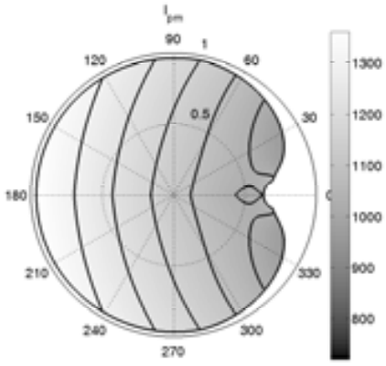

Fig. 33. Maximal input phase current under unbalanced voltage supply (L = 1 mH, R = 0.1 Ω, V_{dc} = 400 V).

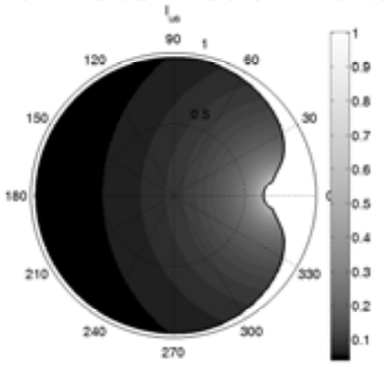

Fig. 34. Input current unbalance under unbalanced voltage supply (L = 1 mH, R = 0.1 Ω, V_{dc} = 400 V).

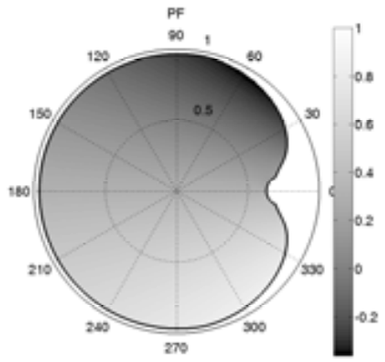

Fig. 35. Power factor under unbalanced voltage supply (L = 1 mH, R = 0.1 Ω, V_{dc} = 400 V).

A different situation arises when the input resistance is increased ten times to 1 Ω. The corresponding electrical quantities are shown in Figures 36 through 39. The increase in the DC-link and input phase currents is not as dramatic as the resistance plays less significant role in limiting the currents than the inductance. The values of the currents are similar to the ones in the first case.

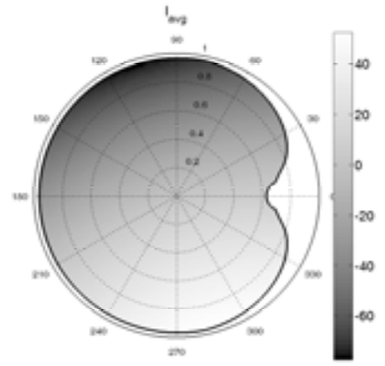

Fig. 36. DC-link current under unbalanced voltage supply (L = 1 mH, R = 1 Ω, V_{dc} = 400 V).

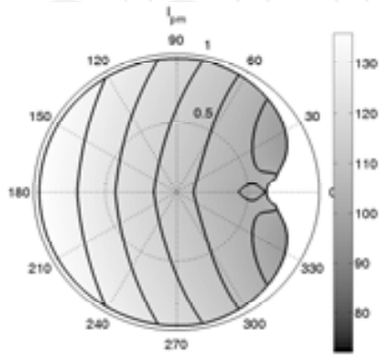

Fig. 37. Maximal input phase current under unbalanced voltage supply (L = 1 mH, R = 1 Ω, V_{dc} = 400 V).

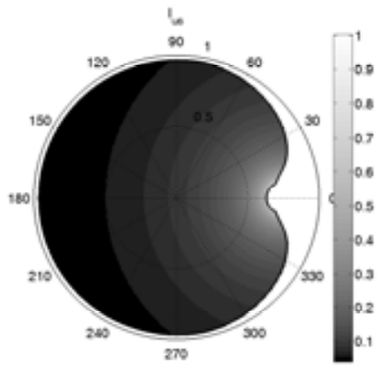

Fig. 38. Input current unbalance under unbalanced voltage supply (L = 1 mH, R = 1 Ω, V_{dc} = 400 V).

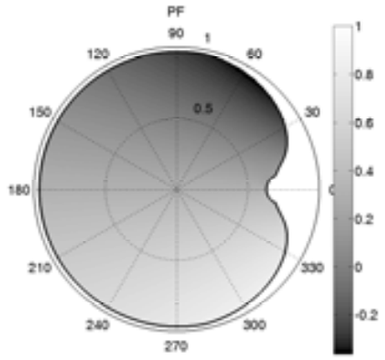

Fig. 39. Power factor under unbalanced voltage supply (L = 1 mH, R = 1 Ω, V_{dc} = 400 V).

A change in the DC-link voltage introduces, on the other hand, a noticeable change in the shape of constraints caused by the limitation of the switching functions. Figures 40 through 43 show the situation for the decrease in the DC-link voltage from 400 V to 200 V and Figures 45 through 47 show the situation for the increase to 600 V. In the latter case, a rise of an isolated restricted area in the right hand side of the figure completely surrounded by available control space can be noticed.

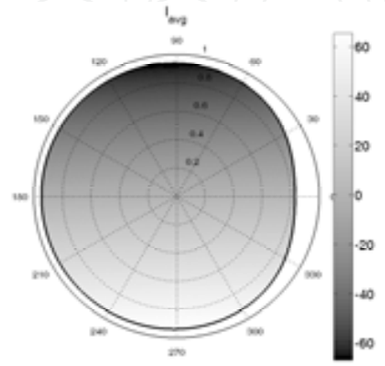

Fig. 40. DC-link current under unbalanced voltage supply (L = 10 mH, R = 0.1 Ω, V_{dc} = 200 V).

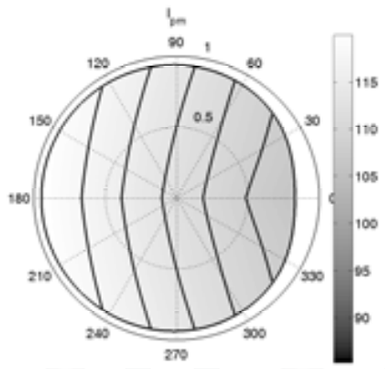

Fig. 41. Maximal input phase current under unbalanced voltage supply (L = 10 mH, R = 0.1 Ω, V_{dc} = 200 V).

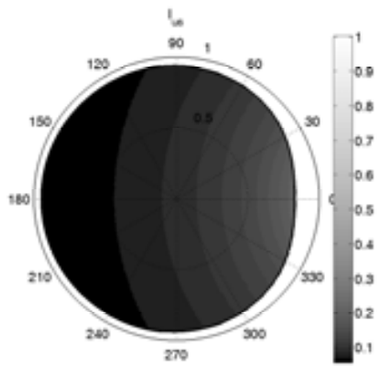

Fig. 42. Input current unbalance under unbalanced voltage supply (L = 10 mH, R = 0.1 Ω, V_{dc} = 200 V).

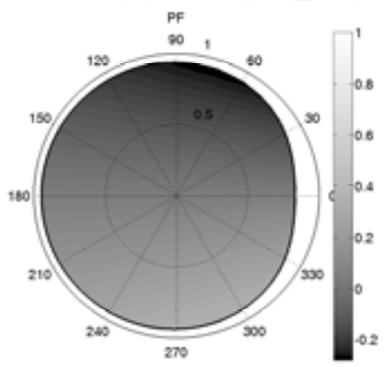

Fig. 43. Power factor under unbalanced voltage supply (L = 10 mH, R = 0.1 Ω, V_{dc} = 200 V).

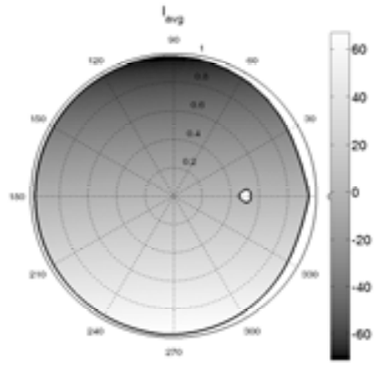

Fig. 44. DC-link current under unbalanced voltage supply (L = 10 mH, R = 0.1 Ω, V_{dc} = 600 V).

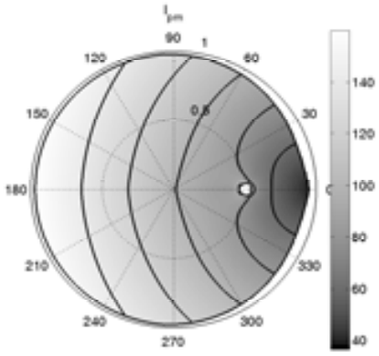

Fig. 45. Maximal input phase current under unbalanced voltage supply (L = 10 mH, R = 0.1 Ω, V_{dc} = 600 V).

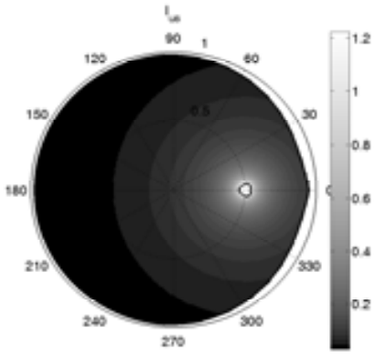

Fig. 46. Input current unbalance under unbalanced voltage supply (L = 10 mH, R = 0.1 Ω, V_{dc} = 600 V).

Measurements on an experimental system identical to the simulated one have been carried out in order to verify the investigated method. The scope traces in Figure 48 show the measured current in phase A and the DC link current when the negative-sequence in the supply voltage is not compensated for by the control method and the DC link current, therefore, contains significant component pulsating with a frequency of 100 Hz, twice the

fundamental network frequency. The case when unbalanced voltage system is compensated by the investigated control method is illustrated in Figure 49. It can be seen that the pulsating component of the DC link current has been effectively eliminated by the investigated method.

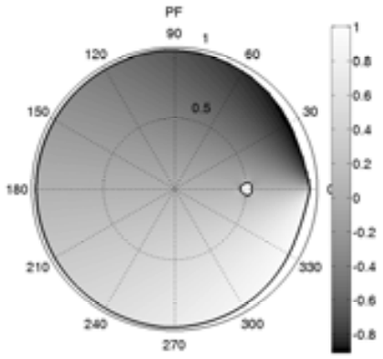

Fig. 47. Power factor under unbalanced voltage supply (L = 10 mH, R = 0.1 Ω, V_{dc} = 600 V).

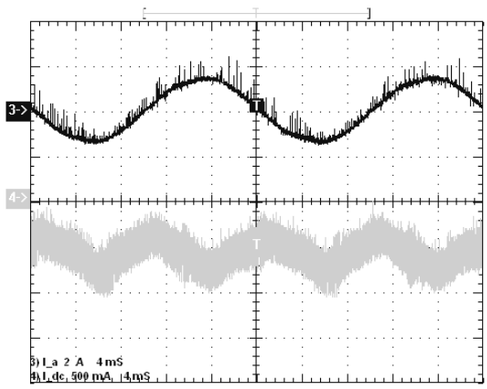

Fig. 48. Phase A current and DC-link current under unbalanced voltage supply without elimination of pulsating component.

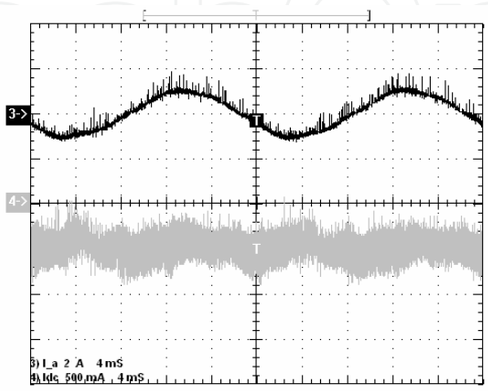

Fig. 49. Phase A current and DC-link current under unbalanced voltage supply with elimination of pulsating component.

7. Conclusion

It has been shown in the article that it is possible to effectively compensate for the unbalanced voltage source at the input of a solid-state converter so that constant power flow into the DC bus is maintained. The results of simulations show that the choice of the operating point of front end converter may significantly affect the impact of the rectifier on the supplying power grid. It is possible to select the optimal operating point according to the chosen optimization criteria, which can be e.g. maximal power factor or current unbalance.

8. Acknowledgment

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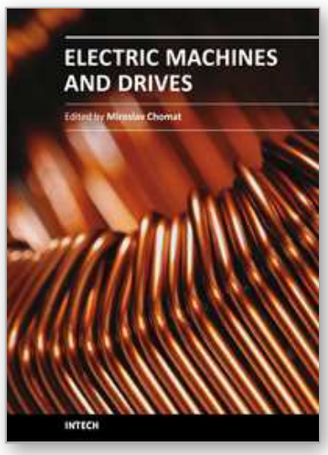

Electric Machines and Drives

Edited by Dr. Miroslav Chomat

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The subject of this book is an important and diverse field of electric machines and drives. The twelve chapters of the book written by renowned authors, both academics and practitioners, cover a large part of the field of electric machines and drives. Various types of electric machines, including three-phase and single-phase induction machines or doubly fed machines, are addressed. Most of the chapters focus on modern control methods of induction-machine drives, such as vector and direct torque control. Among others, the book addresses sensorless control techniques, modulation strategies, parameter identification, artificial intelligence, operation under harsh or failure conditions, and modelling of electric or magnetic quantities in electric machines. Several chapters give an insight into the problem of minimizing losses in electric machines and increasing the overall energy efficiency of electric drives.

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