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Tunable Analog and Reconfigurable Digital Circuits with Nanoscale DG-MOSFETs

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1. Introduction

1.1 CMOS downscaling to DG-MOSFETs

As device scaling aggressively continues down to sub-32nm scale, MOSFETs built on Silicon on Insulator (SOI) substrates with ultra-thin channels and precisely engineered source/drain contacts are required to replace conventional bulk devices (Celler & Cristoloveanu, 2009). Such SOI MOSFETs are built on top of an insulation (SiO_2) layer, reducing the coupling capacitance between the channel and the substrate as compared to the bulk CMOS. The other advantages of an SOI MOSFET include higher current drive and higher speed, since doping-free channels lead to higher carrier mobility. Additionally, the thin body minimizes the current leakage from the source to drain as well as to the substrate, which makes the SOI MOSFET a highly desirable device applicable for high-speed and low-power applications. However, even these redeeming features are not expected to provide extended lifetime for the conventional MOSFET scaling below 22nm and more dramatic changes to device geometry, gate electrostatics and channel material are required. Such extensive changes are best introduced gradually, however, especially when it comes to new materials. It is the focus on 3D transistor geometry and electrostatic design, rather than novel materials, that make the multi-gate MOSFETs as one of the most suitable candidates for the next phase of evolution in Si MOSFET technology (Skotnicki et al., 2005; Amara & Olivier, 2009).

The multi-gate MOSFET architectures can efficiently control the channel from multiple sides of the channel instead of the top-side in planar bulk MOSFETs. The ability to alter channel potential by multiple gates (i.e double, triple, surround) provides a relatively easier and robust way to control the channel electrostatics, reducing the short channel effects and leakage concerns considerably. Thus, the last decade has witnessed a frenzy of design activity to evaluate, compare and optimize various multi-gate geometries, mostly from the digital CMOS viewpoint (Skotnicki et al., 2005). While this effort is still ongoing, the purpose of the present chapter is to underline and exemplify the massive increase in the headroom for CMOS nanocircuit engineering, especially at the mixed-signal systems, when the conventional MOSFET architecture is augmented with one extra gate. Being the simpler and relatively easier to fabricate among the multigate MOSFET structures (FinFET, MIGFet, Π-MOSFET and so on) the double gate (DG) MOSFET is chosen here to explore these new circuit possibilities.

The great potential of DG-MOSFETs for new directions in circuit engineering has been explored also by others. For instance the Purdue group, led by Roy (Roy et al., 2009) has explored the impact of DG-MOSFETs (specifically in FinFET device architecture) for power reduction in digital systems and for new SRAM designs. Kursun (Wisconsin & Hong Kong) has illustrated similar power/area gains in sequential and domino-logic circuits (Tawfik & Kursun, 2008). Several French groups have recently provided a very comprehensive review of their DG-MOSFET device and circuit works in a single book (Amara & Olivier, 2009). Their works contain both simulation and practical implementation examples, similar to the work carried out by the AIST XMOS initiative in Japan (AIST, 2006) as well as a unique DG-MOSFET implementation named FlexFET by the ASI Inc.(ASI, 2009).

1.2 Context: Mixed-Signal & Adaptive Systems

In addition to features essential for digital CMOS scaling (Skotnicki et al., 2005; Mathew et al., 2002) such as the higher I_{ON}/I_{OFF} ratio and better short channel performance, DG-MOSFETs possess architectural features also helpful for the design of massively integrated mixed-signal and adaptive systems with minimal overhead to the fabrication sequence. Given the fact that they are designed for sub-22nm technology nodes, the DG MOSFETs can effectively handle GHz modulation, making them relevant for the mixed-signal system-on-chip applications with wireless/RF connectivity and giga-scale integration. Also, they have reduced cross-talk and better isolation provided naturally by the SOI substrate, multi-finger gates, low parasitics and scalability. However, the DG-MOSFET's potential for facilitating mixed-signal and adaptive system design is highest when the two gates are driven with independent signals (Pei & Kan, 2004; Raskin et al., 2006). It is the independently-driven mode of operation that furnishes DG MOSFET with a unique capability to alter the front gate threshold via the back gate bias. This in turn leads to:

- Increased operational capability out of a given set of devices and circuits.

- Reduction of parasitics and layout area in tunable or reconfigurable circuits

- Higher speed operation and/or lower power consumption with respect to the equivalent conventional circuits.

On the digital end, gate-level tunability of DG-MOSFETs allow us to explore reconfigurable logic architectures that can increase functionality and flexibility of logic blocks such as ALU and programable arrays without significant overheads in terms of size, power or design complexity. As a result, the DG-CMOS circuitry has gained steady and growing attention for mixed-signal community in the last 5 years. Many works that utilizes DG-MOSFETs in RF amplification and mixing applications (Reddy et al., 2005; Mathew et al., 2004), in tunable analog circuit blocks, Schmitt triggers, filters have been already published (Kaya et al., 2007). This chapter reviews some of these efficient and compact mixed-signal system blocks, exploring their feasibility and capabilities. At a time when performance gains resulting from circuit engineering is desperately needed to mitigate the impasse of aggressive device scaling, this is believed to be timely and very useful.

1.3 DG-MOSFET structure

DG-MOSFETs considered in this work are chosen to comply with the mixed-signal circuit design constraints that integrate analog circuits on the same substrate as digital building
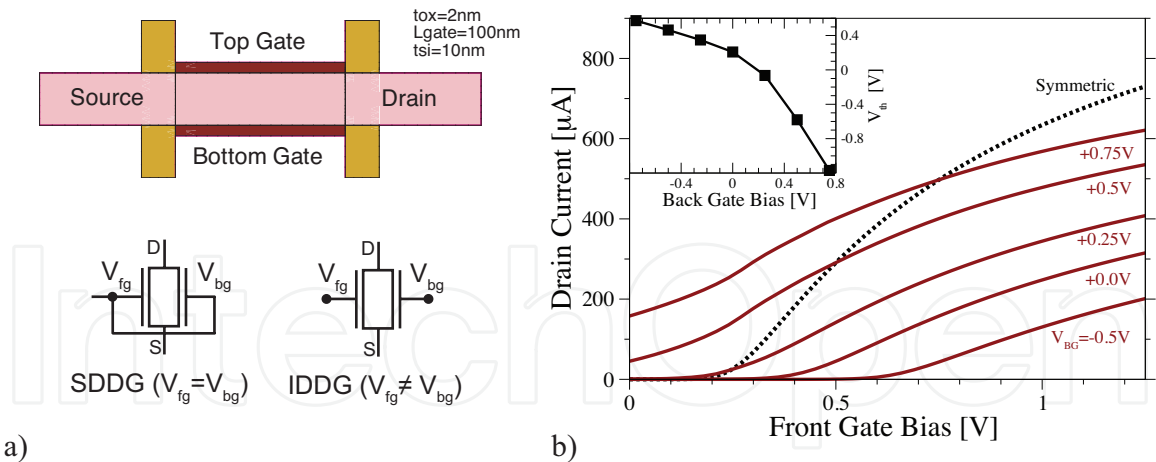
Fig. 1. a) The DG-MOSFET device structure used in this work and its circuit symbols for SDDG and IDDG modes, b) simulated characteristics of an n-type DG-MOSFET at different back-gate bias conditions. For comparison, symmetric ($V_{fg}=V_{bg}$) drive case is also included. Inset shows the resulting shift in the front gate threshold

blocks with minimal overhead to the fabrication sequence (Raskin et al., 2006; Kranti et al., 2004). This implies using DG-MOSFETs with a minimal body thickness ($t_{Si} \leqslant 20$nm), oxide insulator thickness ($t_{ox} \leqslant 2$nm) and gate length (L $\geqslant 20$nm), and maximum I_{ON}/I_{OFF} ratio optimized normally for minimum switching delay power product. It is assumed that both gates have been optimized for symmetrical threshold $V_T = \pm 0.25$V using a dual-metal process.

Fig.1a above illustrates the generic DG-MOSFET structure used in 2D simulations of all devices and circuits. The device simulations in this work are accomplished using either TCAD (DESSIS (Synopsys, 2008)) or UFDG-SPICE3 (Fossum, 2004) simulators in drift-diffusion approximation for carrier transport, which is sufficient for low-power circuit-configurations explored here. The transfer (I_D-V_G) characteristics of a generic n-type DG-MOSFET simulated using DESSIS is also available in Fig.1b. It is obvious that the top-gate threshold can be tuned via the applied back-gate voltage. This 'dynamic' threshold control is crucial to appreciate the tunable properties of the circuit structures presented here. However, such independently driven double gate (IDDG) devices have lower transconductance, and higher sub-threshold slope than the symmetrically driven double gate (SDDG) counterparts under equal geometry and bias conditions (Pei & Kan, 2004). Thus bottom-gate tunability comes with a reduction in intrinsic DG-MOSFET performance, a price well justified by the wide variety of circuit possibilities as explored below.

2. DG CMOS modeling & simulation

The last ten years have witnessed a sizable effort in migrating conventional compact models to more sophisticated but numerically demanding novel approaches based on the surface-potential. Such a move was inevitable given the aggressively scaled dimensions and new physics such as tunneling and quantization effects that must be accounted for accurately. Yet, there is no public-domain surface-potenial based DG-CMOS SPICE models that can be accessible to the circuit and system engineers in terms of availability and usability. As a result, we adapted using two commercial modeling approaches successfully to simulate the DG-CMOS circuits, which are detailed below.

2.1 UFDG SPICE

The UFDG model is a process/physics and charge based compact model for generic DG MOSFETs (Fossum, 2004). The key parameters are related directly to the device physics. This model is a compact parameterized Poisson-Schrodinger solver for DG MOSFETs that physically accounts for the charge coupling between the front and the back gates. The UFDG allows operation in the independent gate mode and is applicable to fully-depleted SOI MOSFETs. The quantum mechanical (QM) modeling of the carrier confinement, dependent on the ultra-thin body (t_{Si}) as well as transverse electric field, is incorporated via Newton Raphson iterations that link it to the classical formalism. The dependence of carrier mobility on t_{Si} on transverse electric field is also accounted for. In addition, the carrier velocity overshoot and dependence on carrier temperature is characterized in the UFDG transport modeling to account for the ballistic and quasiballistic transport in scaled DG MOSFETS (Ge et al., 2001). The channel current is limited by the thermal injection velocity at the source, which is modeled based on the QM simulation. The UFDG model also accounts for the parasitic (coupled) BJT (current and charge) which can be driven by transient body charging current (due to capacitive coupling) and/or thermal generation (Kim, 2001). Lumped source and drain contact resistances, gate-induced barrier lowering and impact ionization currents are also considered, the latter of which is characterized by a non-local carrier temperature-dependent model for the ionization rate integrated across the channel and the drain. The charge modeling which is patterned after that is physically linked to the channel-current modeling. All terminal charges and their derivatives are continuous for all bias conditions, as are all currents and their derivatives. Temperature dependence for the intrinsic device characteristics and associated model parameters are also implemented without the need for any additional parameters. This temperature dependence modeling is the basis for the self-heating option, which iteratively solves for local device temperature in DC and transient simulations in accord with a user defined thermal impedance. Hence UFDG model has sufficient rigor to accurately model sub-100 nm devices commonly used for in the proposed circuits.

2.2 TCAD

A secondary approach adapted in our simulations is the use of technology CAD (TCAD) package by Synopsys (Synopsys, 2008), which can solve the appropriately coupled set of electron/hole transport equations and electrostatic (Poission) equation over realistic 2D/3D meshes. In TCAD no mathematical models are assumed for the terminal characteristics and a precise device geometry can be accounted for to estimate the outcome of semiconductor processing technologies and device characteristics. The TCAD device simulation tools are applicable to a broad range of applications including Analog/RF devices and can be used as an aid to gain insight to device performance and operation.

In the two-tiered TCAD packages, the process simulator deals with geometrical modeling of the fabrication steps of semiconductor devices such as transistors and diodes. On the other hand, the device simulator simulates the electrical characteristics of the devices, in response to the external electrical, thermal or optical boundary conditions imposed on the structure. Figs.1 & 2 shows the I_d-V_{fg} characteristics at different back-gate bias conditions for an n-channel MOSFET an a DG-CMOS pair, respectively, as obtained from so-called mixed-mode TCAD simulations that include multiple instances of devices in an outer SPICE-like network solver. Due to the multiple transistors each containing upwards of 2000 mesh points and the
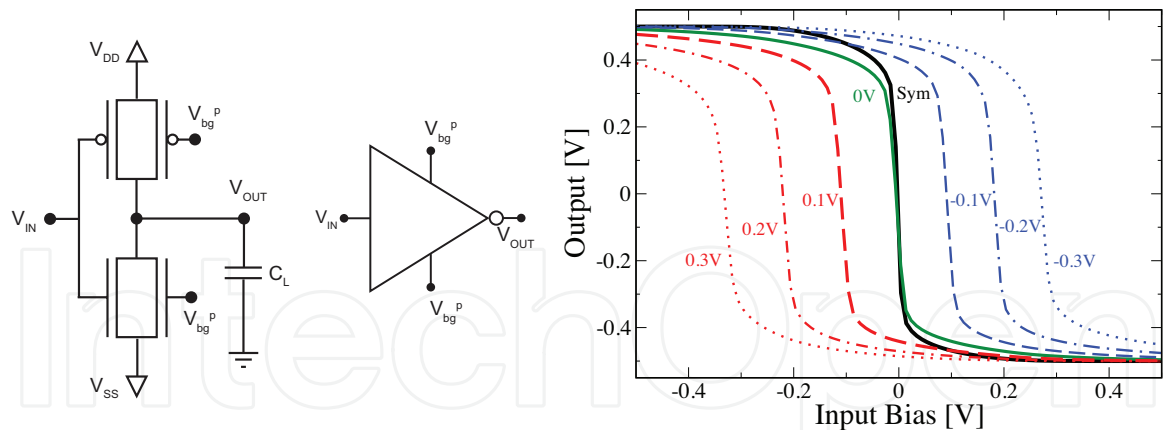
Fig. 2. a) The simple inverter implemented using the DG MOSFETs with additional inputs for tuning transfer characteristics b) TCAD simulated DC transfer characteristics when the two back gates are biased jointly (V_{bg}^n = -V_{bg}^p).

bipolar charge transport in each device these simulations are CPU intensive and require rather large memory space. This situation is further compounded when the quantum mechanical corrections and sophisticated dependence of mobility on parallel and perpendicular fields. Therefore the TCAD approach must be carefully considered in large circuits and may be only needed where accuracy is the prime concern.

3. Analog circuits blocks

In the following we provide examples for compact & low-power RF-CMOS system blocks designed using independent gate DG-MOSFETs. In all cases, the bottom gate is used to tune the circuit performance while also reducing overall system size (number of transistor and total area). Many integrated signal processing platforms can use these system blocks to process the signals from receivers and nanosensors. Using simulations, we explore how compact low-power circuits including tunable single-ended and differential amplifiers, integrators, filters and current and voltage controlled-oscillators may be built and tuned. Depending on the nature of nanosensing devices and S/N ratio, more custom solutions may always be possible.

3.1 CMOS voltage amplifier

The DG CMOS inverter pair (see Fig.2) can serve as a high-gain push-pull amplifier when biased in the transition region. Depending on the selection of the sign and magnitude of the bottom-gate bias, the simple amplifier's characteristics can be altered in a number of ways, which greatly enhances the variety of applications for this otherwise simple circuit. For instance, Fig.2b shows that co-setting of the bottom gates at the same voltage (V_{bg}^n = V_{bg}^p) results in proportional shifts in the voltage window for amplification. This "window-shifting" can be conveniently utilized in a number of ways such as in analog wave-shaping circuits sensitive to DC bias levels or in Schmitt triggers (Kaya et al., 2007; Cakici et al., 2003). An alternative scheme for programming the CMOS pair is conjugation, whereby the two complementary bottom-gates are driven by separate signals of equal magnitude but opposite polarity, i.e V_{bg}^n = - V_{bg}^p. In a mixed-mode design using bipolar supply voltages, this biasing scheme is indeed possible and provides a method of varying the amplifier gain. As shown
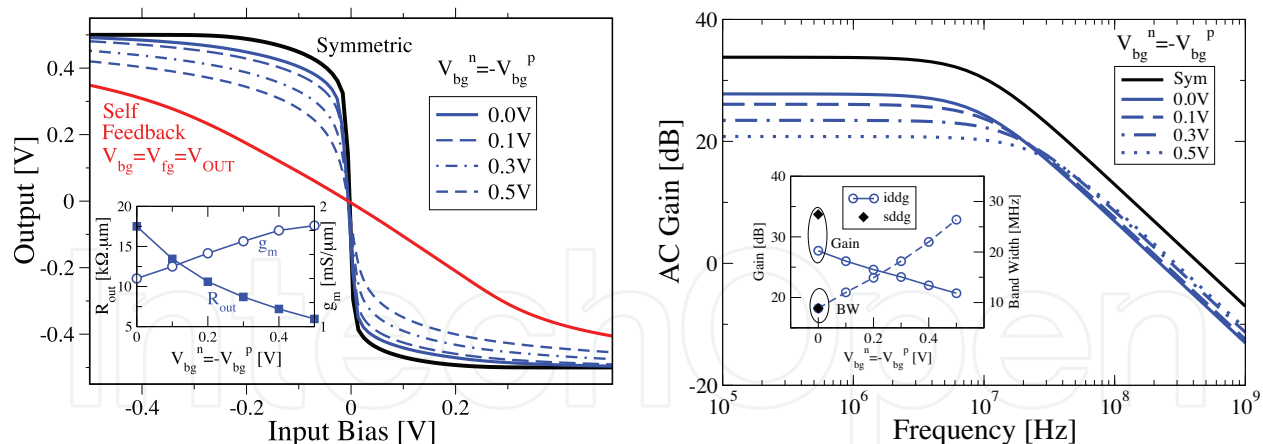
Fig. 3. a) The simulated DC response of the tunable DG-CMOS pair for various joint back gate biases (V_{bg}^{n} = -V_{bg}^{p}). The amplifier gain changes with the back gate bias and b) AC gain analysis

in Fig.3a, the slope (gain) of the transition region is a function of conjugate bias levels set on the bottom gates and the change in the output impedance (inset, R_{out}=1/g_d) dominates the simulated intrinsic gain (g_m/g_d) response. For comparison, the output of SDDG CMOS pair is also provided in the both plots above. While the gain of SDDG inverter is higher, without any bias control, it offers neither design latitude nor alternative configurations. On the other hand, the self-feedback arrangement also included in Fig.3a, where the output of the IDDG CMOS pair drives their bottom-gates (V_{bg}^{n} = V_{bg}^{p} = V_{OUT}), results in a inverting buffer with a gain of one. This may be especially suitable in applications where a linear signal buffer is required. The gain-bandwidth tradeoff of the IDDG-CMOS amplifier is illustrated in Fig.3b, which shows the outcome of AC analysis with a load capacitor of C_L =1 pF. Thus, it should be possible to fine tune simple CMOS amplifier's frequency response using the conjugate biasing scheme in a very linear fashion.

3.2 Current mirrors

Another essential block used in the design of analog circuitry is the simple current mirror. Normally the current copying characteristics of the simple current mirror (CM) (Fig.4a), is fixed once the circuit is built and depends on the ratio of transistor width between the input (reference) and output branch. In the case of DG-CMOS, however, a similar gain factor can be easily obtained, and dynamically altered, by appropriate back biases of DG-MOSFETs used in the mirror block, as shown in Fig.4b. The back bias can modulate overall conductivity of the output transistor, thus effecting the copying ratio. Such tunability not only greatly enhances the variety of applications for this otherwise simple circuit, but could also lead to area and/or power savings over similar circuits built using bulk MOSFETs, as also discussed by others (Kumar et al., 2004)

Even for the modest back-bias conditions at the output transistor (V_{set}^{o} ⩽ 1 V), it is possible to achieve mirror ratios around 100. Note that poor output impedance of the simple CM is due to short gate length (⩽ 100nm) devices employed here. Such compromise in the output conductance can be easily dealt with by adapting a cascade CM, as shown in Fig.4c. The cascade CM design retains all aspects of tuning in the simple CM, while increasing the output impedance of the CM (Fig.4d). Once again, the above simulations not only show the great potential in Independently Driven Double Gate (IDDG) tunable current mirrors but also
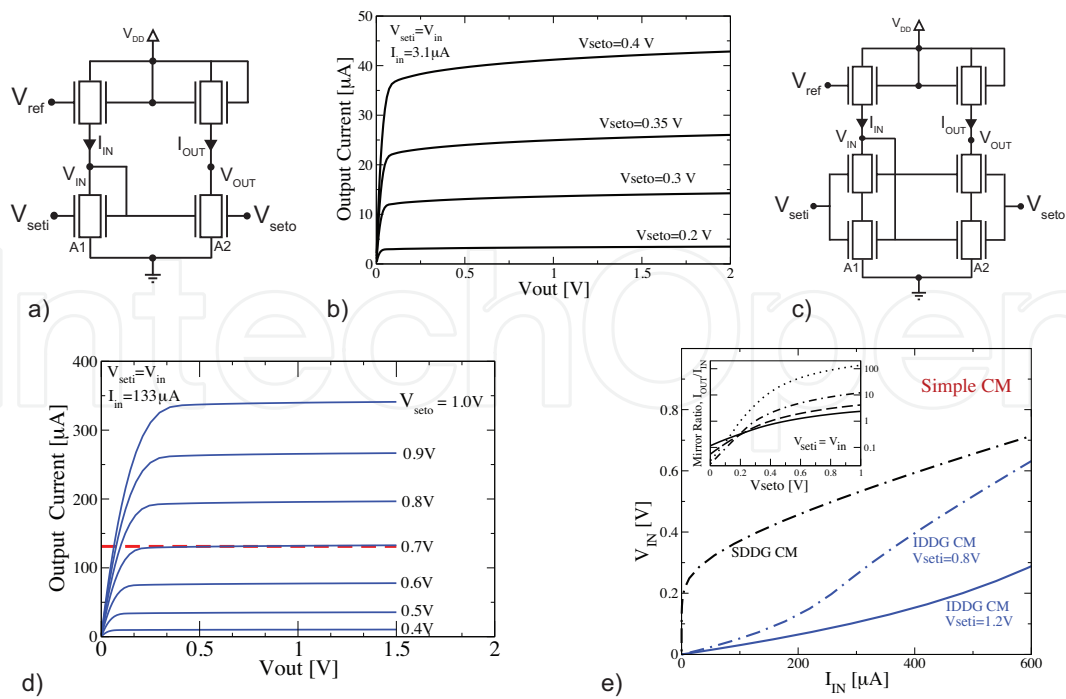
Fig. 4. a) simple DG current mirror and b) the simulated output I-V response as a function of tuning voltage V_{set}^o. The output impedance is low due to short channel effects c) The improved DG cascade current mirror d) The dependence of the I-V response of the cascade current mirror on V_{set}^o. e) Comparison of the required voltage across the input of the simple CM in three configurations: SDDG (no back gate control) and IDDG with two different back gate voltages

provide valuable insights for the more complicated current-mode circuits blocks investigated in the following sections, which uses a number of such CM in a differential topology to form amplifiers, filters and alike. Moreover, comparison at the same current levels shows that the input voltage across DG current mirror can be significantly lower than that required for conventional version (Fig.4d). Therefore, in addition to the tunability without the use of an extra transistor (less area and parasitics), another major advantage of DG CM circuits is the potential to lower voltage supply and power dissipation (lower V_{IN}).

3.3 Current amplifier
The dynamic alteration of mirror ratios is the principle of amplification behind the simple but tunable current amplifier in Fig.5a, which can also be built using the cascade CM for higher performance. The proposed current amplifier is built using a two-stage design consisting of an amplification (A1:A2) block and an DC offset cancellation blocs (A2:A2). Without the error cancellation stage this differential block would still operate but can result in DC offset errors in driving similar differential blocks. Both of these blocks are built using DG CMs: the back gates of lower transistor pairs (V_{seto}) are used for scaling the output current, while the back gates of input transistors (V_{seti}) are used for scaling the input current. PMOS transistors bias the amplifier to a DC operating point, which can be controlled also using the back-gate V_b.
It is possible to achieve appreciable gain and bandwidth programming in various biasing schemes for the bottom-gate control voltages on the input and output sides (V_{seti}, V_{seto}), as shown in Fig.5a. Our simulations indicate that the bandwidth can be easily tuned by two orders of magnitude and the gain by 15 dB using this amplifier. Moreover, by combining
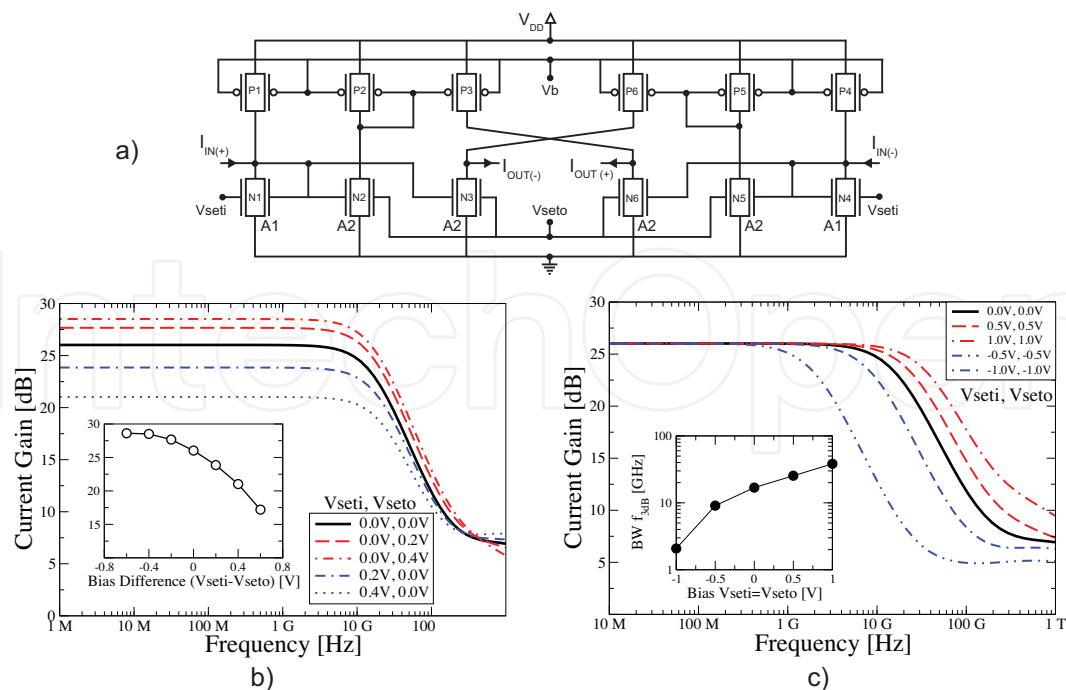
Fig. 5. a) Current amplifier circuit implemented using simple DG CM components, b) the gain control and c) bandwidth control in current amplifier via asymmetric and symmetric biasing schemes, respectively.

these biasing schemes, it should be possible to concurrently tune the gain and bandwidth in the same amplifier. Once again, this is achieved without the use of extra transistors found in conventional tunable CMOS circuits, thus, in principle, reducing the area and power requirements considerably. Moreover, this current amplifier may be realized also in the single-ended fashion, i.e. a single CM stage, which can be used as a sense amplifier with a tunable frequency response that can be very useful in nanosensor environments with a cluttered spectrum.

3.4 Operational Transconductance Amplifiers - OTA
Operational transconductance amplifiers (OTA) produce differential output currents in response to differential voltage inputs. They have become increasingly popular in the last two decades due to ease of design and reduction in circuit complexity compared to operational voltage amplifiers in certain applications (Sanchez-Sinencio & Silva-Martinez, 2000). They often drive a capacitive load in a compact OTA-C block that can act as very efficient integrators and appear also in other filter elements. Since the back-gate biasing in DG-CMOS architecture offers real advantages to current mode circuit design to alter circuit operation with minimal intrusion, the OTAs with current outputs are set best for taking advantage of the tunability in amplifier designs. Accordingly, we focus below in two different OTA circuits.

3.4.1 Simple OTA
The first OTA topology explored is the simplest of all, as illustrated in Fig.6a, which is adapted from bulk MOSFET implementation normally requiring 6 transistors (Szczepanski et al., 2004), as opposed to 4 DG-MOSFETs in the new topology. The availability of the individual bottom gates allows the elimination of the two extra transistors for transconductance (g_m) tuning
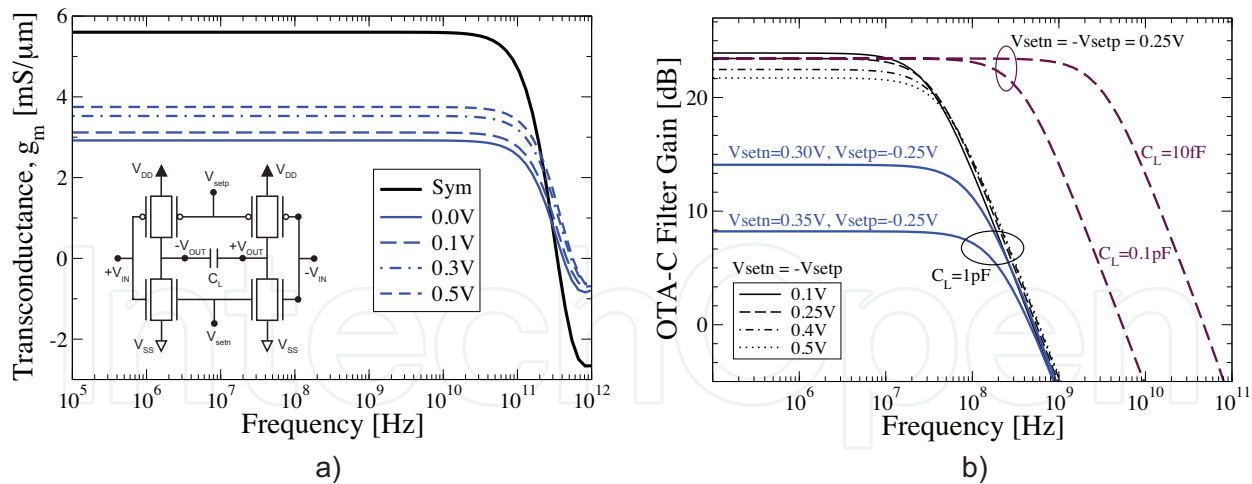
Fig. 6. a) Transconductance (g_m) of the unloaded (C_L=0) OTA circuit (inset) versus frequency as a function of the conjugate tuning bias. g_m has a linear dependence on the bias setting and does not trade-off with the bandwidth b) AC gain of OTA-C filter at various bias settings and for three capacitance values. For a typical C = 10 fF, GHz operation is within reach. Although gain can be tuned using conjugate bias pairs, a wider tuning range is possible via asymmetric bias ($V_{setn} \neq V_{setp}$)

across the two branches of the OTA, which should save both power and area while also minimizing the parasitics.

Similar to the CMOS amplifier case, there are two tuning schemes available to this simple OTA circuit: an asymmetric bias ($V_{set}^p \neq V_{set}^n$) to shift frequency response or a conjugate bias ($V_{set}^p = -V_{set}^n$) to alter the transconductance (g_m) of OTA. Fig.6a summarizes this latter case, where the frequency dependence of g_m on the conjugate programming voltage is plotted against frequency. The most important figure of merit, g_m, of OTA varies linearly with the programming voltage and the bandwidth (BW) of the OTA is constant despite varying g_m, which is one of the main hallmarks of OTAs (Sanchez-Sinencio & Silva-Martinez, 2000). The g_m is constant up-to ~ 100 GHz range limited by small parasitic capacitances on SOI substrate. When an asymmetric bias is used to tune the OTA, we can conveniently shift the frequency response. For a fixed realistic load of C_L = 10 fF and $V_{set}^p = -V_{set}^n$=0.25V, the resulting OTA-C circuit serves as a low-pass filter with a corner frequency $\sim$5 GHz, as shown in Fig.6b. Even for a relatively large load of C_L = 1 pF, the filter pass-band extends up to 200 MHz. The same corner frequency can be tuned almost a decade depending on the asymmetric bias on the back gates. This simple but powerful example aptly illustrates the potential of DG-MOSFET analog circuits.

3.4.2 VHF OTA

Practical implementation of high-performance tunable OTAs requires more sophisticated architectural elements that optimize the gain as well as the input and output impedance. Such elements modify the transfer function by canceling poles and shifting zeros in the complex plane to improve frequency performance and/or stability. However, a detailed account of DG-CMOS OTA optimization is beyond the scope of this chapter. Instead, we shall attempt to illustrate that improvements to the simple OTA structure above is indeed possible. For instance, a more advanced version of the simple OTA circuit with cross feed-forward elements intended to improve the output conductance is presented in Fig.7a. There are two sets of tuning nodes in this circuit: the input side with nodes V_{CpI}, V_{CnI} and the load side with
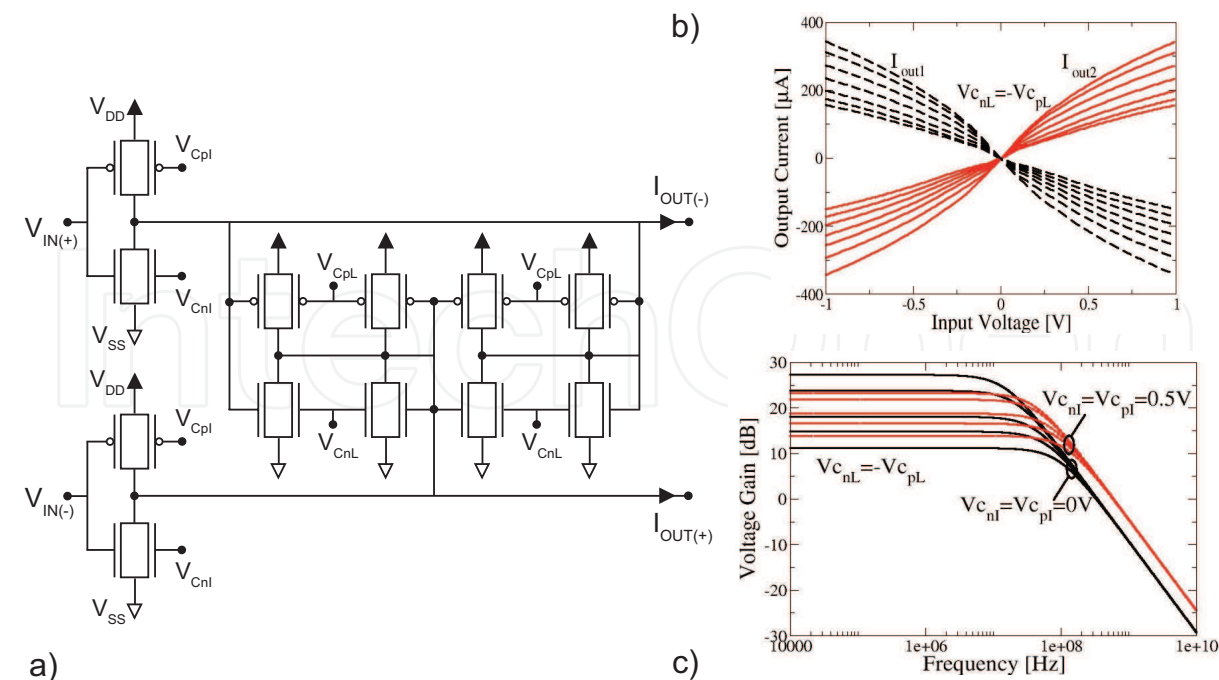
Fig. 7. a) A tunable operational transconductor amplifier (OTA) based on simple DG-MOSFET inverters with feedforward compensators. b) The simulated response of the differential OTA as a function of conjugate bias $V_{CpL}=-V_{CnL}$ at feedforward structure, and c) the AC characteristics of a simple $g_m - C$ integrator with $C_L = 1\ pF$ as a function various values of control bias $V_{CpL}=-V_{CnL}$ for two cases of $V_{CpI}=V_{CnI}$ 0 and 0.5 V.

V_{CpL}, V_{CnL}. The former mostly impacts the transconductance term, while the later determines the output conductance (Nauat, 1992). Normally, all control nodes are held at 0.0V, unless otherwise noted, and the conjugate bias pairs may be varied. The resulting architecture operates linearly up to large values (500mV or higher) of the input signal amplitude and the g_m (i.e. the slope) can be tuned using voltages V_{CpL}, V_{CnL}, as evident in Fig.7b.

The ability to tune the transconductance can be readily utilized in a variety of applications such as the C-g_m integrator shown in Fig.7c. A fairly large capacitor value of C=1 pF was used in this circuit. The BW of the integrator can be tuned by the control nodes V_{CpI}, V_{CnI} as well as the capacitor value, while the gain can be determined by the nodes V_{CpL}, V_{CnL}. In comparison with the simple OTA (Fig.6a), the unloaded (C_L=0) bandwidth of the VHF OTA structure is found to improve by an order of magnitude, which compares well with the bulk CMOS implementation (Nauat, 1992) as well as the loaded data (C=1 pF) in Fig.7c. A SDDG version could operate at much higher frequencies, although it would require more power and area, as discussed in the previous section. We also observe that the tuning range of DG-CMOS OTA circuit is more limited than the current mode integrator, a point to be discussed in more detail in the next section.

3.5 Current-Mode Integrator and High-Order Filters

To illustrate the power of the simple DG circuit blocks and address another important building block used in almost all analog RF systems, this section is dedicated to examples of first and second order filters. Hierarchically as well as pedagogically, it is appropriate to start the discussion with first-order tunable integrators, which can then be used to build higher-order
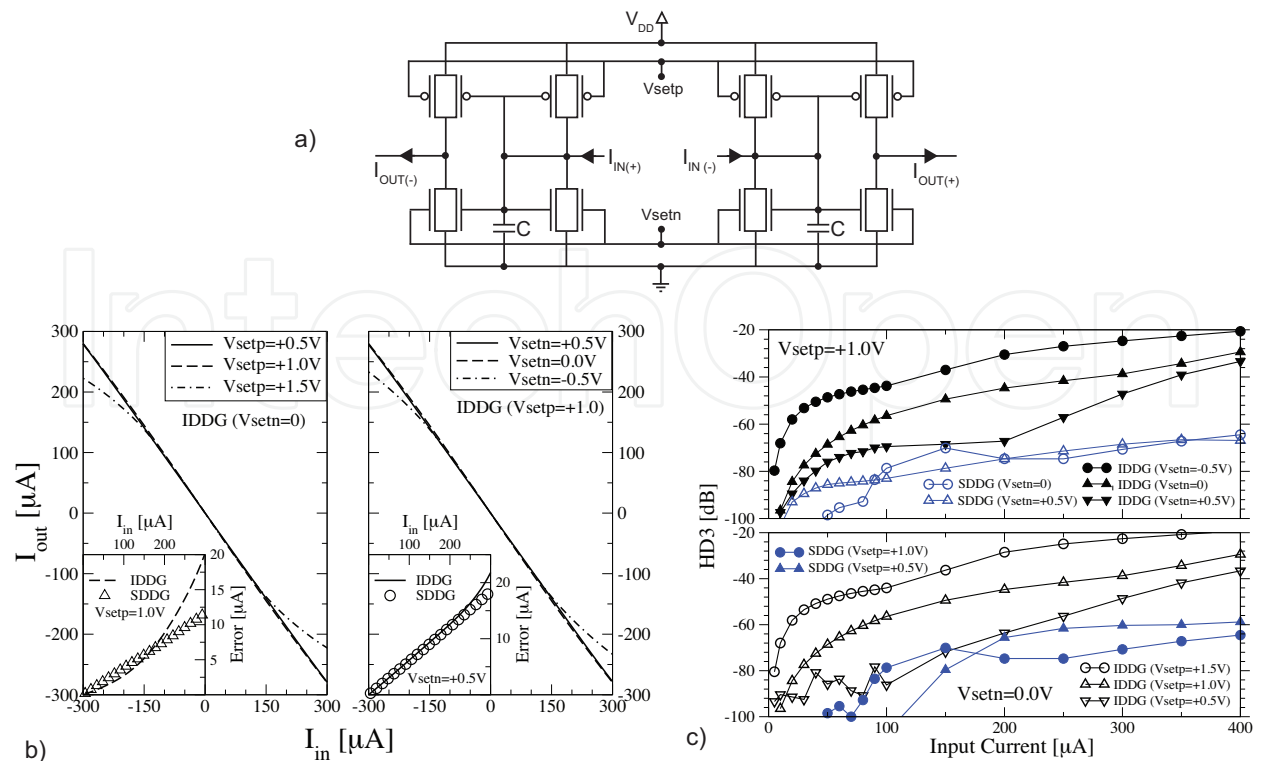
Fig. 8. a) A differential current-mode integrator implemented using only eight IDDG MOSFETs and two capacitors C. b) Simulated DC transfer characteristics of the integrator for various Vsetp (Vsetn=0V), and Vsetn (Vsetp=1.0V) values. The tuning is achieved by either the top (V_{setp}) or the bottom (V_{setn}) half of the circuit, without causing any DC offsets. Its impact on the linearity (inset) is only slightly below the SDDG performance at identical conditions. c) The third-order harmonic distortion (HD3) is a strong function of the tuning voltage in IDDG integrator. Even though it is below in down-tuning conditions, for up-tuning configurations (Vsetn>0 or Vsetp<1) the HD3 figures of IDDG design are quite comparable to that of SDDG.

examples. Although there are many options and transfer function choices, again, we focus on current mode integrators that can fully take advantage of DG-CMOS architecture.

As the first example, a current-mode integrator proposed in (Karsilayan & Tan, 1995) is implemented using IDDG MOSFETs, as shown in Fig.8a. This design eliminates the additional output blocks used in tunable bulk CMOS equivalent, reducing the transistor count from 16 to 8. Halving the number of transistors not only reduces the silicon layout area, but it can also translate to reduction in power consumption and transistor parasitics, all of which are crucial considerations in integrated RF systems (Kaya et al., 2009). In the present circuit, each parallel pMOSFET pair have been realized with a single p-type DG-MOSFET with twice the width of the n-type devices, i.e. $(W/L)_n$=10 and $(W/L)_p$=20. In the conventional circuits used for comparison, every IDDG-MOSFET is replaced with twin SDDG or bulk CMOS transistors in parallel. The conventional CMOS transistors used for this purpose have identical gate stack as the DG-MOSFETs but 3 times deeper (30nm) junctions typically found in bulk Si technology.

The proposed integrator circuit is essentially composed of two balanced current-mirror blocks, clamped together at the center nodes, and an input capacitor. The input current offsets the balance between the n-type and p-type branches by (dis)charging the center node higher (lower), resulting in a net deficit (excess) current at the output node. To facilitate tunability, the back-gates all of n-type (p-type) DG-MOSFETs are tied together to a voltage V_{setn} (V_{setp}).
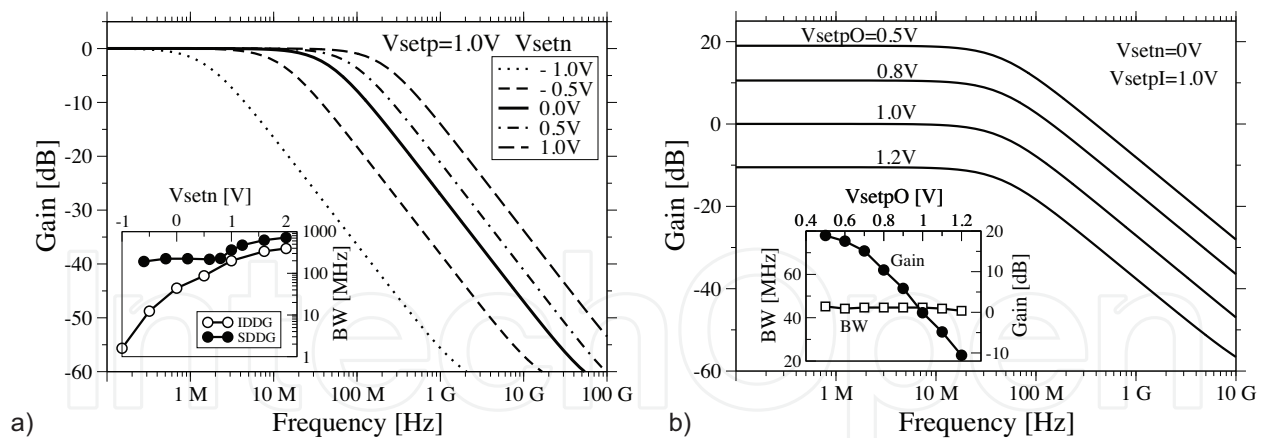
Fig. 9. a) Simulated BW of the balanced integrator for C=1pF. The inset shows the extracted tuning range for the same figures in the SDDG and IDDG cases b) Simulated gain tuning of the integrator for C=1.0pF. The inset shows there is no trade-off between the BW and the gain in this current-mode circuit.

The tuning of the integrator can be accomplished either by adjusting voltage V_{setn} for a fixed $V_{setp}=V_{DD}=1.0V$ or by setting V_{setp} while V_{setn} is grounded. The integrator can also be tuned by concurrently setting the V_{setn} and V_{setp}.

Overall, the integrator circuit is found to have very good linearity and an impressive tuning performance, indicated by the DC transfer data in Fig.8b. The unique feature of this circuit is the common node between the upper and lower CM blocks, which prevents the development of DC offsets by the concurrent modulation of these blocks by the input capacitance C. The lack of DC offset at the output which often plague such tunable circuits (Sedighi & Bakhtiar, 2007; Zeki et al., 2001) is a distinguishing characteristic of this circuit.

Using the integral function method developed by Cardeira and co workers (Cerdeira et al., 2004), it is possible to analyze the same DC transfer curves to calculate total harmonic distortion as well as the 3rd harmonic distortion (HD3) as shown in Fig.8c. Even with very large input currents we find that HD3 remains below −20dB. The linear relationship between I_{out} and I_{in} is especially impressive for $|I_{in}|<150\mu A$. For $|I_{in}|>150\mu A$, down-tuning ($V_{setn}<0.0$ and $V_{setp}>1.0V$) results in a less-linear circuit. However, at up-tuning ($V_{setn}>0.0$ and $V_{setp}<1.0V$) settings the errors in the output of IDDG circuit approaches that of the SDDG counterpart for $|I_{in}|<250\mu A$ and HD3 drops to −80 dB level. Such a wide variation in linearity performance indicates that even though IDDG-MOSFETs are intrinsically capable of matching SDDG performance for distortion, this is only possible at up-tuning that fully activate the back gates.

The AC response of the integrator (Fig.9a&b) indicates that the BW and gain can be tuned by using different but non-exclusive biasing schemes requiring only ±1V. The tuning of BW by more than two decades can be obtained via a single control node (V_{setn} or V_{setp}), whereas the gain tuning by 30dB requires the asymmetric bias of V_{setn} between the input (V_{setnI}) and output (V_{setnO}) nodes. To illustrate the superiority of this IDDG integrator over conventional counterpart, in terms of tunability, we also include in the inset of Fig.9a&b the simulated response of the SDDG integrator with twice as many transistors. Since the SDDG devices have intrinsically higher g_m and employs additional transistors for tuning it has almost twice larger BW, although with a limited tuning range. This limitation arises because the conventional tuning is limited when the parallel MOSFET shuts off below its threshold. In the case of IDDG tuning, the back gate can modulate the current in the front gate even when its own conductive
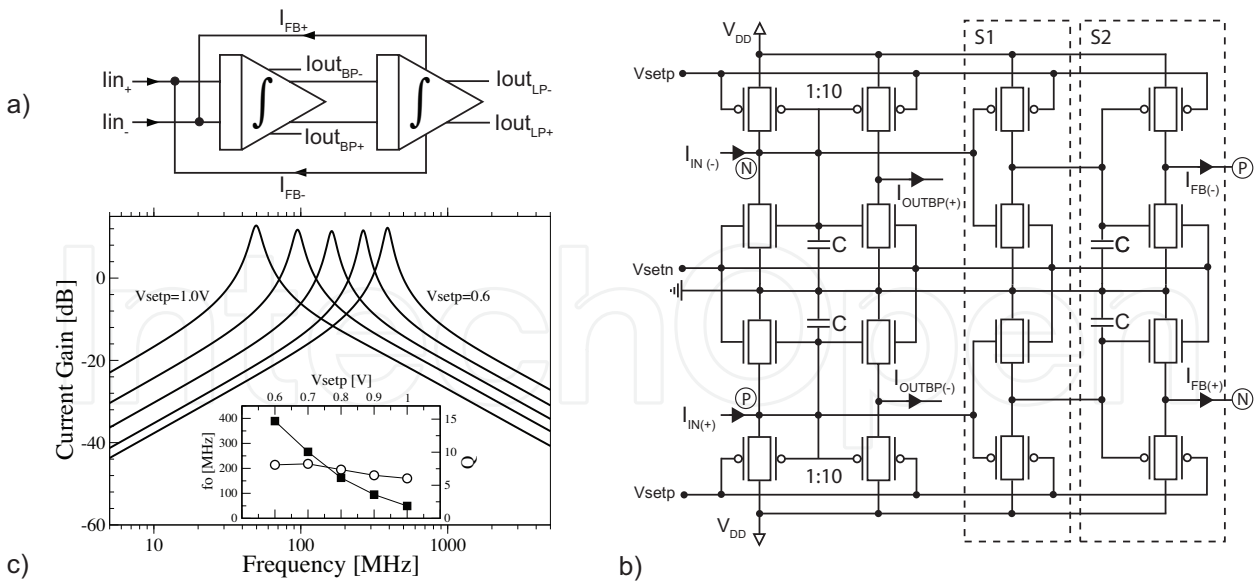
Fig. 10. a) The block diagram for the tunable current-mode 2nd order LP/BP filter using the integrator above. b) The full circuit diagram for the 2nd-order BP filter using two integrator stages. The second stage (S2) is simplified by using a simple C-g_m integrator since an LP output is not used in this case. A full LP filter would require the full integrator block in S2 but not the intermediate block S1 as BP output is redundant. A size ratio 1:10 in the 1st stage is used to generate gain. c) Simulated frequency response of the 2nd-order BP filter (C=1pF) as a function of control node V_{setp}. The filter can be tuned only using 0.5V and without impacting Q.

channel ceases. It must be pointed out that the inset in Figure 10c also shows vividly the lack of gain tradeoff in this current-mode circuit.

Two of the tunable integrators above can be employed to build a dual-response low-pass/band-pass filter. The circuit topology for this low/band-pass filter is shown in Fig.10a&b). To create a more compact design the second stage (S2) integrator is simplified by using a basic current-mode C-g_m integrator. It is sufficient to replace this stage with the full design to provide also a low-pass output. Conversely, the secondary output of the first stage (S1) may be eliminated if the band-pass output is not required. Either way, it possesses very impressive tunable characteristics, as shown in Fig.10c, BW moving over a decade just by tuning one of the control nodes, in this case V_{setp}, by half a Volt. By combining the control node for the n channel MOSFET block (V_{setn}) and extending the voltage range, it should be possible to move the center frequency further or tune the quality factor, which is weakly dependent on any one of the control signals, as shown in the inset of Fig.10c.

3.6 Oscillators

So far the oscillator circuit design has not extensively benefited from the DG-CMOS architectures as the limited number of published works concentrate on the DG implementations of known circuits. Yet the use of IDDG MOSFETs make these circuits tunable oscillators, which have a very wide and significant application potential illustrated in the examples below.

3.6.1 Voltage-Controlled Ring Oscillator (VCRO)

Normally a conventional ring-oscillator circuit has oscillation frequency fixed by the architecture and the number of inverters used. Fig.11a shows that the basic IDDG-inverter
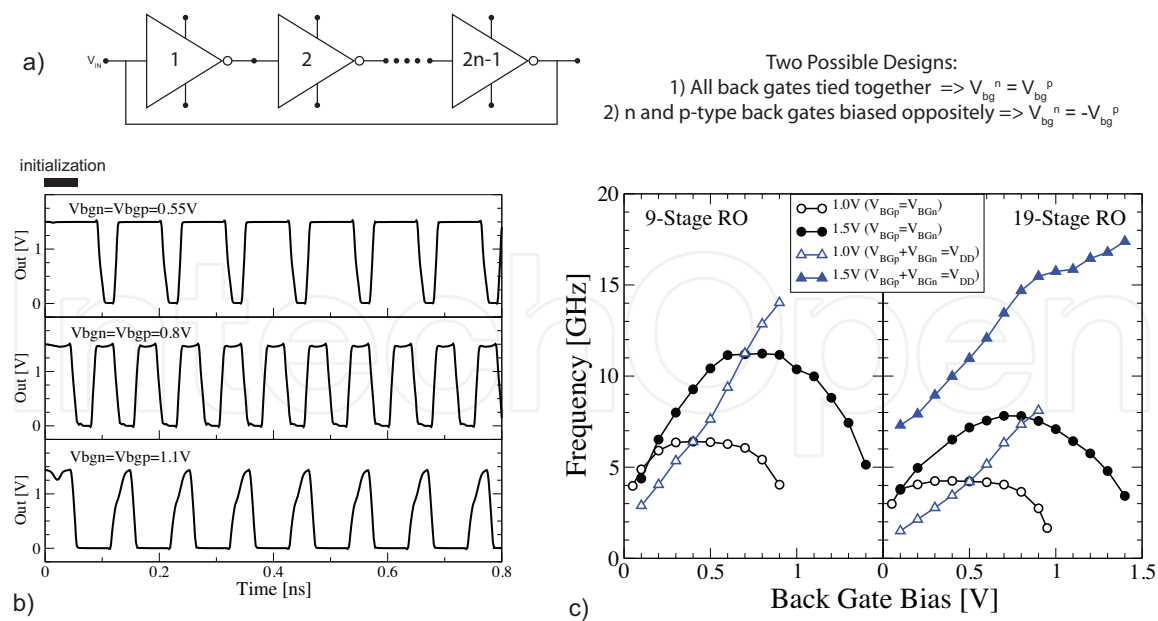
Fig. 11. a) Simple ring oscillator becomes a versatile VCO in the IDDG implementation based on back-gate biasing of inverters (L=50nm and W_p/W_n=2) b) The transient response of the VCO to various control biases when $V_{bg}^n = V_{bg}^p$ c) The proposed control characteristics of the VCO in single and dual control schemes for two different sizes of the rings

can be used to build a simple yet efficient tunable ring oscillator with two different operation modes depending on the back-gate biasing scheme used. These two modes correspond to single and differential gate control, where the back gates of n- and p-type DG-MOSFETs are either tied together ($V_{bg}^n=V_{bg}^p$) or biased oppositely ($V_{bg}^n=-V_{bg}^p$). As the two biasing schemes change the threshold or the delay of the IDDG inverters, respectively, the oscillation response becomes sensitive to the bias voltages. The transient response of a nine-stage IDDG ring VCRO is shown in Fig.11b for three cases of the control signal $V_{bg}^n=V_{bg}^p$. The typical control characteristics of the same circuit are shown in Fig.11c for two different designs (9 or 19 stages). The oscillation frequency of this VCRO is a strong, almost linear function of the applied control bias, especially in the case of differential control bias ($V_{bg}^n=-V_{bg}^p$). The two branches of tuning curve in the single bias control case ($V_{bg}^n = V_{bg}^p$) correspond to oscillations with different duty ratios ($t_{ON}/t_{OFF} > 0.5$ vs. $t_{ON}/t_{OFF} < 0.5$) for the output signal. Note that a wider tuning range is possible for larger V_{dd} values as well as longer chains of inverters, which has been kept here fairly small to minimize the simulation times (hence the GHz frequencies). A preliminary study of phase noise and jitter performance on the VCRO structure has revealed that, the proposed VCRO circuit has mediocre characteristics in terms of stability and may not be used for timing or system clock circuits. However, they will still be very attractive options for simple sensing and counting circuits as well as local oscillators in the communication circuits (Kaya & Kulkarni, 2008)

3.6.2 Current Controlled Oscillators (ICO)
For sensors producing current signals, such as found in most optoelectronic systems, it is more convenient to alter the oscillator output via a current input. The inset of Fig.12a shows the IDDG implementation of such an ICO, based on the ultra-low power RC relaxation oscillator
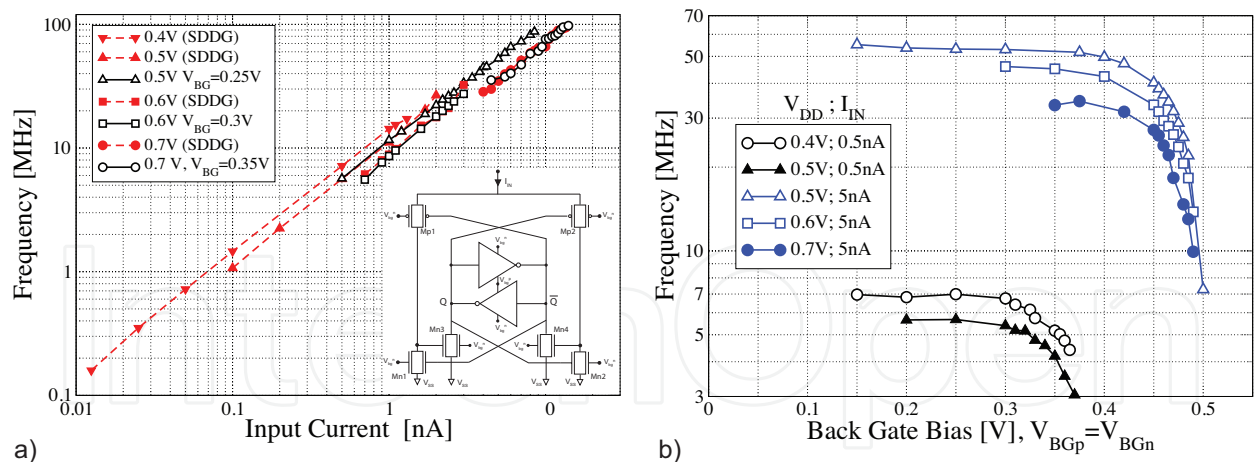
Fig. 12. a) (inset) the switched-current ICO circuit built using IDDG MOSFETs (L=50nm and W_p/W_n=2) and a latch,and its ICO response. b) The same circuit can also operate as a VCO circuit using back-gate biasing, albeit with a lower sensitivity. Note that the ICO response is extremely linear and spans for orders of magnitude even on a log-log scale

circuit proposed by (Chunyan et al., 2003). The most interesting, and also attractive, feature of this circuit is the lack of bias supply for the input block comprising two p-type MOSFETs (M_{p1},M_{p2}) and four n-type MOSFETs (M_{n1}-M_{n4}). As a whole the circuit is a switched current circuit driving a CMOS latch block at the center. The output (Q,Qb) of the latch is also the oscillator output driven by the middle nodes (drains) of the inverters M_{n1}/M_{p1} or M_{n2}/M_{p2}. For weak signals it takes much longer to (dis)charge these intermediate nodes so the latch output does not alter frequently. When it does, the same input signal is directed to the opposite branch to continue the (dis)charge operation over again and so on. Therefore the input stage does not need a steady DC current source or large voltage drops beyond a single threshold. The result is an ICO that have a very impressive sensitivity to the input current down to pA range as shown in Fig.12a, only limited in the present simulations by the numerical accuracy of the transistor models and convergence criteria. In principle sub-pA range of currents can be detected (Chunyan et al., 2003), while at the higher frequency end the circuit is only limited by the delay of the latch. Moreover the oscillations are possible at low V_{dd} values down to 0.3 V or so, depending on the DG-CMOS thresholds.

Strictly speaking, the ICO circuit above does not need a DG-CMOS for operation. However, the DG-CMOS implementation has two advantages: i) it can be used also as a VCO by virtue of the back gate bias and ii) operates more efficiently with a higher upper limit as a result of higher transconductance of DG-MOSFETs. The former can be achieved in a variety of fashions. For instance the back gates of the transistors in the input block can be biased using either the single or the differential fashion as found in the precious circuits. Or the center latch circuit can be back-biased. The outcomes of these two approaches is presented in (Chunyan et al., 2003). Although the accessible frequency range in the VCO mode is dwarfed in contrast to massive ICO response given in logarithmic scale, the VCO performance can be improved by increasing V_{dd} above 0.5 V or by employing more number of inverter stages for the latch. Thus the same circuit can be used as a universal ICO/VCO circuit capable of operation with pW level of signals. More importantly, based on the above example, it should be possible to convert *any* ICO circuit to a VCO using the back gates in IDDG-MOSFET equivalents. This opens up exciting possibilities for ICO/VCO design and analog signal processing.
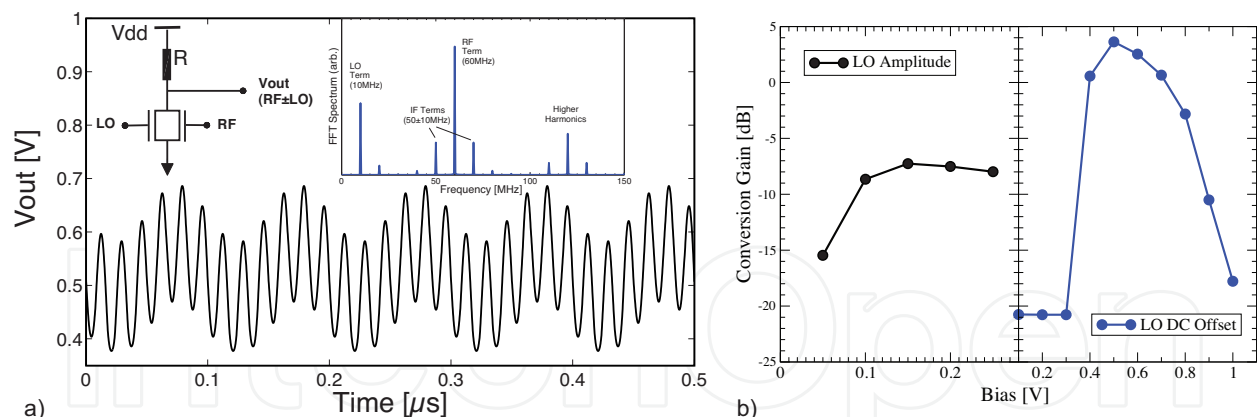
Fig. 13. a) A one transistor simple DG mixer circuit and its output in time and frequency domain (inset). b) The dependence of the mixer down conversion performance as a function of local oscillator (LO) amplitude and DC offset for an RF signal of 80 mV$_{pp}$

3.7 RF Mixers

RF mixers are commonly used in transceiver and analog signal processing systems for up or down conversion of input signals with respect to a reference signal, the local oscillator (LO). They mix (multiply) the two input signals (RF and LO), to produce an output that contain sum ($w_{RF} + w_{LO}$) and difference ($w_{RF} - w_{LO}$) term in the spectral content also known as Intermediate frequency (IF) terms. These new terms at the output is a direct consequence of the non linear transconductance of the transistors. For a good mixer, higher the IF terms the better with respect to the incoming signal amplitude, whose ratio decided the conversion gain. The smallest bulk CMOS circuit accomplishing this task requires 3 transistors, where as the balanced Gilbert Cell is built with as many as 6 transistors. Therefore, the simplicity and performance of a single transistor mixer realizable with a IDDG MOSFET is a truly efficient and interesting one, which we investigate below.

The DG MOSFETs possess natural features suitable for signal cross modulation in efficient and compact RF mixers. The availability of closely coupled and well matched pair of of gates along with fully depleted body in a DG-MOSFET allows us to build a mixer circuit using only one DG MOSFET as shown in Fig.13a (inset). The resistor is intended for setting a reasonable DC bias as well as serving as an AC load for the mixer. Both the TCAD and UFDG simulations have been found to produce almost equivalent temporal oscillations (main panel) and the FFT spectra given in Fig.13a (also inset). Using an RF (50MHz) and LO signals (10MHz) with equal and small amplitudes (100mV), we can clearly observe the IF terms in the FFT spectrum. In order to avoid the bias-point related considerations DC level of both the RF and LO signals are set at 0.5V. Since the DG-MOSFET used in this case has a threshold around 0.25V a depletion mode device may be more suitable in physical implementation when DC level is zero. The appearance of higher harmonics ($w_{RF} - 2w_{LO}$=40MHz and $w_{RF} + 2w_{LO}$=80MHz) in the spectrum is indicative of the higher order non-linear terms in DG-MOSFET transconductance as well as the non-balanced architecture of this single transistor mixer. This can be easily remedied with the inclusion of well known balanced mixer topologies canceling odd terms by current addition. The optimum operating conditions and peak performance of this simple mixer architecture can be explored with the aid of Fig.13b. The left panel shows that conversion efficiency already saturates when the RF amplitude reaches 100mV, while the right panel indicates that a gate overdrive ($V_{GS}-V_T$ of around)
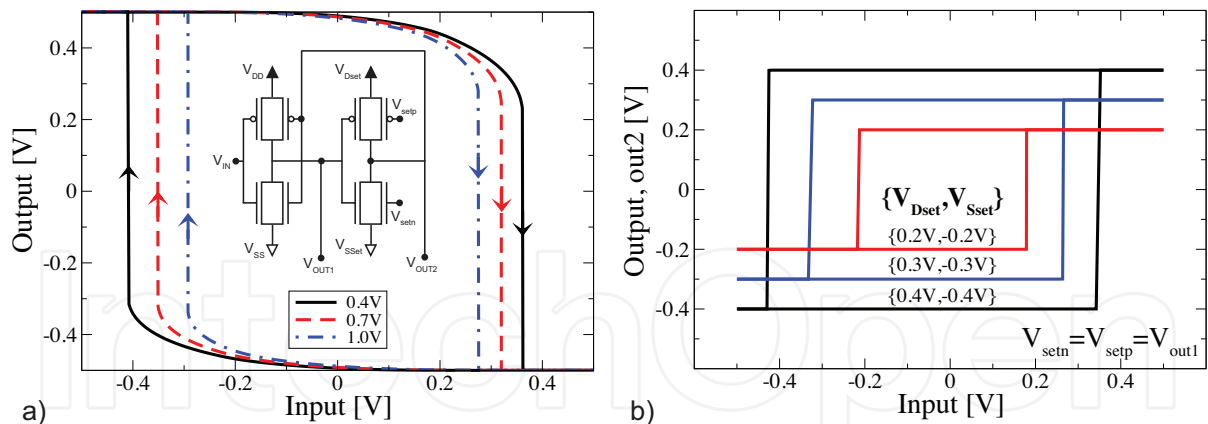
Fig. 14. a) Simulated DC response of the tunable inverting Schmitt Trigger with a large hystereses obtained with relatively small control voltages ($V_{set}^p = -V_{set}^n$), thanks to large gain of CMOS pair used in the second stage for feedback and the inversion is obtained at the output node out1 b) An alternative design for a tunable non-inverting Schmitt Trigger, where tunable rail voltages (V_{Sset} and V_{Dset}) and a higher gain second stage with symmetric gates ($V_{set}^n=V_{set}^p=V_{out1}$) are used. In this case the output is at node out2 , thus non-inverting, and the hysteresis can be scaled both vertically and horizontally using only 4 DG-MOSFETs

250mV is sufficient as the sweet spot in device operation where the non-linear terms are maximized.

It is possible to build other interesting but more complex mixer architectures with DG-CMOS devices, at the expense of circuit area. However, the simple mixer above may find a special welcome for area-tight wireless communication circuits where space and price is a premium. Moreover, the performance of the simple DG-mixer can be further enhanced by material and electrostatic optimization of contacts, channel strain and even doping, known to play a big role in linear device design.

4. Mixed-Signal & Digital Circuit Blocks

Designed as solutions to extend Si CMOS scaling, the DG MOSFETs are known to offer a better switching performance in logic circuits, especially in SDDG configuration. However, this is not the objective of this section and would not be suitable for the general theme of this book. Yet, the inclosure of a section on logic blocks have relevance in two aspects: they are important just as much in mixed-signal circuitry and they can be beneficial pedagogically in exploring more creative designs in building adaptive systems. In some cases, notably in non-linear analog circuits such as the Schmitt trigger circuits or Threshold Logic circuits to be presented next, the boundary between the analog and digital world is even more blurred and parts of the circuit effectively works as an analog computing element.

4.1 Schmitt Triggers

The ability to laterally shift the CMOS amplifiers transfer response paves the way for the construction of a simple Schmitt Trigger circuit, a non linear analog circuit block very useful in reducing noise in analog wave shaping and control circuits as well as in digital systems. In our design, we use only four DG-MOSFETs as opposed to six MOSFETs needed in bulk CMOS design (Cakici et al., 2003). Previous attempts with DG-MOSFETs were either not tunable or needed six transistors for tunability (Kumar et al., 2004). To built a circuit that
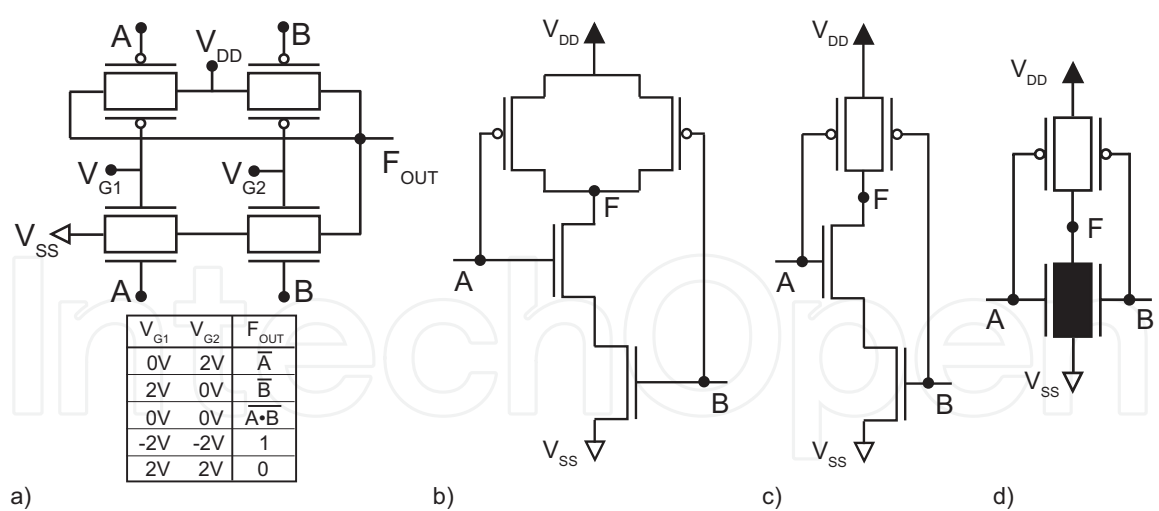
Fig. 15. a) a fine-grain reconfigurable static CMOS digital logic gate realizing five different functions via back gate control by (Beckett, 2008) b) Bulk CMOS NAND implementation, c) hybrid NAND circuit with p-type DG-MOSFET and d) ultra-compact NAND gate realized using a high-V_T n-type DG-MOSFET (filled black) (Chiang et al., 2005)

overcomes these inadequacies, we consider in Fig.14a (inset) a two-stage CMOS circuit where the conjugate programming of the second stage (V_{set}^{p}=$-V_{set}^{n}$) shifts the first stage's response to two extremes. The simulated output of the Schmitt Trigger circuit is shown in Fig.14a for three different bias settings. The conjugate bias required to set the two extremes, *i.e.* the width of the hysteresis, can be decided from Fig.2b. The relatively large gain of the second stage is a key here in producing a very large hysteresis width. To design a small hysteresis, application of a relatively large conjugate bias may be needed, limiting the output swing of the second stage or the amount of shift for the first stage. An upper limit for the resulting power savings in this Schmitt Trigger circuit with four transistors is expected to be around 11% to 14% as shown by earlier works (Cakici et al., 2003).

It is also possible to scale the whole hysteresis by adopting a different topology in the second stage. In this case the rail voltages are the programmable nodes (V_{Dset} and V_{Sset}), and the back gates are tied to front gates (V_{set}^{p}=V_{set}^{n}=V_{out1}), i.e, the SDDG inverter configuration. The simulated characteristics of such a circuit are given in Fig.14b for three rail voltage combinations. The hysteresis is scaled both vertically and horizontally as the feedback voltage from the output of the second stage changes. Also, the gain of the second stage is higher, resulting in a noninverting Schmitt trigger with almost ideal shapes and more spacing between them.

Yet another way of optimizing the Schmitt Trigger circuits would be to reduce bottom-gate coupling by a thicker gate oxide, which would result in smaller shifts in Figure 9a between bias settings. This requires process changes and may be a less desirable path than voltage tuning, which can be realized in a number of alternative fashions besides the above approaches. In any case, tuning via rail voltages may have its own limitations if the tuning circuitry cannot tolerate low-impedance nodes in the circuits above.

4.2 Reconfigurable Static DG CMOS Logic

The DG-CMOS inverter, previously utilized as a high gain amplifier, is the first and foremost reconfigurable logic block to consider in exploring the boundaries of reconfigurable logic

circuits designed with the DG-CMOS technology. It is a simple yet very important circuit. Also known as the logic NOT gate in digital logic circuits, it has a very wide range of usage in all digital systems at all levels of complexity, and determines power×delay product. The switching threshold is usually a trade-off for power and speed and is likely to remain fixed once the device is fabricated. The fabrication tolerances can result in unwanted switching thresholds that are difficult to compensate, which can lead to logic errors or poor performance. The DG-CMOS inverter, on the other hand, can modify the DC transfer curves in order to compensate for the process, voltage, and temperature variations. Such a flexibility will only be becoming more important as the device dimensions go below 20nm, beyond which parameter fluctuations are much larger and more varied (Hwang et al., 2009) At the same time, even a single IDDG-MOSFET can offer a lot as a programmable elements used for turning off power to a complete logic block in an effort to cut down leakage in power-off modes (Tawfik & Kursun, 2004). Therefore, the variable threshold in IDDG devices has many more avenues to impact mixed-signal design than discussed in the following sections.

An interesting and powerful example for reconfigurable static CMOS logic may be found in Fig.15a that uses the back-gate mediated extreme threshold swings to alter the output functionality obtained from only 4 transistors. Obviously, what is interesting is not the actual functions implemented, which are trivial, but the concept which can be extended to include a more complex array of functions using only a fraction of transistors that would be needed in conventional designs.

Another impressive approach to building compact reconfigurable circuits were proposed by IBM group, who indicated that IDDG n-MOSFETs threshold can be selected high enough so that it would only conduct when both inputs are high. This is of course the logic AND functionality from a single transistor, which can be employed in CMOS NAND gates as shown in Fig.15b. It provides impressive gains in Si area usage (∼50% reduction), switching speed (11% improvement for a four-input NAND) and power dissipation (10% reduction), which are experimentally confirmed (Chiang et al., 2006). While these result are impressive in themselves, the elegancy of the concept and flexibility it can provide in reconfigurable and programmable circuits are probably so far under-appreciated.

4.3 Compact Dynamic Digital Circuits

A dynamic CMOS digital circuit performs its functions in successive pre-charge $\Phi = 0$ and evaluation pulses ($\Phi = 1$) of a periodic clock signal. Dynamic digital circuits feature a high-speed operation because the parasitic capacitance is minimized by abandoning the pull-up network in favor of clocking a single p-channel MOSFET that always charges the output node to logic '1' state before the output evaluation phase. Transistor sizing is a key aspect for performance, as optimum transistor size in the pull-down network would lead to a a faster discharging rate. In contrast to a static digital circuit, which would always have twice the capacitive loading (pull-up and pull-down networks), this results in faster operation and lower power dissipation. Two dynamic logic circuits (NAND and NOR) built using IDDG-MOSFETs are studied in this section to illustrate the capabilities of DG-MOSFETs for reconfigurable logic systems. The circuits Fig.16a&b also employ the high-V_T transistors at the logic kernel (see previous section), which leads to halving of the number of input transistors as compared to the conventional CMOS design. It also shortens the long chains of n-channel MOSFET in the path of discharge current by 50%, which is important for its speed performance. Also, the clock inputs are designed using SDDG transistors in an effort to boost
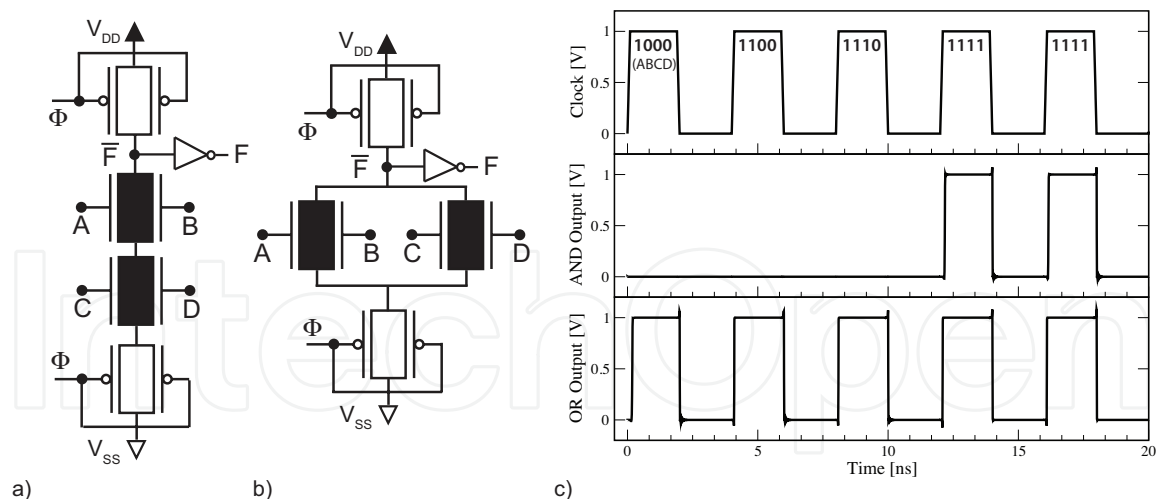
Fig. 16. High-V_T threshold DG-MOSFETs (filled symbols) is used in the logic kernels of the ultra-compact a) 4-input domino F=AND logic gate and b) 4-input domino F=OR logic gate. c) The corresponding timing diagrams obtained from SPICE simulations verifying correct operation as recorded at the non-inverting output (F).

pre-charge and evaluation performance. Note that each pair of inputs driving the independent gates of a single nMOSFET actually carries out an AND functionality as implied by the high-V_t (Chiang et al., 2006). It is therefore important to choose and control DG-MOSFET threshold accurately for this scheme to work.

The simulated timing diagrams obtained from transient SPICE simulations of these two circuits are jointly plotted in Fig.16c, which verifies the correct operation for each input vector indicated in the clock-panel. It is helpful to remember that the output evaluation is done at the rising-edge of a clock signal. Although these circuit examples are simple, the implications for an array of logic systems including memories have been well documented (Datta et al., 2009). For instance, it has been reported that IDDG dynamic logic circuits with improve the read stability of SRAMs by 62%, while reducing its idle mode leakage power, the write power, and the cell area by up to 62%, 16.5%, and 25.53%, respectively (Tawfik & Kursun, 2004)

4.4 Power Efficient DG-XOR Circuit

A practical example of how the DG-CMOS devices can improve the static CMOS circuit performance may be found in Fig.17a, which shows a compact XOR ($\oplus$) circuit block based on high-V_T IDDG transistors. XOR circuits are crucially important for implementing a number of common logic blocks such the parity coders or adders. Thus improvements in this circuit has large implications for a given technology. The number of transistors required to implement this four-input circuit in conventional CMOS technology is eight. However, we only use four transistors and shorter pull-up network thanks to AND functionality hidden with the high V_T IDDG transistors. An evaluation of the SPICE transient output given in Fig.17b confirms that the circuit works accurately. The power dissipated in this DG-XOR implementation V_{DD}=1V is found to be 54% less than that of the conventional circuits with eight single gate transistors. This is accompanied by a 20% speed improvement as well, which resulted from the reduced parasitics.
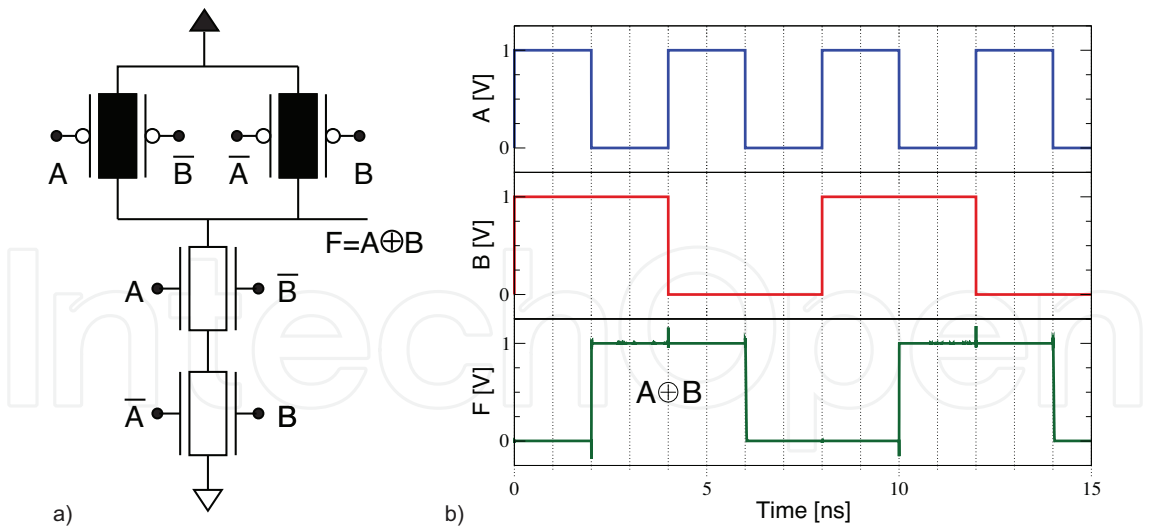
Fig. 17. a) DG XOR circuit with 4 IDDG-MOSFETs, two of which are high V_T (filled black) and b) the simulated output of this circuit

4.5 DG Threshold Logic Gates

In order to build reconfigurable logic systems, one can also use a threshold logic gates (TLG), which is not as widely known as, but can be more powerful than the elementary Boolean gates studied so far (Kaya et. al, 2007). TLGs are composed of two blocks: an input circuit calculating weighted sums of the logic inputs ($\Sigma \omega_i x_i$) and an output block comparing this weighted sum against a pre-set gate Threshold (**T**). If $\Sigma \omega_i x_i \geq$ **T** then the function output F=1, otherwise F=0. Using a multiple input circuits with tunable **T**, it is possible to produce many different logic functions with a single TLG.

To fully exploit the nature of reconfiguration in IDDG MOSFETs, an ultra-compact threshold logic gate is presented in Fig.18 This circuit is designed with IDDG transistors in the input block, resulting in fewer transistors, as compared to the original bulk CMOS circuit. The back-gate of the front half-sized transistors are tied to power rails, ensuring that transistors are constantly turned on to contribute the half weights as indicated in Fig.18. The half-sized transistors serve to prevent undefined states when all input transistors are turned off or to avoid a V_{sum} =0.5 condition. Both channels of double-gate transistors are used for input signals in this design, so the number of input transistors is halved. The input signals applied to p-channel and n-channel double-gate transistors contribute positive or negative magnitude weights, respectively.

The correct operation of AND, MAJ and OR logic functions are verified using SPICE simulations as shown in Fig.19. Although this 8-input circuit functions correctly, there is a concern with the odd-number of inputs being active. When the number of active transistors is not equal between the n- and p-input blocks, it has been found that noise margins may deteriorate. This is because the IDDG transistors current increases typically $\times 2.5$ as opposed to simple doubling when both gates are turned on as in the SDDG case. This additional current can upset circuit operation. However, it is possible to remedy the noise margin problem problem using the tunable IDDG threshold at the inverter. Lowering the **T** slightly to $\sim$0.45V (V_{DD}=1V) provides compensation for the asymmetry in the noise margin, such that correct switching is restored. This demonstrates that **T** adjustment via back-gate biasing may be used for erroneous output transitions or badly designed TLG circuits. Since the weight
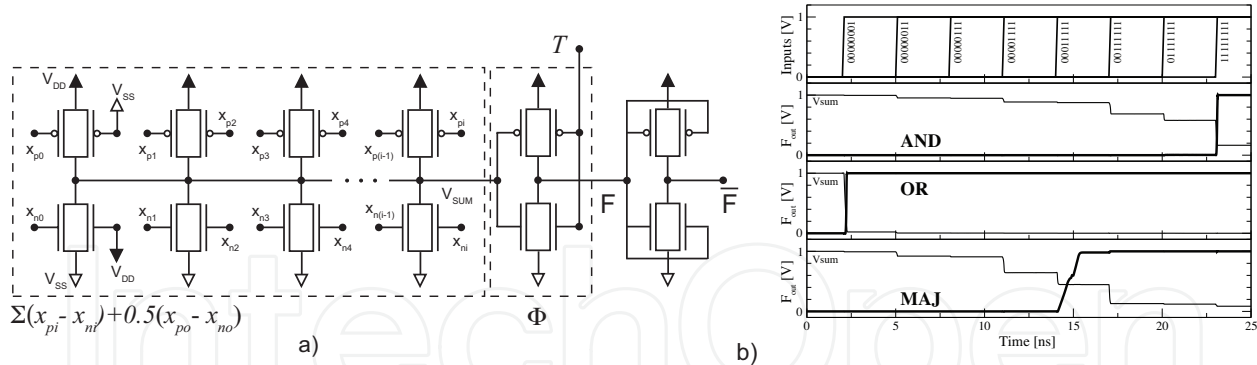
Fig. 18. a) A static-weight threshold logic gate designed using DG-CMOS devices with a minimalist input block and a tunable gate threshold, and b) its simulated logic functionality

transistors can be eliminated and back-gates used as additional inputs, this implementation offers remarkable gains in silicon area while also capable able to correct any design errors.

4.6 DG-TLG with Dynamic Weights

Expanding on the static weight DG-TLG design introduced above, an innovative circuit with dynamic weight programming capability is possible when the back gates are used weight programming nodes, as shown in Fig.19a. Although it has the more number of input transistors as compared to the previous circuit, it takes advantage of the back-gates to dynamically program the weights for all inputs. The back-gate biasing changes weights of each transistor associated with the input at the front gate. The typical range of the back-biasing voltages are needed for practical weights and can be found from the plot in Fig.19b. These weights have been calculated by normalizing simulated currents with the IDDG-MOSFET current as both gates held at 1.0V. The calculated weights have limited V_{ds} biasing dependency for weights less than 4. It must be noted that to have zero current at $w_i=0$ or $x_i=0$ case, the input transistors must have high-V_T (>1.0V) in Fig.19a. Therefore, only when both inputs are high simultaneously ($w_i=x_i=1$) will the IDDG transistor be able to conduct current. The identical half-sized double-gate transistors located in the front of the circuit are biased for contributing half weights in the analog computation block so race conditions are less likely.

To verify the circuit performance and functionality, a SPICE simulation is conducted in Fig.20a, which illustrates examples of weight programming for this highly adaptive digital system. Using the same block with different weights and gate threshold, one can realize different logic functions easily. Especially for large weights, however, a dedicated D/A converter may be needed, which is the main drawback of this implementation. The TLG functions work correctly in all cases, and designed to produce identical outputs, as would be expected from the choice of weights and the gate threshold (**T**). Clearly, this circuit has an expandable functionality, which is useful for fine-grain reconfigurability.

There is one complication in Fig.20a, however, which is associated with the slow speed of the second function $F_2=2x_1+2x_3+2x_5+2x_7$. The speed of this circuit is slow mainly because the headroom of the noise margin is inferior, as can be seen from the internal node voltage, $V_{sum} \approx T = 0.5V$ at the time of transition. This implies that the transistor sizes chosen in the design are not optimum in this particular implementation. The delay in output transition is significantly influenced by the noise margin as much as the size of input transistors and implemented functions. Unlike the static-weight circuit, this variable-weight circuit has smooth transitions
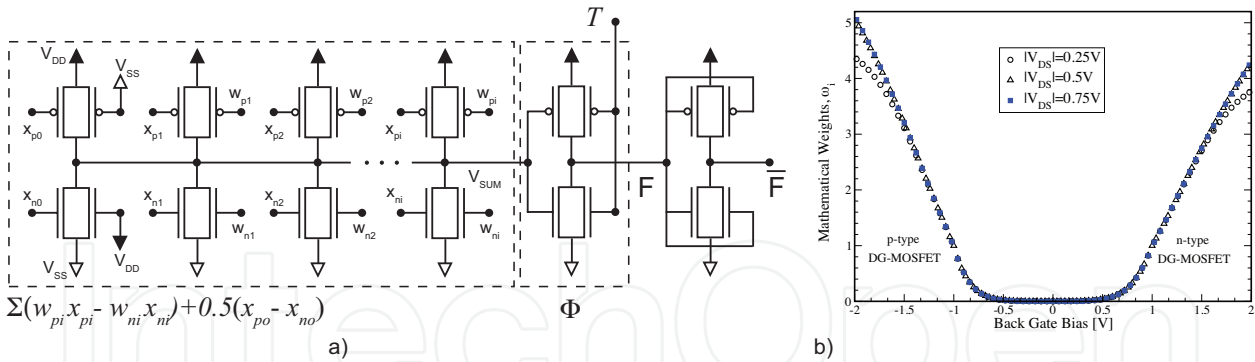
Fig. 19. a) DG-TLG circuit re-designed for dynamic weights and b) typical values of mathematical weights accessible via back-gate biasing

and outstanding noise margins in terms of "stair-case" response shown in Fig.20b. As input transistors are activated one at a time, no errors appear up to eight active inputs. Therefore, no complications are expected in weight programming, except providing additional circuitry to set appropriate back-bias voltages and routing such signals on the chip layout.

5. Future Directions & Summary

With the imminent arrival of public-domain surface-potential based SPICE models for multiple gate SOI MOSFETs in general and DG-MOSFETs in particular, circuit engineering is well poised to take advantage of the remarkable design latitude and functional flexibility these transistors have in store for extending Si roadmap to the next decade. With these new simulation engines and rapidly expanding system-level efforts led by several national and international programs in Japan and Europe, along with the several companies and academic centers now providing practical means to prototype DG circuits, we should expect a wide range of tunable analog RF circuits, reconfigurable logic blocks, on-chip power management blocks and mixed-signal system-on-chip applications to come into existence in the next few years. It would not be surprising therefore to find in five years actual products containing SDDG and IDDG MOSFETs in 'hybrid' implementations, whereby a limited number of such circuits and devices are employed to improve nanocircuits fault tolerance, and adaptability. Although this timeline is probably rather speculative, once the Si scaling reaches sub-20nm, it is conceivable to expect that all 'bets' are open. Then all technologies that can provide maximum amount of performance leverage (technology nodes) with minimum amount of investment and departure from the established fabrication lines are in the race to extend Moore's Law. We believe DG-MOSFETs may offer what is just needed.

This chapter has provided multiple examples for many of the fundamental analog CMOS building blocks (including amplifiers, oscillators, filters, mixers and logic gates) used in today's wireless communication, mobile computing, and signal sensing and mixed-signal processing platforms. These building blocks have tunable performance and offer fine-grain reconfigurable functionalities thanks to the DG-CMOS devices expected to make a big impact in the final stretch of Si scaling. Especially in the independently driven configuration, the DG devices are capable of providing the design latitude and flexibility that will be especially valuable when conventional circuits can not be further pursued due to matching problems, power dissipation or both. However, they will also bring their own challenges in terms of layout, control signal routing and additional steps in fabrication.
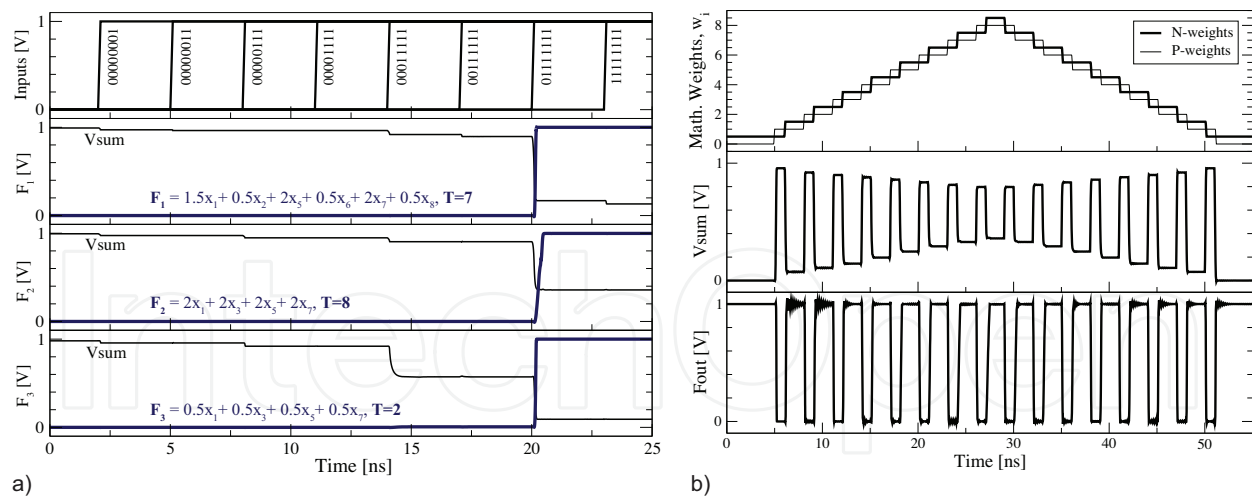
Fig. 20. a) verification of correct operation of the dynamic weight DG-TLG circuit. b) stair case simulation exploring the worst case scenarios for the noise margin in NAND/AND functions of increasing size
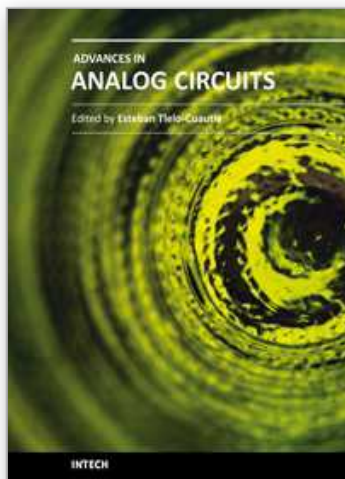
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