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Lifetime Yield Optimization of Analog Circuits Considering Process Variations and Parameter Degradations

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1. Introduction

As semiconductor technology continuously scales, the joint effects of manufacture process variations and operational lifetime parameter degradations have been a major concern for analog circuit designers since they affect the lifetime yield value, i.e., the percentage of the products which can satisfy all of the pre-defined specifications during lifetime operation (Alam, Kang, Paul & Roy, 2007), (Gielen et al., 2008).

The analysis and optimization of analog circuits considering process variations alone have been in research for decades, and certain design centering algorithms and commercial software are available to achieve a design for yield (more specifically, fresh yield) (Nassif, 2008), (Antreich et al., 1994). On the other hand, the modeling of device parameter degradations such as Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI) has been so far focusing mainly on the nominal values without considering the underlying variations during manufacture process (Jha et al., 2005), (Liu et al., 2006) and (Martin-Martinez et al., 2009). A robust analog circuit design is thus needed tolerant of both process variations and lifetime parameter degradations, maximizing the lifetime yield value. Most of the past works quantify the influences of process variations and lifetime degradations separately. However, since lifetime degradations will drift certain device parameters, e.g., V_{th} , from their fresh values during circuit lifetime operation, the distribution of the circuit-level performance will also shift its position during lifetime, as can be seen in Figure 1, where 1000 Monte-Carlo simulations are run on a fresh and 5-year-old Miller OpAmp. Values of Gain-Bandwidth Product (GBW) and Rising Slew Rate (SR) are shown, both moving towards negative direction. In order to ensure a robust design, it is thus necessary to consider the joint effects of process variations and lifetime parameter degradations during design phase, such that certain weak points can be detected early, and additional safe margins can be assigned properly.

In this chapter, a novel design methodology to analyze and optimize the lifetime yield value of analog circuits based on the idea of lifetime worst-case distance is presented. It does not involve Monte-Carlo simulations, and considers process variations and major parameter degradation mechanisms such as NBTI and HCI.

The proposed work is based on the preliminary methods presented in (Pan & Graeb, 2009) and (Pan & Graeb, 2010). The content is augmented such that the sizing constraints for both

fresh and aged circuits are considered, as well as the required additional area penalty for the reliability optimized design is analyzed.

The rest of the chapter is organized as follows. Section 2 introduces the physical behavior of two main degradation effects, namely, NBTI and HCI. Section 3 briefly reviews the current methods in literature which study the joint effect of process variations and parameter lifetime degradation. Section 4 gives basic definitions needed throughout the chapter. The definitions of lifetime yield and lifetime worst-case distance are proposed in Section 5, which are the key concepts of the chapter. Section 6 introduces the sizing constraints which must be considered in the proposed method. The new reliability-aware design flow is proposed in Section 7. Section 8 introduces a linear prediction model in time domain which is used to speed up the analysis of lifetime worst-case distance values. Then experimental results are given in Section 9. Finally Section 10 concludes the chapter.

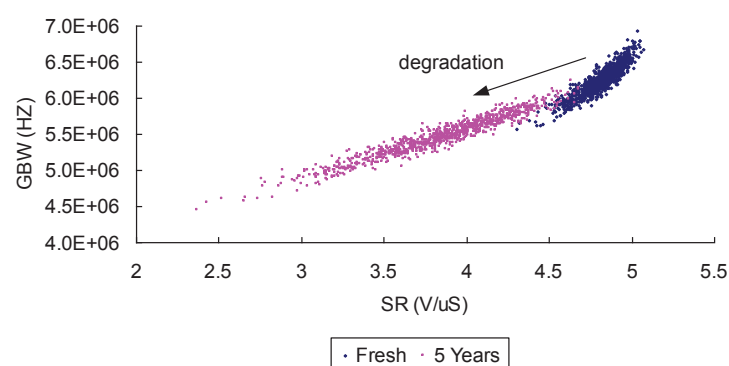


Fig. 1. Degradation of performance distributions from fresh circuit to 5 years of a Miller OpAmp by 1000 Monte-Carlo simulations.

2. Degradation physics

In this section, the physical characters of HCI and NBTI will be briefly introduced. For a more complete discussion, please refer to (Hu et al., 1985), (Schroder & Babcock, 2003), (Alam, Kufluoglu, Varghese & Mahapatra, 2007) and (Wang et al., 2007).

2.1 HCI

Figure 2(a) shows the simplified physical behavior of HCI effect on an NMOS transistor. HCI effect is the result of injection of channel carriers from the conducting channel under the gate into the gate dielectric. It happens near the drain area where the lateral electric field is high and the channel carriers gain enough kinetic energy during the acceleration along the channel. The hot channel carriers may hit an atom in the substrate, breaking a electron-hole pair or a Si-H bond, and introducing interface traps and a substrate current.

Traditional modeling method of HCI is by analyzing the substrate current I_{sub} (Hu et al., 1985). The correlation is due to the fact that both hot-carriers and substrate current are driven by a common factor-the maximum channel electric field E_m at the drain end. Some recent research (Wang et al., 2007) point out that, as technology scales, I_{sub} will be dominated by various leakage components such as gate leakage, junction current, etc. Authors in (Wang et al., 2007) proposed the following reaction-diffusion based model for the degraded parameter ΔV_{th} due

to HCI as:

$$\Delta V_{th} = \frac{q}{C_{ox}} K_2 \sqrt{Q_i} \exp\left(\frac{E_{ox}}{E_{o2}}\right) \exp\left(-\frac{\psi_{it}}{q\lambda E_m}\right) t^{n'} \quad (1)$$

where Q_i is the inversion charge, ψ_{it} is the trap generation energy and the time exponential constant n' is 0.45.

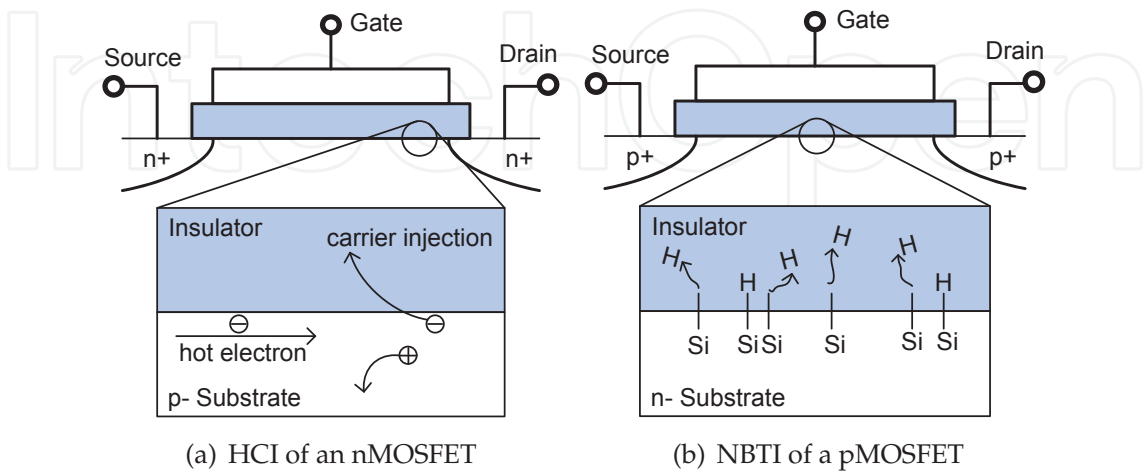


Fig. 2. Physics of HCI and NBTI

2.2 NBTI

The physical behavior of NBTI on a PMOS transistor is shown in Figure 2(b). It is commonly accepted that NBTI is the result of hole-assisted breaking of Si-H bonds at Si/SiO₂ interface (Alam, Kufluoglu, Varghese & Mahapatra, 2007) when a PMOS is biased in inversion using the Reaction-Diffusion (R-D) model:

$$\frac{dN_{IT}}{dt} = k_F(N_0 - N_{IT}) - k_R N_H(0) N_{IT} \quad (2)$$

where N_{IT} is the fraction of Si-H bonds at the Si/SiO₂ interface which breaks at time t , N_0 is the initial number of all Si-H bonds, and k_F is the dissociation rate constant. The second term in (2) describes the annealing process of the released H atoms. $N_H(0)$ is the H concentration at the interface.

NBTI is getting more serious as technology scales, since the vertical oxide field is continuously increasing to enhance transistor performance. Thus a hole in the channel can be easily captured and a two-electron Si-H covalent bond at the Si/SiO₂ interface can be weakened by it. The weakened Si-H bonds break easily at certain high temperature. Atomic H's are released in short time, then they convert to and diffuse as molecular H₂ in long time (>100 s) (Alam, Kufluoglu, Varghese & Mahapatra, 2007).

NBTI effect will degrade certain transistor parameters, such as threshold voltage, drain current, transconductance, etc. Threshold voltage degradation due to NBTI is given by (Yan et al., 2009)

$$\Delta V_{th} = A \left(\frac{V_{gs}}{t_{ox}}\right)^\alpha \exp\left(-\frac{E_a}{kT}\right) t^n \quad (3)$$

where K is Boltzmann's constant, E_a is the activation energy, $n = 0.25$ for atomic H in short time, and $n = 0.16$ for molecular H₂ in long time as discussed above.

The intrinsic variations of NBTI are studied in (Rauch, 2002). The expression of variation in ΔV_{th} shift is

$$\sigma(\Delta V_{th}) = \sqrt{\frac{K t_{ox} \mu (\Delta V_{th})}{A_G}} \quad (4)$$

where T_{ox} is effective gate oxide thickness, A_G is its area and K is an empirical constant.

It is pointed out in (Schroder & Babcock, 2003) that, NBTI should not exhibit any gate length dependence, since it does not depend on lateral electric fields. But NBTI is sometimes enhanced with reduced gate length, which is not well understood yet. The closeness of the source and drain maybe one of the reasons for that.

3. State of the art

It is only since very recent years that the joint effects of process variations and lifetime parameter degradations are proposed in literature. They differ in the type of reliability effects considered and the type of circuits studied.

For digital circuits, NBTI-aware statistical timing analysis considering process variations are proposed in (Vaidyanathan, Oates, Xie & Wang, 2009), (Vaidyanathan, Oates & Xie, 2009), (Wang et al., 2008) and (Lu et al., 2009). Authors in (Vaidyanathan, Oates, Xie & Wang, 2009) build up gate-level delay fall-out model by propagating the device parameter fall-out model due to NBTI and process variations into the gate delay model. They consider in addition the intrinsic variations of NBTI process in (Vaidyanathan, Oates & Xie, 2009). Using variation-aware gate delay model, the timing behavior of a path is modeled in (Wang et al., 2008). Authors in (Lu et al., 2009) apply the NBTI aging-aware statistical timing analysis into circuit level. All of those methods rely on the analytical expression of performance features, which is suitable for digital circuits but difficult in analog domain.

For analog circuits, authors in (Maricau & Gielen, 2009) use Monte-Carlo simulation loop to obtain the degraded performance values for each fresh random sample at every lifetime point. Then the most appropriate distribution function at each time is fitted, thus a failure distribution throughout the lifetime can be found. It results in a high simulation effort and difficulty for further optimization. They improve their method in (Maricau & Gielen, 2010) using response surface model to speed up the simulations, where certain numbers of random samples are still required to obtain the degraded distribution information.

None of the above mentioned methods proposes an analog circuit design flow considering the joint effects of process variations and lifetime parameter degradations. A new methodology concerning such joint effects is thus required to help designer during the design phase.

4. Definitions

We first consider the fresh circuit here, i.e., no degradation is occurred. We distinguish three types of parameter vectors,

- design parameters \mathbf{d} , for example transistor widths and lengths, which are optimization parameters of the analog sizing process.
- statistical parameters \mathbf{s} , for example, V_{th} , t_{ox} , L_{eff} , etc, that have variations during manufacturing process. They are usually modeled by Gaussian, log-normal or uniform distributions. Without loss of generality, those distributions can be transformed into a Gaussian distribution (Eshbaugh, 1992) with mean vector \mathbf{s}_0 and covariance matrix \mathbf{C} in

the following form: $\mathbf{s} \sim \mathcal{N}(\mathbf{s}_0, \mathbf{C})$, with

$$\text{pdf}_N(\mathbf{s}) = \frac{1}{\sqrt{2\pi}^{n_s} \cdot \sqrt{\det \mathbf{C}}} \cdot \exp\left(-\frac{\beta^2(\mathbf{s})}{2}\right) \quad (5)$$

whose level contours are ellipsoids

$$\beta^2(\mathbf{s}) = (\mathbf{s} - \mathbf{s}_0)^T \cdot \mathbf{C}^{-1} \cdot (\mathbf{s} - \mathbf{s}_0) \quad (6)$$

- range parameters \mathbf{r} , for example supply voltage and temperature.

It is obvious that the integration of (5), the multi-dimensional probability density function (pdf) of a Gaussian distribution, over the entire statistical parameter space is 1. However, we have to consider the specified performance features also.

The performance vector \mathbf{f} results from the output of a numerical circuit simulation, for example gain, bandwidth, slew rate:

$$\mathbf{d}, \mathbf{s}, \mathbf{r} \mapsto \mathbf{f}(\mathbf{d}, \mathbf{s}, \mathbf{r}) \quad (7)$$

Each element of \mathbf{f} has a certain lower bound and/or upper bound. As a result, in the statistical parameter space, certain part of the Gaussian pdf will be cut off, since a part of parameter variations falls out of the acceptance region bordered by the performance specifications. In other words, from (7) a corresponding set of statistical parameters can be found to make performances fulfill their specifications for all range parameter vectors within their acceptance region T_r . Thus a statistical parameter acceptance region $A_s(\mathbf{d})$, the shape of which depends on \mathbf{d} , can be defined as

$$A_s(\mathbf{d}) = \left\{ \mathbf{s} \mid \forall_{\mathbf{r} \in T_r} \mathbf{f}_l \leq \mathbf{f}(\mathbf{d}, \mathbf{s}, \mathbf{r}) \leq \mathbf{f}_u \right\} \quad (8)$$

Fresh yield Y is the percentage of manufactured circuits that satisfy the performance specification considering statistical parameter variations.

$$\begin{aligned} Y &= \text{prob}\left\{ \forall_{\mathbf{r} \in T_r} \mathbf{f}_l \leq \mathbf{f}(\mathbf{d}, \mathbf{s}, \mathbf{r}) \leq \mathbf{f}_u \right\} \\ &= \text{prob}\{\mathbf{s} \in A_s(\mathbf{d})\} \end{aligned} \quad (9)$$

As pointed out in (Graeb, 2007) and (Antreich et al., 1994), the worst-case distance, β_w , can be used as an indicator of circuit robustness. It corresponds to the ellipsoid among the level contours of Gaussian pdf that just touches the performance boundary at worst-case point \mathbf{s}_w :

$$\beta_w^2 = (\mathbf{s}_w - \mathbf{s}_0)^T \cdot \mathbf{C}^{-1} \cdot (\mathbf{s}_w - \mathbf{s}_0) \quad (10)$$

\mathbf{s}_w has the highest probability density among all boundary parameters. In a practical analog circuit yield analysis and design centering flow, it is found numerically by solving

$$\mathbf{s}_w = \arg \min_{\mathbf{s}} \{\beta^2(\mathbf{s}) \mid f(\mathbf{s}) = f_{l,u}\} \quad (11)$$

β_w can be interpreted as β_w -sigma circuit robustness. The resulting fresh yield with respect to one performance specification f_i can be approximated by

$$Y_i = \int_{-\infty}^{\beta_{w,i}} \frac{1}{\sqrt{2\pi}} e^{-\frac{1}{2}\xi^2} \cdot d\xi \quad (12)$$

for a transformed standard Gaussian distribution.

5. Lifetime yield and lifetime worst-case distance

Extending to the definition of lifetime yield, we take the circuit operating time t into consideration. For the three types of parameters defined previously, statistical parameters will degrade from its fresh value during lifetime. Consequentially the performance value will also drift. Thus both of them are functions of operating time.

At time t , we have $\mathbf{s}(t) \sim \mathcal{N}(\mathbf{s}_0(t), \mathbf{C}(t))$, and

$$\mathbf{d}, \mathbf{s}(t), \mathbf{r} \mapsto \mathbf{f}(\mathbf{d}, \mathbf{s}(t), \mathbf{r}) \quad (13)$$

The statistical parameter acceptance region now becomes

$$A_s(\mathbf{d}, t) = \{\mathbf{s}(t) \mid \forall \mathbf{r} \in T_r, \mathbf{f}_l \leq \mathbf{f}(\mathbf{d}, \mathbf{s}(t), \mathbf{r}) \leq \mathbf{f}_u\} \quad (14)$$

The corresponding lifetime yield $Y(t)$ at time t is the percentage of circuits which can still fulfill the performance specifications after parameter degradation. Since the original distribution around \mathbf{s}_0 will shift to a new distribution with new mean vector $\mathbf{s}_0(t)$ and covariance matrix $\mathbf{C}(t)$, a certain percentage of the fresh circuits which satisfied the specification will fall out of the acceptance region after time t (Figure 3).

Lifetime yield at time t can be defined as

$$\begin{aligned} Y(t) &= \text{prob}\{\forall \mathbf{r} \in T_r, \mathbf{f}_l \leq \mathbf{f}(\mathbf{d}, \mathbf{s}(t), \mathbf{r}) \leq \mathbf{f}_u\} \\ &= \text{prob}\{\mathbf{s}(t) \in A_s(\mathbf{d}, t)\} \end{aligned} \quad (15)$$

Comparing with (12), we can see that the fresh yield is just a special case for lifetime yield when t is set to 0 for the fresh circuit without any degradation (denoted as $t = t_0$ from now on). The value of lifetime yield thus can reflect the influence of parameter degradations.

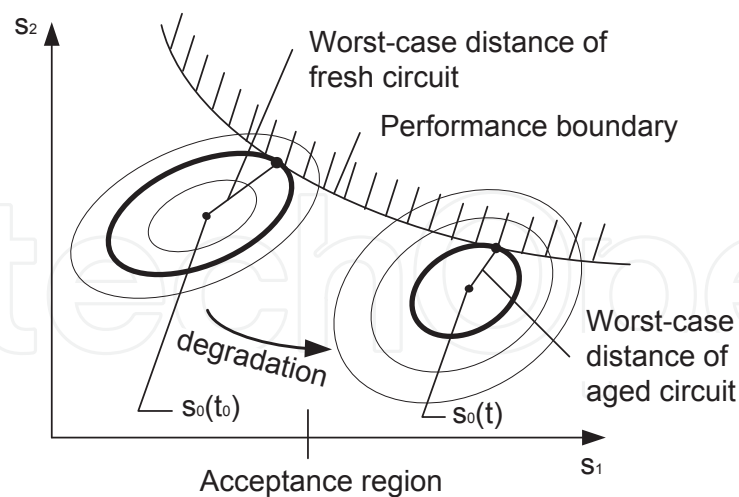


Fig. 3. Lifetime worst-case distances of fresh and aged circuits with corresponding ellipsoids (in thick) during lifetime degradation for one performance specification.

Figure 3 shows lifetime worst-case distance of fresh and aged circuits in statistical parameter space with corresponding ellipsoids (in thick) for one performance specification both at time t_0 and t . It is assumed from now on that worst-case distance degrades monotonically.

As can be seen, during lifetime degradation both $\mathbf{s}_0(t)$ and $\mathbf{C}(t)$ change their values, a part of statistical parameters around worst-case parameter $\mathbf{s}_w(t_0)$ thus fall out of the acceptance region $A_{s,i}(\mathbf{d})$ for the i th performance feature in vector \mathbf{f} . Worst-case distance decreases, leading to a decreasing lifetime yield. Note that the mean vector $\mathbf{s}_0(t)$ still fulfills the specification, but the parameters around $\mathbf{s}_w(t_0)$ are very sensitive to the degradation, since they already locate on the boundary of $A_{s,i}(\mathbf{d})$ before degradation occurs. The value of lifetime yield $Y_i(t)$ with respect to one performance feature f_i can be estimated by:

$$Y_i(t) = \int_{-\infty}^{\beta_{w,i}(t)} \frac{1}{\sqrt{2\pi}} e^{-\frac{1}{2}\xi^2} \cdot d\xi$$

(16)

where $\beta_{w,i}(t)$ is the corresponding lifetime worst-case distance

$$\beta_{w,i}^2(t) = (\mathbf{s}_w(t) - \mathbf{s}_0(t))^T \cdot \mathbf{C}(t)^{-1} \cdot (\mathbf{s}_w(t) - \mathbf{s}_0(t))$$

(17)

Table 1 shows the correspondence between worse-case distance and yield.

β_w	-3	-2	-1	0	1	2	3
Yield	0.1%	2.2%	15.8%	50%	84.1%	97.7%	99.9%

Table 1. Worst-case distances and corresponding yield value at any time t .

For example, $\beta_{w,i}(t_0) = 3$ refers to a 3-sigma design at t_0 of a performance feature f_i . The total lifetime yield $Y(t)$ is bounded by:

$$1 - \sum_i (1 - Y_i(t)) \lesssim Y(t) \lesssim \min_i Y_i(t)$$

(18)

A smaller worst-case distance during lifetime leads to more significant yield loss, thus it is important in our new design flow to analyze and optimize the worst-case distances and the corresponding yield values during lifetime to ensure a robust design.

6. Sizing rules

As shown in (Massier et al., 2008), sizing rules of the analog circuits are the constraints that must be satisfied during circuit sizing. They include, for example, geometry constraints (e.g., transistor width, length, area) and electrical constraints (e.g., transistor gate-source voltage V_{gs} , drain-source voltage V_{ds}). They are used to ensure the proper functionalities of the circuits, for example, preventing the transistors from entering the inappropriate operation regions, or limiting the voltage difference of V_{ds} in a transistor pair to a certain value, etc. It is known that some of the sizing rules for the fresh circuit will not be fulfilled after the step of lifetime yield optimization carried out on the aged circuit (Pan & Graeb, 2009). Which means, even if the fresh yield happened to be high after the step of lifetime yield optimization, the resulting circuit is very sensitive to the process variations at fresh time. Considering such sizing rules for both fresh and aged circuits, we apply the fresh and aged sizing rules checking during the lifetime yield optimization process, which will ensure the functionality and robustness of both fresh and aged circuits.

7. New design flow

The proposed lifetime yield optimization flow uses a tool WiCkeD (Antreich et al., 2000) and aging simulator RelXpert from Cadence with NBTI and HCI degradation engines. The lifetime yield of the analog circuit is optimized by maximizing both the fresh worst-case distance and lifetime worst-case distance values, considering the sizing constraints for both fresh and degraded circuits. The result of the flow ensures a robust analog design tolerant of both process variations and lifetime parameter degradations, at the cost of an additional layout area.

7.1 Software

EDA tools that contain various degradation models are available today. One of the most famous tools is the Berkeley Reliability Tools (BERT) (Tu et al., 1993), which is the origin of the tool RelXpert by Cadence today. Our proposed new design flow does not rely on specific tools or models. Here we take RelXpert as an exemplary degradation tool for demonstration purpose.

A simplified working flow of RelXpert is shown in Figure 4. It can generate degraded BSIM3/4 model cards for each transistor at a specified time t , taking the fresh circuit netlist and Cadence's AgeMOS model as input. The transistor degradation as well as the degraded circuit netlist at time t are produced, ready for SPICE simulation to get a degraded performance.

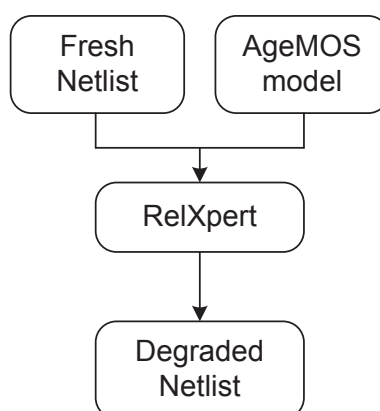


Fig. 4. Simplified work flow of RelXpert from Cadence.

For design centering/yield optimization, we exemplarily use the design optimization software WiCkeD (Antreich et al., 2000). Its yield analysis and optimization algorithms are based on worst-case distances mentioned above. It can always produce an optimized design parameter vector towards a maximized yield considering distributions of statistical parameters.

7.2 New design flow

Considering both process variation and lifetime degradation, our new design flow to analyze and optimize the lifetime yield is shown in Figure 5.

In the new design flow, the fresh circuit with initial design parameters \mathbf{d} is first optimized to obtain a maximum fresh yield, producing \mathbf{d} for optimal yield. It involves internal loops between circuit simulator and WiCkeD. During this step, the fresh sizing rules are checked. Then the circuit lifetime yield optimization for a specified time point t is performed on

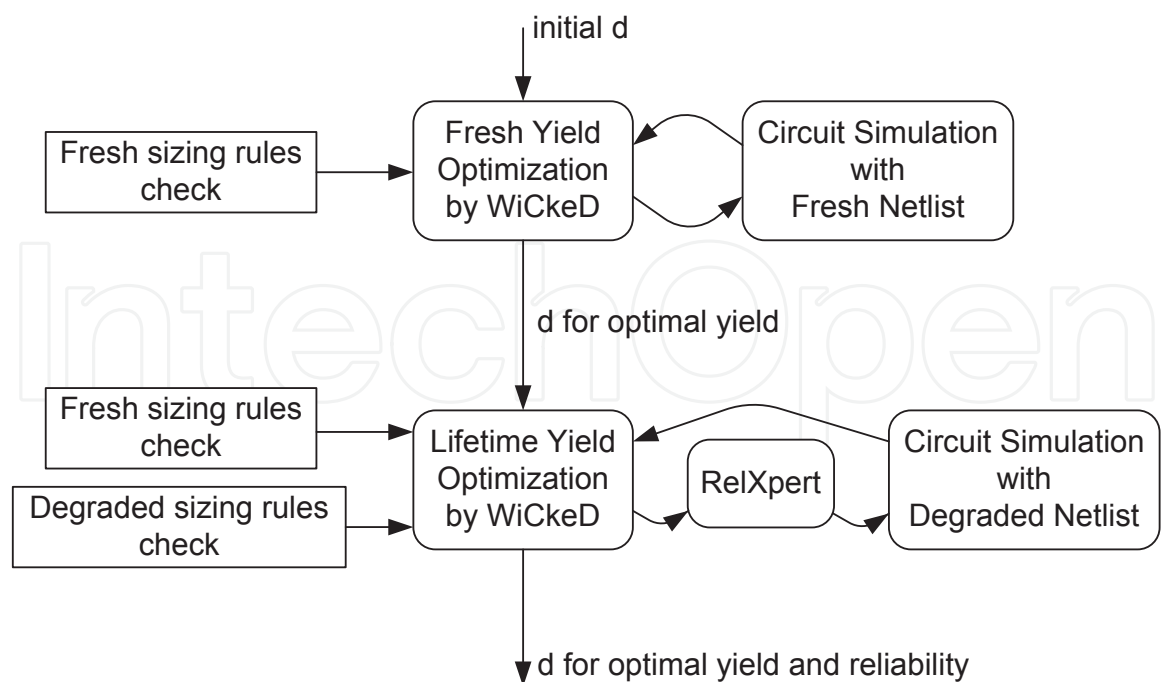


Fig. 5. The new design flow with reliability optimization.

the degraded netlist generated by RelXpert. Note that for each internal optimization loop, an updated netlist from WiCkeD will be given to RelXpert to obtain a renewed version of degraded netlist. During this step, both the fresh and degraded sizing rules are checked to ensure the correct functionality of the circuit both at fresh time and after degradation. The final obtained design parameters \mathbf{d} for optimal yield and reliability are the resulting solution of the design flow.

Fresh yield optimization step ensures that the smaller worst-case distances will be increased, thus the fresh design is centered such that it is already less sensitive to parameter drift. This provides a reasonable starting point for lifetime yield optimization, since the influence of parameter degradation on the performance and yield is kept at minimum level.

After the lifetime yield optimization, optimized design parameters are obtained such that any decreasing worst-case distances during lifetime are increased again as much as possible. The design is centered now such that the most degradation-sensitive worst-case distance will be kept maximum. The resulting design solution is thus optimal considering both process variations and lifetime degradations.

8. Prediction: Speed up the $\beta_w(t)$ evaluation

In this section, a prediction model of lifetime worst-case distance in time domain is presented to speed up the analysis of lifetime yield value. Only performance and statistical parameter sensitivity analysis are needed, in comparison to the Monte-Carlo simulation method and numerical optimization solutions. It is based on the linear performance model as follows. The index i of i th performance in vector \mathbf{f} is left out for simplicity. Without loss of generality, only upper bound f_u is considered hereafter.

8.1 Linear performance model

At any time t during the lifetime, the first-order Taylor expansion of performance $f(t)$ with respect to $\mathbf{s}(t)$ from worst-case point $\mathbf{s}_{w,u}$ in \mathbf{s} space is

$$f(\mathbf{s}(t)) \equiv f(t) \approx f(\mathbf{s}_{w,u}(t)) + \nabla f(\mathbf{s}_{w,u}(t))^T \cdot (\mathbf{s}(t) - \mathbf{s}_{w,u}(t)) \quad (19)$$

By assuming a linear performance model, the sensitivity of performance over statistical parameters keeps constant, i.e.,

$$\nabla f(\mathbf{s}_{w,u}(t)) \equiv \mathbf{g} \quad (20)$$

is constant over the entire \mathbf{s} space at any time. Thus the level contours of f in \mathbf{s} space are equidistant lines as illustrated in dashed lines in Figure 6. $f(\mathbf{s}_{w,u})$ in (19) is the upper bound value f_u . So from (19) the linear performance model at t can be formulated as

$$f(t) \approx f_u + \mathbf{g}^T \cdot (\mathbf{s}(t) - \mathbf{s}_{w,u}(t)) \quad (21)$$

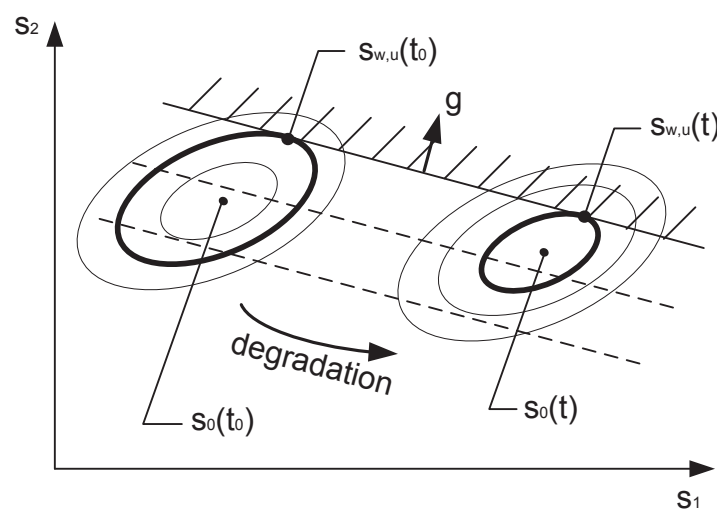


Fig. 6. Linear performance model during lifetime degradation in statistical parameter space (dashed lines are equidistant level contours of f , ellipsoids are level contours of statistical parameters).

$\mathbf{s}_{w,u}(t)$ is called worst-case statistical parameter vector at t . It is the statistical parameter vector where the corresponding performance f reaches its boundary value f_u at t . It corresponds to the position in \mathbf{s} space where the probability of occurrence reaches its maximum in the non-acceptance region (shaded area in Figure 6). A robust design indicates that such a probability of occurrence should be kept minimum, i.e., $\mathbf{s}_{w,u}$ should be positioned furthest away from $\mathbf{s}_0(t)$ so that it is least sensitive to the \mathbf{s} changes which may cause it fall into non-acceptance region.

Since $\mathbf{s}(t) \sim \mathcal{N}(\mathbf{s}_0(t), \mathbf{C}(t))$, the mean and the variance of the linearized performance model can be formulated from (21) as

$$\mu(f(t)) = f_u + \mathbf{g}^T \cdot (\mathbf{s}_0(t) - \mathbf{s}_{w,u}(t)) \quad (22)$$

$$\sigma_{f(t)}^2 = \mathbf{g}^T \cdot \mathbf{C} \cdot \mathbf{g} \equiv \sigma_f^2 \quad (23)$$

where (23) is constant over time. Taking the process variation as second order effects on the sensitivity towards degradation, $\mathbf{C}(t)$ is assumed to be constant, i.e., $\mathbf{C}(t) = \mathbf{C}$ (Sobe et al., 2009).

Considering parameter degradation from t_0 to t , a first-order Taylor approximation of $\mu(f(t))$ with respect to t from t_0 can be expressed as

$$\bar{\mu}(f(t)) = \mu(f(t_0)) + \frac{\partial \mu_f}{\partial t} \Big|_{t_0} \cdot (t - t_0) \quad (24)$$

From (22) we have

$$\mu(f(t_0)) = f_u + \mathbf{g}^T \cdot (\mathbf{s}_0(t_0) - \mathbf{s}_{w,u}(t_0)) \quad (25)$$

and

$$\frac{\partial \mu_f}{\partial t} \Big|_{t_0} = \mathbf{g}^T \cdot \left(\frac{\partial \mathbf{s}_0(t)}{\partial t} \Big|_{t_0} - \frac{\partial \mathbf{s}_{w,u}(t)}{\partial t} \Big|_{t_0} \right) \quad (26)$$

It can be observed from (26) that the product

$$\mathbf{g}^T \cdot \frac{\partial \mathbf{s}_{w,u}(t)}{\partial t} \Big|_{t_0} \quad (27)$$

remains zero, since the two vectors \mathbf{g} and $\frac{\partial \mathbf{s}_{w,u}(t)}{\partial t} \Big|_{t_0}$ are orthogonal to each other. This is easy to understand because during the degradation of \mathbf{s} parameters, the worst-case point $\mathbf{s}_{w,u}$ moves along the performance boundary f_u , as can be observed in Figure 6, while the performance gradient \mathbf{g} always points to the direction that is vertical to that boundary in the performance model.

So (26) becomes

$$\frac{\partial \mu_f}{\partial t} \Big|_{t_0} = \mathbf{g}^T \cdot \frac{\partial \mathbf{s}_0(t)}{\partial t} \Big|_{t_0} \quad (28)$$

and (24) can be further expressed as

$$\bar{\mu}(f(t)) = f_u + \mathbf{g}^T \cdot (\mathbf{s}_0(t_0) - \mathbf{s}_{w,u}(t_0)) + \mathbf{g}^T \cdot \frac{\partial \mathbf{s}_0(t)}{\partial t} \Big|_{t_0} \cdot (t - t_0) \quad (29)$$

8.2 Prediction of $\beta_{w,u}(t)$

To predict $\beta_{w,u}(t)$, a first-order Taylor expansion of $\beta_{w,u}(t)$ with respect to t from t_0 is

$$\beta_{w,u}(t) = \beta_{w,u}(t_0) + \frac{d\beta_{w,u}(t)}{dt} \Big|_{t_0} \cdot (t - t_0) \quad (30)$$

where the sensitivity part, $\frac{d\beta_{w,u}(t)}{dt} \Big|_{t_0}$ can be derived using results from Section 8.1 as follows. Since at the worst-case point $\mathbf{s}_{w,u}(t)$, the corresponding level contour of $\mathbf{s}(t)$ is

$$\beta_{w,u}^2(t) = (\mathbf{s}_{w,u}(t) - \mathbf{s}_0(t))^T \cdot \mathbf{C}^{-1} \cdot (\mathbf{s}_{w,u}(t) - \mathbf{s}_0(t)) \quad (31)$$

It touches the performance boundary at $\mathbf{s}_{w,u}(t)$, which means the orthogonal on (31) is parallel to \mathbf{g} :

$$\mathbf{C}^{-1} \cdot (\mathbf{s}_{w,u}(t) - \mathbf{s}_0(t)) = \lambda \cdot \mathbf{g} \quad (32)$$

Inserting (32) into (31) we have

$$\beta_{w,u}^2(t) = \lambda^2 \cdot \mathbf{g}^T \cdot \mathbf{C} \cdot \mathbf{g} \quad (33)$$

By taking λ from (33) into (32) we obtain

$$(\mathbf{s}_{w,u}(t) - \mathbf{s}_0(t)) = \frac{\beta_{w,u}(t)}{\sqrt{\mathbf{g}^T \cdot \mathbf{C} \cdot \mathbf{g}}} \cdot \mathbf{C} \cdot \mathbf{g} \quad (34)$$

Then (34) is taken back into (22):

$$\mu(f(t)) = f_u - \beta_{w,u}(t) \cdot \sqrt{\mathbf{g}^T \cdot \mathbf{C} \cdot \mathbf{g}} \quad (35)$$

so that the worst-case distance at t can be expressed as

$$\beta_{w,u}(t) = \frac{f_u - \mu(f(t))}{\sqrt{\mathbf{g}^T \cdot \mathbf{C} \cdot \mathbf{g}}} \quad (36)$$

Then from (36) and (29) the worst-case distance degradation rate can be formulated as

$$\left. \frac{d\beta_{w,u}(t)}{dt} \right|_{t_0} = -\frac{1}{\sigma_f} \cdot \mathbf{g}^T \cdot \left. \frac{\partial \mathbf{s}_0(t)}{\partial t} \right|_{t_0} \quad (37)$$

which differs from (5) in (Sobe et al., 2009). From (37) it is clear that the evaluation of the worst-case distance degradation rate for a performance upper bound involves only multiple sensitivity evaluations which can be carried out efficiently. Especially in our case, both σ_f and \mathbf{g} remain constant, requiring an one-time evaluation only. The sensitivity of $\mathbf{s}_0(t)$ over t is calculated by finite-difference approximation. The values of $\mathbf{s}_0(t)$ at respective time points are obtained from exemplary aging simulator in our experiment described in Section 7, then the corresponding sensitivity and the worst-case distance degradation rate can be evaluated.

Thus, by taking (37) back into (30), the values of $\beta_{w,u}(t)$ at time t can be predicted efficiently without searching for the worst-case statistical parameters $\mathbf{s}_{w,u}(t)$ through iterative optimization method.

9. Experimental results

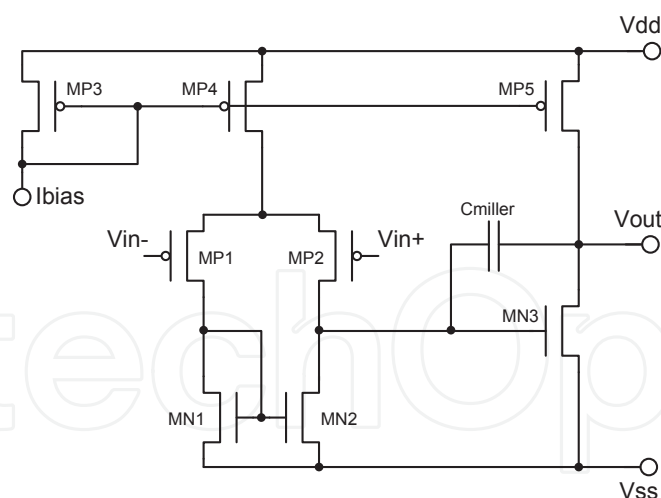


Fig. 7. Circuit topology of Miller OpAmp used in the experiment.

The circuit structure of the two stage Miller OpAmp used in the experiment is shown in Figure 7. The first stage is the differential stage, with the input differential pair, consisting of PMOS MP1 and MP2, and its active load, a current mirror consisting of NMOS MN1 and MN2. The second stage is a CMOS inverter with an NMOS MN3 as driver and a PMOS MP5 as its active load.

It is clear from the circuit structure that certain sizing constraints on transistors concerning the node voltages impose certain stress levels of each transistor.

9.1 Results of the new design flow

	yield-optimal		reliability-optimal	
	fresh	10 years	10 years	fresh
Gain \geq 80dB	4.0	3.9	3.9	3.9
Slew Rate $\geq 3V/\mu s$	4.2	1.9	3.4	5.8
GBW ≥ 2 MHz	5.8	5.7	5.8	5.9
Phase Margin $\leq 120deg$	5.2	4.3	5.1	5.9
Power $\leq 2mW$	5.9	5.8	6.2	6.6
CMRR \geq 80dB	3.4	2.2	3.3	4.2
Relative Area	100%		107%	
Lifetime Yield	99.96%	94.50 %	99.93%	99.99%

Table 2. Experimental results of the new design flow with reliability optimization.

We apply the new design flow in Figure 5 to the Miller OpAmp as introduced above. One of the stop criteria of the tool WiCkeD during fresh or lifetime yield optimization process, the maximum yield difference between two consecutive iterations, is set to 0.1%. That is, the fresh or lifetime yield optimization stops if the improvement of the yield value between two consecutive iterations is smaller than 0.1%. A 180nm technology is used with a supply voltage of 1.7V. The circuit is degraded to time $t=10$ years with example AgeMOS degradation model parameters inside RelXpert. The covariance matrix of statistical parameters is assumed to be constant over time. Table 2 shows the simulation results. Six of the performances are considered here, namely, DC Gain, Rising Slew Rate (SR), Gain-Bandwidth Product(GBW), Phase Margin, Power and Common-Mode Rejection Ratio (CMRR).

From result of fresh yield optimization we can see that the fresh circuit design is centered with 99.96% fresh yield, the corresponding design parameters are initial \mathbf{d} at t_0 . After degradation to 10 years with the same design parameters, all of the performances and worst-case distances will degrade, as well as the lifetime yield, which is only 94.50% now. Then a design centering on the degraded circuit is performed during lifetime yield optimization step. The result shows that the degraded circuit will have a lifetime yield of 99.93% with increased worst-case distances. Thus a design solution \mathbf{d} for optimal yield and reliability is found.

Verification result on last column shows that with this optimized design, fresh circuit at t_0 will be centered to a better position in terms of both fresh yield and lifetime yield. The fresh yield is 99.99%, and almost all of the worst-case distances here are much bigger compared to the fresh design where no degradation is considered.

For the price we pay for the more robust circuit, the approximated total area of the circuit layout is evaluated. For the area of a transistor, it is simply the product of the width and the length. For the area of the Miller capacitor, it is transformed into the corresponding area by a constant. The results in Table 2 show that 7% more relative layout area is needed for the more robust circuit.

9.2 Results of the prediction model

To verify the prediction model of (30), the lifetime worst-case distance values obtained from the tool WiCkeD and the prediction model are compared for two performances, SR and CMRR. The comparison results and relative errors at different t 's are plotted in Figure 8 and Figure 9. It is clear from the results that the prediction model can track the $\beta_w(t)$ degradation with an acceptable error. For the simulation time, it takes five minutes on average for WiCkeD to evaluate one $\beta_w(t)$ for one performance at t , while using the prediction model it takes only about forty seconds. A clear speedup about eight times is observed.

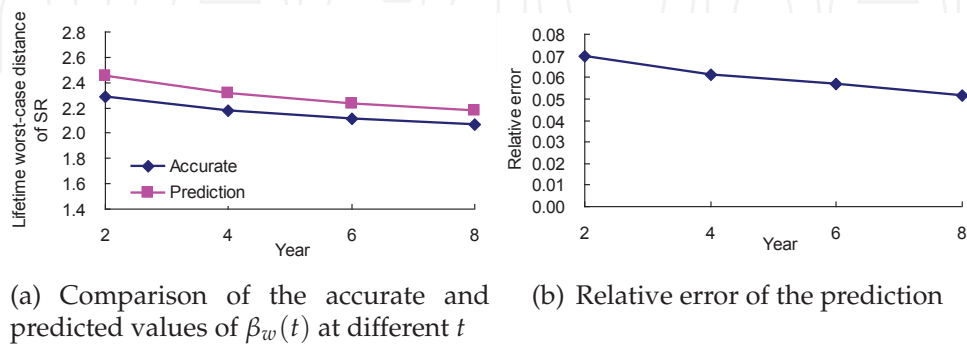


Fig. 8. Prediction results on SR

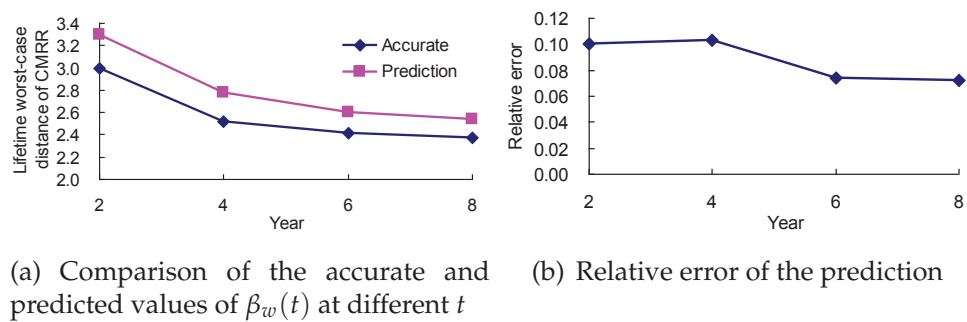


Fig. 9. Prediction results on CMRR

10. Conclusion

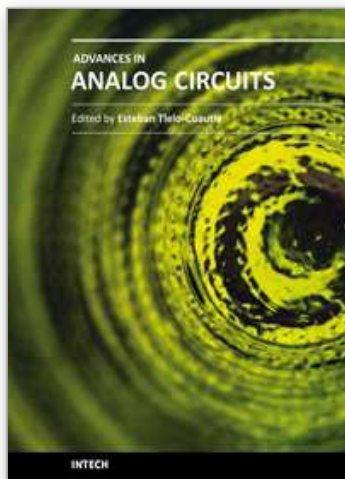
As semiconductor technology continuously scales, the joint effects of manufacturing process variations and parameter lifetime degradations have been a major concern for analog circuit designers, since the deviation of performance values from the nominal ones will impact both the fresh yield and lifetime yield. In this chapter, a new analog design flow with reliability optimization is presented. The effect of both process-induced parameter variation and time-dependent parameter degradation can be analyzed automatically. The remaining lifetime yield of the designed circuit can be predicted and optimized early in the design phase. After lifetime yield optimization, simulation results show that a more reliable design is achieved, tolerant of both process variation and lifetime degradation. A prediction model for the lifetime worst-case distances is proposed to speed up the analysis of lifetime worst-case distance values. The experimental results show that the model can

effectively evaluate during design phase the remaining lifetime yield of the circuits after degradation occurs in their lifetime.

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