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Behavioral Modeling of Mixed-Mode Integrated Circuits

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1. Introduction

Modeling is a preliminary work or construction that serves as a plan from which a final product can be made. Modeling at the transistor level of abstraction in the integrated circuit (IC) industry has roots in the primitives found in the popular simulation program with integrated circuit emphasis (SPICE). Although the SPICE models have evolved to increased accuracy, improvements in simulation speed have been small without going to higher levels of abstraction, rules and guidelines to enhance the design of modern analog integrated circuits (Alvarado et al., 2010; Beelen et al., 2010; Fakhfakh et al., 2010; McAndrew, 2010; Muñoz-Pacheco & Tlelo-Cuautle, 2009; S. Steinhorst & L. Hedrich, 2010).

Behavioral modeling is performed according to the kind of application, for example not only transistors models can be refined to work at radio frequency (RF) and microwave applications (Gaoua et al., 2010), but also integrated resistors can be refined to include parasitic effects (McAndrew, 2010). Additionally, transistors and parasitic elements can be modeled into hardware description languages (Alvarado et al., 2010), so that the development time of integrated circuits may be shrinked and the models can be tested before they are included into commercial simulators, namely SPICE and ELDO.

An important issue is the application of symbolic analysis to generate analytical expressions to describe the behavior of devices and circuits (Beelen et al., 2010; Tan & Shi, 2004). More recently, McConaghy & Gielen (2009) introduced a template-free symbolic performance modeling of analog circuits, mainly focused on operational transconductance amplifier

(OTA) based circuits. The application of symbolic analysis has also shown its usefulness in parasitic-aware optimization and retargeting of analog layouts (Lihong et al., 2008). In fact, the circuit design cycle covers different stages which can be performed in a hierarchical way, from the specifications down to the layout, and from the extraction of layout-parasitics up to the simulation of the whole circuit or system. In all cases, a refinement of the model is very much needed at low- and high-level of abstraction (Ruiz-Amaya et al., 2005; Vasilevski et al., 2009).

In some cases, symbolic analysis is combined with numerical simulation to perform semi-symbolic behavioral modeling (Balik, 2009). Other important issues in behavioral modeling of analog circuits is the generation of noise expressions (Martinez-Romero et al., 2010), and the determination of dominant circuit-elements for the design of low-voltage amplifiers (Tlelo-Cuautle, Martinez-Romero, Sánchez-López & X.-D. Tan, 2010).

Although many novel approaches for symbolic behavioral model generation have been introduced for analog circuits, as recently reported in (Fakhfakh et al., 2010), yet the generation of compact analytical expressions is an open problem. Some recent research has been oriented to apply model order reduction (MOR) techniques (Qin et al., 2005; Shi et al., 2006; Sommer et al., 2008; Tan & He, 2007), to capture the dominant behavior, but as already mentioned in (Shi et al., 2006), a reduced symbolic expression is very difficult to generate with MOR techniques. In this manner, this book chapter highlights some recent developments in applying symbolic analysis to generate behavioral models of mixed-mode integrated circuits (Bhadri et al., 2005; Krishna et al., 2007; McConaghy & Gielen, 2009; Sánchez-López, Fernández & Tlelo-Cuautle, 2010; Sánchez-López & Tlelo-Cuautle, 2009; Tan & Shi, 2004; Tlelo-Cuautle et al., 2009; Tlelo-Cuautle, Sánchez-López, Martinez-Romero & Tan, 2010; Tlelo-Cuautle, Sánchez-López & Moro-Frias, 2010).

In the following sections, we show the generation of behavioral models of mixed-mode devices and circuits. This process is performed by using the nullor element to describe the topology of the active devices and by applying symbolic nodal analysis to compute the analytical expressions of the devices and circuits. Furthermore, to show the usefulness of the generated symbolic behavioral models, they are used in the design process of an oscillator, for which some insigths are derived in order to determine the circuit-element values and to speed up circuit simulation. The chapter finishes by discussing some issues related to the application of MOR techniques to approximate the dominant behavior of mixed-mode circuits, and the generation of symbolic models including noise and distortion behavior.

2. Mixed-mode devices

In the analog domain, the input and output transfer relationships can be expressed by two kinds of signals: voltage and current. When the signals are voltages, the device or circuit is working in voltage-mode. This is the case of operational amplifier based circuits. On the other hand, when the signals are currents, the device or circuit is working in current-mode. However, when the device or circuit drives both voltage and current signals, it is working in mixed-mode.

The first active device allowing the transfer of voltage and current was introduced in 1968 (Smith & Sedra, 1968), it was named current conveyor. Nowadays, the current conveyor has evolved into three generations with direct and inverting characteristics (Tlelo-Cuautle, Sánchez-López & Moro-Frias, 2010). All kinds of current conveyors work in mixed-mode and basically they are composed of unity gain cells (Soliman, 2009; Tlelo-Cuautle, Duarte-Villaseñor & Guerra-Gómez, 2008), which can be superimposed (Tlelo-Cuautle,

Moro-Frias & Duarte-Villaseñor, 2008) to generate different kinds of active devices (Biolek et al., 2008), all of them useful for analog signal processing applications. Among the unity gain cells, the voltage mirror (Tlelo-Cuautle, Duarte-Villaseñor & Guerra-Gómez, 2008) and current mirror can be modeled by using nullators and norators (Tlelo-Cuautle, Sánchez-López, Martinez-Romero & Tan, 2010), but also they have the pathological representation introduced in (Saad & Soliman, 2010), and they can be used to model the behavior of active devices with inverting characteristics.

Although the current conveyor is a mixed-mode device, it can be used to implement voltage-mode circuits such as active filters (Chen, 2010; Maheshwari et al., 2010). Some mixed-mode integrated circuits implemented with other active devices can be found in (and A. Bentrcia and S.M. Al-Shahrani, 2004; Bhadri et al., 2005; Soliman, 2007), and one approximation to generate their behavioral models is given in (Krishna et al., 2007). The modeling of all kinds of active devices by using controlled-sources can be found in (Biolek et al., 2008). However, that models may generate systems of equations bigger than by using nullors. For instance, in Fig. 1 are shown the models of the operational amplifier, OTA and negative-type second generation current conveyor (CCII- (Tlelo-Cuautle, Sánchez-López & Moro-Frias, 2010)), using nullors.

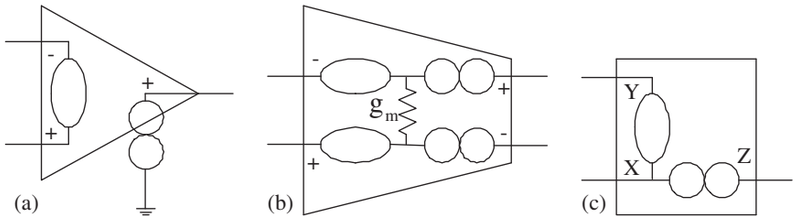


Fig. 1. Modeling the (a) operational amplifier (opamp), (b) operational transconductance amplifier (OTA), and (c) negative-type second generation current conveyor (CCII-) using nullors

From the properties of the nullator whose voltage and current are zero (Sánchez-López, Fernández & Tlelo-Cuautle, 2010), and for the norator whose voltage and current are arbitrary, the active devices shown in Fig. 1 have the following relationships:

- From Fig. 1(a), the voltage and current at the input port of the opamp are zero due to the properties of the nullator. At the output port, the voltage and current can be infinity due to the property of the norator. Then, the ideal behavior of the opamp is well described by using one nullator and one norator.
- From Fig. 1(b), the voltage across the conductance g_m is just the differential voltage at the input port because the voltage across each nullator is zero. Further, the current through g_m is the one leaving the output port of the OTA, i.e. $i_o = g_m(v^+ - v^-)$, where $v^+ - v^-$ is the differential voltage at the input port of the OTA.
- From Fig. 1(c), the property of the nullator generates $i_Y = 0$ and $v_X = v_Y$, while the property of the norator allows $i_Z = -i_X$. These three equations describe the ideal behavior of the CCII-.

Among the mixed-mode active devices, the positive-type second generation current conveyor (CCII+) is very versatile because if it is connected with a voltage follower, they describe the current-feedback operational amplifier (CFOA). Both the CCII+ and CFOA are useful to realize linear and nonlinear circuits (Sánchez-López, Trejo-Guerra, Muñoz-Pacheco &

Tlelo-Cuautle, 2010; Trejo-Guerra et al., 2010). Other useful mixed-mode active devices are the transimpedance amplifier (van der Horst et al., 2010), operational transresistance amplifier (OTRA) and current operational amplifier (COA) (Sánchez-López, Fernández & Tlelo-Cuautle, 2010). In the following section we show how to generate the fully-symbolic behavioral model of amplifiers and oscillators by including parasitic effects of the active devices. For instance, when the analog circuits are modeled using nullors, their input-output relationships can be generated by applying the symbolic nodal analysis (NA) method given in (Sánchez-López et al., 2008; Sánchez-López & Tlelo-Cuautle, 2009; Tlelo-Cuautle et al., 2009; Tlelo-Cuautle, Sánchez-López & Moro-Frias, 2010). The models used are very useful for low frequency behavior, but for high frequency behavior yet one needs to investigate how to approximate the gain, poles and zeros, noise and distortion. These aspects are discussed in the following sections.

3. Behavioral modeling of analog circuits using pathological elements

Behavioral modeling has shown its advantages for successful development of analog electronic design automation (EDA) tools due to various types of systems that can be represented by means of an abstract model (Muñoz-Pacheco & Tlelo-Cuautle, 2009). The abstraction levels indicate the degree of detail specified about how a function is to be implemented. Therefore, behavioral models try to capture as much circuit functionality as possible with far less implementation details than the device-level description of the circuit. Some recent developments related to symbolic behavioral modeling can be found in (Fakhfakh et al., 2010).

The generation of behavioral models is very useful to perform different design tasks, such as synthesis (Saad & Soliman, 2008) and sizing (Diaz-Madrid et al., 2008). The applications to analog design also include behavioral modeling of power (Suissa et al., 2010), carbon nanotube field-effect-transistors (Chek et al., 2010), statistical modeling (Li et al., 2010), efficient RF/microwave transistor modeling (Gaoua et al., 2010), etc. In all cases, the goal is not only to capture the dominant behavior (Beelen et al., 2010), but also to generate refined models to enhance high-level simulation (Alvarado et al., 2010; Vasilevski et al., 2009). The refinement helps to approximate the behavior of circuits with strong nonlinearities (McAndrew, 2010; S. Steinhorst & L. Hedrich, 2010), and to improve timing analysis (Hao & Shi, 2009), for instance. The application of symbolic behavioral modeling approaches allows to perform sensitivity analysis (Shi & Meng, 2009), which can be very useful to determine design-limits in designing nonlinear circuits. For example, to determine the tuning range of mixed-mode quadrature oscillators (Ansari & Maheshwari, 2009), the phase margin of opamps (Pugliese et al., 2010), to identify the dominant circuit-elements in low-voltage amplifiers (Tlelo-Cuautle, Martinez-Romero, Sánchez-López & X.-D. Tan, 2010), and to identify the noisy elements at the transistor level of design (Martinez-Romero et al., 2010).

From the advantages infered above, we present the symbolic behavioral modeling of analog circuits using the pathological elements: nullators and norators. The other two pathological elements: voltage mirrors and current mirrors can be described as already shown in (Saad & Soliman, 2010; Tlelo-Cuautle, Sánchez-López, Martinez-Romero & Tan, 2010).

Some examples for the generation of behavioral models for mixed-mode devices and circuits are introduced in (Fakhfakh et al., 2010; Sánchez-López, Fernández & Tlelo-Cuautle, 2010; Tlelo-Cuautle, Sánchez-López, Martinez-Romero & Tan, 2010; Tlelo-Cuautle, Sánchez-López & Moro-Frias, 2010). In this subsection we show the model generation for simple low-voltage amplifiers using the pathological elements nullators and norators (Tlelo-Cuautle,

Martinez-Romero, Sánchez-López & X.-D. Tan, 2010), because they are quite useful to perform symbolic analysis by applying only nodal analysis (NA). Furthermore, to generate a symbolic behavioral model we should replace every transistor and every non-NA-compatible circuit element with their nullor-equivalent, as already shown in (Tlelo-Cuautle et al., 2009). Here, we summarize the NA formulation ($i = Yv$) of analog circuits modeled with nullors.

1. Describe the interconnection relationships of norators (P_j), nullators (O_j), and admittances by generating tables including names and nodes.
2. Calculate indexes associated to set row and column to group grounded and floating admittances:
   - ROW: Contains all nodes ordered by applying the norator property which nodes (m, n) are virtually short-circuited. These indexes are used to fill vector i and the admittance matrix Y.
   - COL: Contains all nodes ordered by applying the nullator property which nodes (m, n) are virtually short-circuited. These indexes are used to fill vector v and the admittance matrix Y.
   - Admittances: They are grouped into two tables: Table A includes all nodes (ordered), and in each node is the sum of all admittances connected to it. Table B includes all floating admittances and its nodes (m, n).
3. Use sets ROW and COL to fill vectors i and v, respectively. To fill Y: if in Table A a node is included in ROW and COL, introduce that admittance(s) in Y at position (ROW index, COL index). For each admittance in Table B, search node m in ROW and n in COL (do the same but search n in ROW and m in COL), if both nodes exist the admittance is introduced in Y at position (ROW index, COL index), and it is negative.

The solution of the NA formulation can be obtained by applying determinant decision diagrams (DDD) (Fakhfakh et al., 2010; Tan & Shi, 2004).

Now we are able to generate the symbolic behavioral model of low-voltage amplifiers. Let's consider the common source amplifier with an active load shown in Fig. 2(a). Our goal is to obtain its behavioral model expressed as a fully symbolic transfer function (Tlelo-Cuautle, Martinez-Romero, Sánchez-López & X.-D. Tan, 2010). The first step consists to obtain its nullor equivalent, which is shown in Fig. 2(b), where the input signal is the current source emulating the voltage v_{in}. As it can be seen, the input voltage from Fig. 2(a) was converted into a current source using one nullator, one norator and one unity-resistor, making it an NA-compatible element, i.e. an element which can be stamped directly into the nodal analysis formulation, and also it does not increase the order of the system of equations, as already shown in (Fakhfakh et al., 2010; Sánchez-López, Fernández & Tlelo-Cuautle, 2010; Tlelo-Cuautle et al., 2009; Tlelo-Cuautle, Martinez-Romero, Sánchez-López & X.-D. Tan, 2010; Tlelo-Cuautle, Sánchez-López, Martinez-Romero & Tan, 2010; Tlelo-Cuautle, Sánchez-López & Moro-Frias, 2010).

The interconnection relationships of the nullators and norators is shown in Table 1, from which the sets COL and ROW are generated as: COL ={(1,2,3),(4,5)}, and ROW = {(1),(3,4,5)}. This means that the order of the admittance matrix is 2×2. The admittances are listed as shown in Table 2, where only one admittance is floating. The formulation of the system of equations is given by (1), and the solution for the behavioral model, i.e. the voltage transfer function, is given by (2).

$$\begin{bmatrix} 1 & 0 \\ g_{m1} - sC_{gd1} & s(C_{gd1} + C_{gs2}) + g_{o1} + g_{o2} + g_{m2} \end{bmatrix} \begin{bmatrix} v_{1,2,3} \\ v_{4,5} \end{bmatrix} = \begin{bmatrix} v_{in} \\ 0 \end{bmatrix} \quad (1)$$

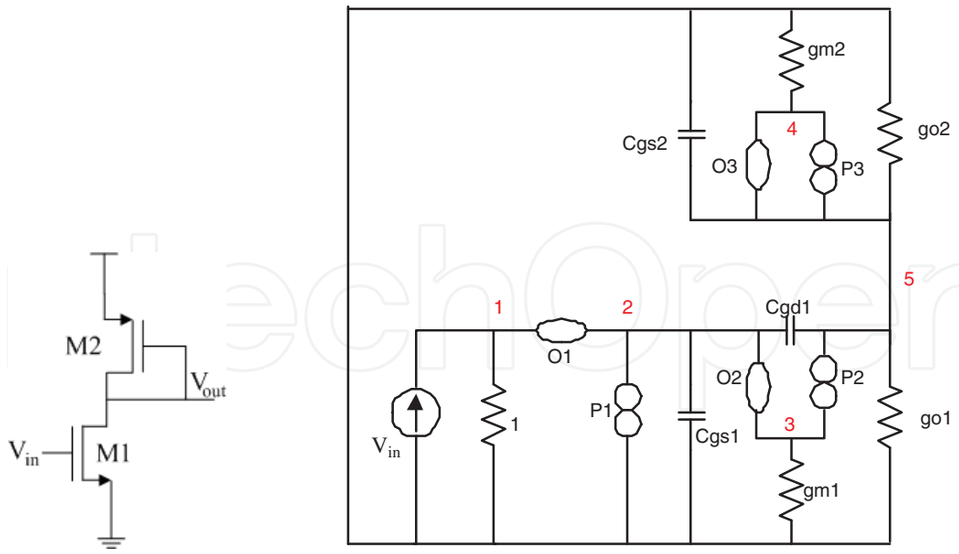


Fig. 2. (a) Low voltage amplifier with active load, and (b) Nullor equivalent.

Nullator	Nodes	Norator	Nodes
O1	1,2	P1	2,0
O2	2,3	P2	3,5
O3	4,5	P3	4,5

Table 1. Data structure of nullators and norators from Fig. 2(b).

Table A		Table B	
Node	Grounded Admittances	Nodes	Floating Admittances
1	1	2,5	sC_{gd1}
2	sC_{gs1}+sC_{gd1}		
3	g_{m1}		
4	g_{m2}		
5	$g_{o1} + g_{o2} + sC_{gd1} + sC_{gs2}$		

Table 2. Data structure of admittances from Fig. 2(b).

$$\frac{v_o}{v_{in}} = -\frac{g_{m1} - sC_{gd1}}{s(C_{gd1} + C_{gs2}) + g_{o1} + g_{o2} + g_{m2}} \tag{2}$$

Another example is taken from (Sanchez-Sinencio, 2009), the three stages uncompensated low-voltage amplifier shown in Fig. 3, which nullor equivalent is given in Fig. 4. To formulate the admittance matrix, we follow the steps provided above so that the sets COL and ROW are (Tlelo-Cuautle, Martinez-Romero, Sánchez-López & X.-D. Tan, 2010): COL = {(1,3,4), (2,8,9), (5,6,7), (10,13), (11), (15,16), (18)}, and ROW = {(1), (2), (4,5,6), (7,9,10), (11,12), (13,14,15), (17,18)}. The admittance matrix is of order 7×7, and it is shown by (3). Following the steps provided at the beginning of this section, the symbolic behavioral model, i.e. the transfer function is given by (4). As one sees, the symbolic expression is very large, and it was generated by using simple nullor equivalentes for the MOSFETs, i.e. every MOSFET from

Fig. 3 was modeled only with a nullor and its transconductance (some MOSFETs include the output conductance to minimize error according to (Tlelo-Cuautle, Martinez-Romero, Sánchez-López & X.-D. Tan, 2010)). Furthermore, were the parasitic capacitors of every MOSFET be used, the expression in (4) becomes huge. A further step should be performed to simplify large symbolic expressions which can also be done by applying model order reduction approaches as shown in the following section.

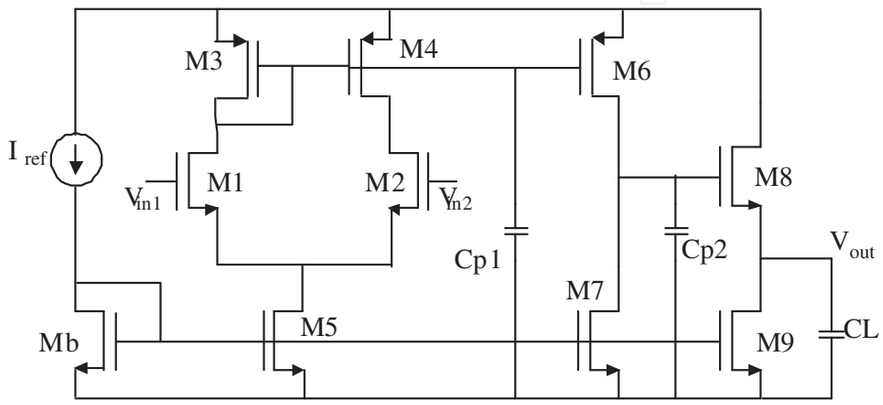


Fig. 3. Three stages uncompensated low voltage amplifier.

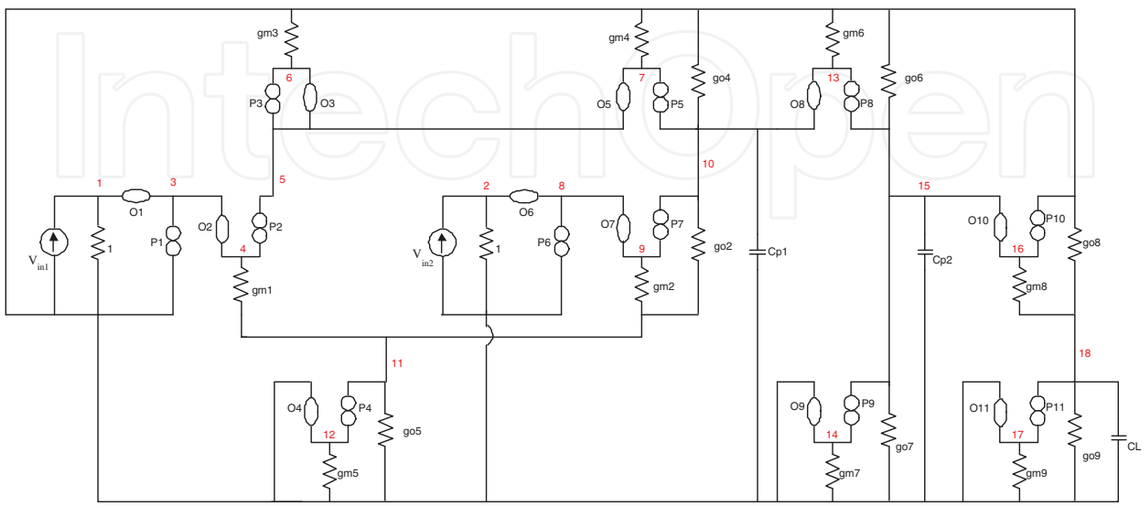


Fig. 4. Nullor equivalent from Fig. 3.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ g_{m1} & 0 & g_{m3} & 0 & -g_{m1} & 0 & 0 \\ 0 & g_{m2} & g_{m4} & g_{o2}+g_{o4}+sC_{p1} & -g_{o2}-g_{m2} & 0 & 0 \\ -g_{m1} & -g_{m2} & 0 & -g_{o2} & g_{m1}+g_{m2}+g_{o2} & 0 & 0 \\ 0 & 0 & 0 & g_{m6} & 0 & g_{o6}+g_{o7}+sC_{p2} & 0 \\ 0 & 0 & 0 & 0 & 0 & -g_{m8} & g_{o8}+g_{o9}+g_{m8}+sC_L \end{bmatrix} \tag{3}$$

$$\frac{v_o}{v_{in}} = -\frac{g_{m8}g_{gm6}g_{m1}(g_{m3}g_{o2}+g_{m3}g_{m2}+g_{m4}g_{o2}+g_{m4}g_{m2})}{D(s)} \tag{4}$$

D(s)=*gm2 gm3 go4 go6 go9+gm1 gm3 go2 go7 go9+gm1 gm3 go2 go7 gm8+ (gm1 gm3 go2 go6 CL+ gm2 gm3 go4 Cp2 go8+ gm2 gm3 go4 Cp2 go9+gm2 gm3 go4 go6 CL+gm1 gm3 Cp1 go7 go9+ gm1 gm3 Cp1 go7 gm8+go2 gm3 go4 Cp2 go9+go2 gm3 go4 Cp2 go8+go2 gm3 Cp1 go6 go9+ go2 gm3 Cp1 go6 gm8+go2 gm3 go4 go6 CL+go2 gm3 go4 go7 CL+gm4 gm1 go2 Cp2 go9+ gm2 gm3 Cp1 go7 go8+gm2 gm3 Cp1 go7 go9+gm2 gm3 Cp1 go7 gm8+gm4 gm1 go2 go6 CL+ gm4 gm1 go2 go7 CL+gm4 gm1 go2 Cp2 go8+go2 gm3 go4 Cp2 gm8+go2 gm3 Cp1 go6 go8+ go2 gm3 Cp1 go7 go8+go2 gm3 Cp1 go7 go9+go2 gm3 Cp1 go7 gm8+gm1 gm3 go4 Cp2 go8+ gm1 gm3 go4 Cp2 go9+gm1 gm3 go2 go7 CL+gm1 gm3 go2 Cp2 go8+gm1 gm3 go2 Cp2 go9+ gm4 gm1 go2 Cp2 gm8+gm1 gm3 go4 Cp2 gm8+gm1 gm3 Cp1 go6 go8+gm1 gm3 Cp1 go6 go9+ gm1 gm3 Cp1 go6 gm8+gm1 gm3 Cp1 go7 go8+gm2 gm3 Cp1 go6 go9+gm2 gm3 Cp1 go6 gm8+ gm1 gm3 go2 Cp2 gm8+gm1 gm3 go4 go6 CL+gm1 gm3 go4 go7 CL+gm2 gm3 go4 go7 CL+ gm2 gm3 go4 Cp2 gm8+gm2 gm3 Cp1 go6 go8) s+gm2 gm3 go4 go6 go8+gm2 gm3 go4 go6 gm8+ go2 gm3 go4 go6 gm8+ (gm2 gm3 Cp1 Cp2 CL+gm1 gm3 Cp1 Cp2 CL+go2 gm3 Cp1 Cp2 CL) s^3 +gm1 gm3 go4 go6 gm8+ gm1 gm3 go4 go7 go8+gm1 gm3 go4 go7 go9+gm1 gm3 go4 go7 gm8+ gm4 gm1 go2 go6 gm8+gm2 gm3 go4 go7 go8+gm2 gm3 go4 go7 go9+gm2 gm3 go4 go7 gm8+ gm4 gm1 go2 go7 go9+gm4 gm1 go2 go7 gm8+ (gm1 gm3 Cp1 Cp2 go8+gm2 gm3 Cp1 Cp2 go9+ gm1 gm3 Cp1 go7 CL+gm1 gm3 Cp1 Cp2 go9+go2 gm3 Cp1 Cp2 gm8+gm1 gm3 Cp1 Cp2 gm8+ go2 gm3 Cp1 Cp2 go9+gm2 gm3 go4 Cp2 CL+go2 gm3 Cp1 Cp2 go8+gm2 gm3 Cp1 Cp2 go8+ gm2 gm3 Cp1 Cp2 gm8+go2 gm3 go4 Cp2 CL+go2 gm3 Cp1 go6 CL+gm2 gm3 Cp1 go6 CL+ gm1 gm3 go2 Cp2 CL+gm1 gm3 go4 Cp2 CL+go2 gm3 Cp1 go7 CL+gm2 gm3 Cp1 go7 CL+ gm4 gm1 go2 Cp2 CL+gm1 gm3 Cp1 go6 CL) s^2+gm4 gm1 go2 go6 go9+go2 gm3 go4 go6 go8+ go2 gm3 go4 go7 gm8+go2 gm3 go4 go6 go9+go2 gm3 go4 go7 go8+go2 gm3 go4 go7 go9+ gm4 gm1 go2 go7 go8+gm1 gm3 go2 go6 go8+gm1 gm3 go2 go6 go9+gm1 gm3 go2 go6 gm8+ gm1 gm3 go2 go7 go8+gm1 gm3 go4 go6 go8+gm1 gm3 go4 go6 go9+gm4 gm1 go2 go6 go8*

If the low voltage amplifier is designed with standard CMOS integrated circuit technology, its gain performance comparison with respect to its behavioral model given by (4) is shown in Fig. 5. To minimize the error it is necessary to include more symbolic elements, as shown in the following section. However, the symbolic expression becomes huge originating a trade-off between the size of the exact symbolic behavioral model and the allowed error compared with HSPICE simulation.

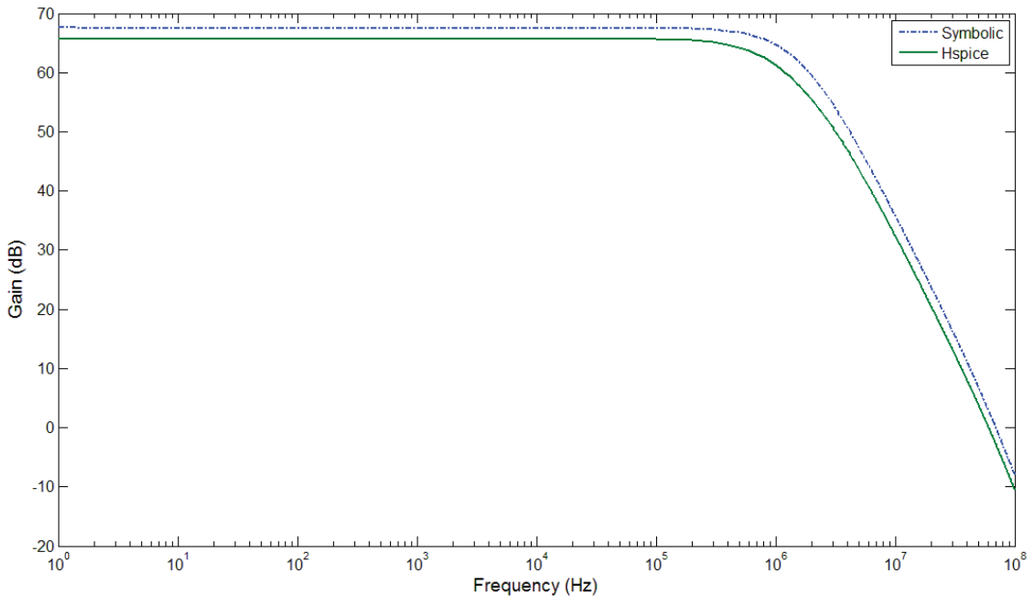


Fig. 5. Comparison between HSPICE and (4).

4. Simplification approaches

To simplify the symbolic expression given in (4), several approaches can be found in (Fakhfakh et al., 2010). Those approaches combine numerical and symbolic techniques to reduce the analytical expression. For instance, the expression reduction can be performed by the application of three complementary methods: simplification before generation (SBG) techniques (negligible elements are pruned from the circuit, graph or matrix associated to the circuit equation formulation); simplification during generation (SDG) techniques (only the significant parts of the symbolic expressions are generated); and simplification after generation (SAG) techniques (least significant terms are pruned from the symbolic expression resulting from the previous approximate analysis steps).

Both, SBG and SDG approaches are usually tied to the kind of analysis method used. In this way, some SBG methods operate at the matrices resulting from analysis methods like nodal analysis. The approaches in (Hsu & Sechen, 1994; Sommer et al., 1993) eliminate device parameters from each cofactor of the nodal matrix if the error induced in the cofactor is below a given error threshold. Concurrently with the device parameter elimination, this technique tries to reduce determinant dimension by factoring out rows and columns with only one nonzero entry and performs row and column operations to reduce the number of symbols or nonzero entries. Other methods by (Guerra et al., 1998; Yu & Sechen, 1996) operate at the graph level; usually, the voltage and current graphs, as the two-graph method has been demonstrated to be the most efficient symbolic analysis method (Wambacq et al., 1996). In this case, graph branches are removed or its terminal nodes are contracted if their contribution (appropriately) measured to the transfer function is sufficiently small. In all cases, an adequate error mechanism is needed to control which matrix entries can be deleted or graph branches can be deleted and graph nodes contracted without exceeding some prescribed maximum magnitude/phase errors. Most approaches (Hsu & Sechen, 1994; Sommer et al., 1993; Yu & Sechen, 1996) perform the evaluation of the contributions to the network function of the elimination of matrix entries or the successive node contractions and branch removals at a set

of frequency samples within the range being considered. An obvious trade-off between the number of frequency samples (directly related to computational time) and the possibility of exceeding the maximum errors between frequency samples exist. An exception is the efficient approach in (Fernández et al., 1998; Guerra et al., 1998; Rodriguez-Garcia et al., 1999), that selects a small set of frequency samples, uses interval analysis techniques to detect if the error is exceeded in some intermediate frequency and new frequency samples are added accordingly.

SDG techniques generate symbolic terms in decreasing order of magnitude until the number of terms is enough to model the behavior of the circuit with a given accuracy. Term generation algorithms in decreasing order of magnitude were originally developed for the two-graph approach. The modeling of analysis problems in terms of matroids has allowed the term generation with many other methods but the two-graph (voltage and current graph) method still remains as the most efficient one. Valid symbolic terms corresponds to ordered enumeration of common spanning trees to both graphs, that in terms of matroids it corresponds to the ordered enumeration of bases common to two graphic matroids. If the terms must belong to a given power of the complex frequency s of functions like (2) and (4), then the bases must be also common to a partition matroid, determined by spanning trees that have a fixed number of frequency-dependent elements. Although there are efficient algorithms for the ordered enumeration of bases common to two matroids, the ordered enumeration of bases common to three matroids is in general a NP-complete problem. The possible alternatives are linked to the error control mechanism used:

- Enumerate bases common to the partition matroid and one of the graphic matroids, and for each one, check if it is also a base of the other graphic matroid (Wambacq et al., 1995; Yu & Sechen, 1995). The generation algorithm is most efficient known but many generated bases may not be common to the three matroids. In this case, error mechanisms that control the error in each coefficient of the transfer function can be used, for instance, by means of a sensitivity driven mechanism (Daems et al., 1999).
- Enumerate bases common to the two graphic matroids (therefore, admittance of frequency dependent elements must be evaluated at a given frequency) and for each one, check if it contains the required number of frequency-dependent elements. The frequency can be selected via a sensitivity-driven mechanism that increases the probability of generation of terms with the desired number of frequency-dependent elements (Wambacq et al., 1998). The same error control mechanism than in the previous case can be used.
- Enumerate bases common to the two graphic matroids for a given frequency. One possibility is to enumerate bases at several frequencies and merge the results (Yu & Sechen, 1997). Another possibility to avoid the use of an excessive number of frequencies, generation of unnecessary terms and possible error excesses between frequency samples is to use a similar sampling approach and error control mechanism to the SBG case: a reduced number of samples, detection of error excesses by interval analysis and step-by-step addition of sampling frequencies (Guerra et al., 1998).

Special attention deserves the approximation of symbolic poles and zeros of transfer functions. Extraction of poles and zeros from symbolic transfer functions is subject to strong limitations for two reasons:

1. The maximum polynomial order that can be extracted analytically is limited to four (in practice, for symbolic roots it is limited to two);

2. Approximation of the transfer function under magnitude and phase error control mechanisms does not map to controlled pole and zero errors.

For these reasons, more powerful approaches specifically devoted to symbolic pole and zero extraction have been developed. One of these techniques (Henning, 2002) applies a simplification before generation technique based on the approximation of the nodal admittance matrix for a selected eigenvalue by ranking the eigenvalue shifts induced by different device parameter eliminations and performing the least significant device prunings while some error criterion in the eigenvalue shift is met. The eigenvalue shift is obtained from a linear prediction formula derived from a Taylor series approximation of the generalized eigenvalue problem, similar to the sensitivity analysis above, yielding a ranking of candidate parameter eliminations. The approach in (Guerra et al., 2002) exploits the Haley's modification-decomposition method (Haley, 1991) to transform the generalized eigenvalue problem into a standard eigenvalue problem. This new formulation can use the efficient QR algorithm to numerically track pole and zero errors, and it contains a time-constant matrix whose entries can be calculated symbolically very efficiently. This opens the possibility to apply simplification before generation techniques at the matrix level (by selecting only the appropriate entries of matrix T, entries that correspond to analysis of simple, purely resistive circuits), simplification before generation techniques at the circuit level (by eliminating negligible devices of the resistive circuit associate to each entry of interest) and simplification during generation techniques at the circuit level (by applying conventional SDG techniques to simplified, purely resistive circuits).
Model order reduction (MOR) technique is another simplification approach (Qin et al., 2005; Shi et al., 2006; Tan & He, 2007). Besides, the technique based on the asymptotic waveform evaluation (AWE) approach (Qin et al., 2005; Tan & He, 2007), can be applied to reduce the order of the behavioral model either symbolic (Shi et al., 2006), or numerically (Sommer et al., 2008). In the rest of this section we show the drawbacks when performing a fully-symbolic AWE approach. Let's us consider the circuit in Fig. 3, by replacing each MOSFET with its nullor equivalent including two parasitic capacitors (connected between gate-source and gate-drain), the nullor circuit is shown in Fig. 6. Compared to the nullor circuit in Fig. 4, in this case there are many floating admittances, so that the system of equations grows and so the size of the symbolic behavioral model.
For this example, the ROW and COL sets are: ROW = (1), (2), (4,5,6), (7,9,10), (11,12), (13,14,15), (17,18), and COL = (1,3,4), (2,8,9), (5,6,7), (10,13), (11), (15,16), (18). Twelve admittances are floating ones, so that the formulation includes the generation of Table A and Table B, as it was done for the low voltage amplifier with active load described above.
The generation of the fully symbolic transfer function from Fig. 6 leads to a fifth order denominator. For instance, when the uncompensated amplifier is designed with standard CMOS integrated circuit technology, and by replacing every symbol-circuit-element with its numerical value computed from an HSPICE simulation, the rational "s-domain" fifth order function is given by (5).

$$H(s) = \frac{1536(2.38E8s^5 + 2.75E20s^4 - 4.4E30s^3 - 4.19E41s^2 - 5.69E51s - 1.94858E61)}{7.67E18s^5 + 1.32E29s^4 + 3.5E38s^3 + 1.51E41s^2 + 3.29E54s + 1.29637E61} \quad (5)$$

Besides, usually a second order polynomial is very sufficient to approach the behavior of an amplifier in analog design. In this manner, AWE is very useful to generate a reduced order behavioral model through Padé approximation. The main operations can be found in (Qin

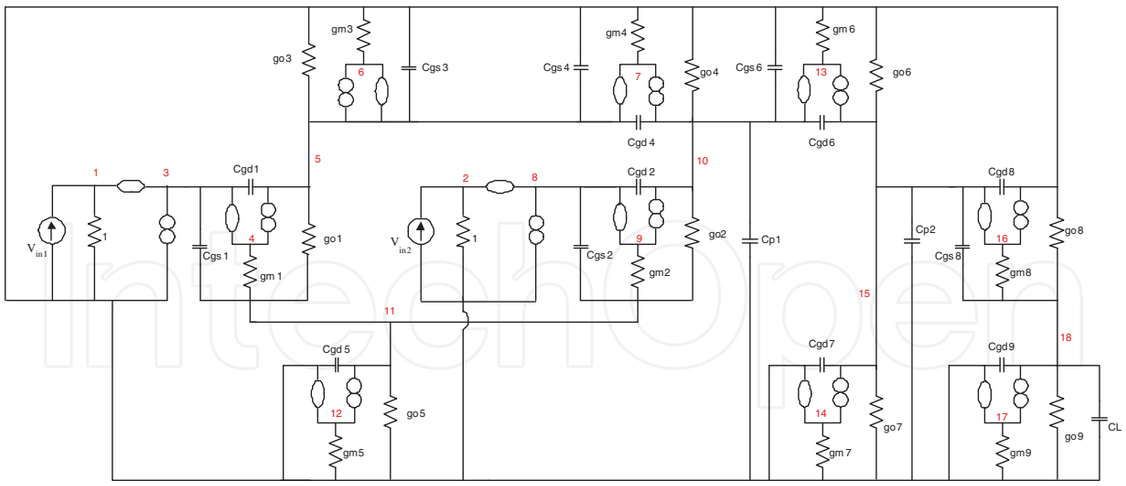


Fig. 6. Nullor equivalent from Fig. 3 including parasitic capacitors to all MOSFETs.

et al., 2005; Tan & He, 2007). Basically, from the computation of the symbolic transfer function (H(s)), one evaluates derivatives to compute moments with respect to the variable "s". The iterative formula is given by (6).

$$m_k = \frac{1}{k!}\frac{d^k H(s)}{ds^k}|_{s=0} \tag{6}$$

Afterwards, Padé approximation generates an expression with reduced order of the form:

$$H_{p,q}(s) = \frac{P(s)}{Q(s)} = \frac{a_0 + a_1 s + a_2 s^2 + \ldots + a_p s^p}{1 + b_1 s + b_2 s^2 + \ldots + b_q s^q} \tag{7}$$

The coefficients a_p and b_q can be obtained by solving two system of equations, for numerator and denominator, respectively. As already described in (Tan & He, 2007). As one can infer, doing this work fully-symbolically to generate a fully-symbolic behavioral model instead of the rational expression in (5), is very time-consuming and it requieres a lot of memory. For instance, the fully symbolic moment m_0 is given by a very large expression where the numerator is espressed as:

-gm8 gm6 gm1 (go3 gm2+go2 gm4+go3 go2+gm3 gm2+gm2 gm4+gm3 go2+go5 gm4)

And the denominator is expressed by:

go1 gm3 go2 go7 gm8+go8 go6 go1 go2 go3+go1 gm2 go4 go6 go9+go1 go5 go4 go6 gm8+go1 gm4 go2 go7 go8+ go1 gm2 go4 go6 go8+go1 go5 go4 go6 go9+go1 go5 go2 go6 go9+go1 gm3 go4 go7 gm8+go1 go2 go4 go6 go9+ go1 go3 go2 go6 gm8+go8 go6 go1 go2 gm3+go8 go7 go1 go2 gm3+go9 go7 go1 go2 gm3+ go1 gm4 go2 go6 go8+ go1 gm3 go2 go6 gm8+go1 gm4 go2 go7 go9+go1 go5 go2 go6 go8+go9 go6 go1 go2 go3+go1 go5 go2 go6 gm8+ go1 go3 go4 go7 gm8+go1 go5 go4 go7 gm8+go9 go6 go1 go2 gm3+go1 gm2 go4 go6 gm8+go1 gm2 go4 go7 go8+ go1 go3 go4 go6 gm8+go1 gm2 go4 go7 gm8+go8 go7 go1 go2 go3+ go1 go2 go4 go7 gm8+go1 go3 go2 go7 gm8+ go1 gm4 go2 go7 gm8+go1 gm4 go2 go6 gm8+go1 go5 go2 go7 go8+go1 gm3 go4 go6 go8+go9 go7 go1 go2 go3+ go1 gm4 go2 go6 go9+go1 gm3 go4 go6 go9+go1 gm3 go4 go7 go8+go1 go2 go4 go6 gm8+go3 gm1 go2 go6 go8+ go3 gm1 go2 go7 go8+go3 gm1 go2 go7 go9+ go3 gm1 go2 go7 gm8+go3 gm1 go2 go6 go9+go3 gm1 go2 go6 gm8+ go3 gm1 go4 go6 gm8+go3 go2 go4 go7 go9+gm3 go5 go4 go7 gm8+go3 go5 go2 go6 go8+go3 go5 go2 go7 go8+ go3 go5 go2 go7 go9+go3 go5 go2 go7 gm8+go3 go5 go2 go6 go9+go3 go5 go2 go6 gm8+gm3 go5 go2 go7 go9+

gm3 go5 go4 go6 gm8+ go3 gm2 go4 go6 gm8+go3 go5 go4 go6 gm8+go3 gm1 go4 go6 go9+go3 gm1 go4 go6 go8+ go3 gm1 go4 go7 go8+go3 gm1 go4 go7 go9+go3 gm2 go4 go6 go9+go3 gm2 go4 go6 go8+go3 gm2 go4 go7 go8+ go3 gm2 go4 go7 go9+go3 go2 go4 go7 gm8+gm3 gm1 go2 go6 go8+gm3 gm1 go2 go7 go8+gm3 gm1 go2 go7 go9+ gm3 gm1 go2 go7 gm8+gm3 gm1 go2 go6 go9+gm3 gm1 go2 go6 gm8+go3 go5 go4 go6 go9+go3 go5 go4 go6 go8+ go3 go5 go4 go7 go8+go3 go5 go4 go7 go9+gm3 gm1 go4 go6 gm8+gm3 gm2 go4 go6 go9+gm3 gm2 go4 go6 go8+ gm3 gm2 go4 go7 go8+gm3 gm2 go4 go7 go9+gm3 gm2 go4 go6 gm8+gm3 go5 go2 go6 go8+ gm3 go5 go2 go7 go8+ gm3 go5 go2 go7 gm8+gm3 go5 go2 go6 go9+gm3 go5 go2 go6 gm8+go3 gm1 go4 go7 gm8+go3 go2 go4 go6 gm8+ gm3 go2 go4 go6 go9+gm3 go2 go4 go6 go8+gm3 go2 go4 go7 go8+gm3 go2 go4 go7 go9+gm4 gm1 go2 go6 go8+ gm4 gm1 go2 go7 go8+gm4 gm1 go2 go7 go9+gm4 gm1 go2 go7 gm8+ gm4 gm1 go2 go6 go9+gm4 gm1 go2 go6 gm8+ gm3 gm2 go4 go7 gm8+go1 go5 go2 go7 go9+go1 gm3 go4 go7 go9+go1 go5 go2 go7 gm8+go1 go2 go4 go7 go9+ go1 go2 go4 go6 go8+go1 gm2 go4 go7 go9+go1 gm3 go4 go6 gm8+go1 go2 go4 go7 go8+go1 go5 go4 go7 go8+ gm3 gm1 go4 go7 gm8+gm3 go2 go4 go7 gm8+ gm3 gm1 go4 go7 go9+gm3 gm1 go4 go6 go9+gm3 gm1 go4 go6 go8+ gm3 gm1 go4 go7 go8+go3 gm2 go4 go7 gm8+go3 go2 go4 go6 go9+go3 go2 go4 go6 go8+go3 go2 go4 go7 go8+ go3 go5 go4 go7 gm8+gm3 go5 go4 go6 go9+gm3 go5 go4 go6 go8+gm3 go5 go4 go7 go8+gm3 go5 go4 go7 go9+ gm3 go2 go4 go6 gm8+ go1 go5 go4 go6 go8+go1 go3 go4 go6 go9+go1 go3 go4 go6 go8+go1 go3 go4 go7 go8+ go1 go3 go4 go7 go9+go1 go5 go4 go7 go9

It can be clearly infered that the size of the expressions for the next moments by applying (6) may grow exponentially, and when the Padé approximation is done by generating (7), much more memory will be needed. Fortunately, in (Fakhfakh et al., 2010) there is a simplification approach for analog integrated circuits designed with MOSFETs, so that the behavioral model for the uncompensated low voltage amplifier can be reduced to a third order described by:

$$H(s) = \frac{-g_{m1}g_{m6}g_{m8}}{C_L C_{p1} C_{p2} s^3 + C_{p1} C_{p2} s^2 + (c_{p1}(g_{o6} + g_{o7}) + C_{p2}(g_{o2} + g_{o4}))g_{m8} s + g_{m8}(g_{o2} + g_{o4})(g_{o6} + g_{o7})} \quad (8)$$

From this example, it can be appreciated that a combination of symbolic and numerical model order reduction approaches can be very useful to generate simplified behavioral models of analog integrated circuits.

5. Behavioral modeling of sinusoidal oscillators

This section provides an overview of the usefulness of generating symbolic behavioral models in the design of sinusoidal oscillators implemented with mixed-mode devices, such as the operational transresistance amplifier (OTRA). This device can also be designed with standard CMOS integrated circuit technology, so that an accurate simplified symbolic behavioral model can be difficult to generate. The following section approaches the behavior of the OTRA with a simple transfer function. This analytical expression can be used in a higher abstraction level, e.g. into Verilog-A as already shown in (Tlelo-Cuautle, Duarte-Villaseñor, Garcia-Ortega & Sánchez-López, 2007; Tlelo-Cuautle, Sánchez-López, Fakhfakh & Loulou, 2007), to accelerate design development time.

The OTRA is an important building block in mixed-mode analog integrated circuit design. One reason is that circuit designers have been focusing their attention on analog signal processing applications extended to high-frequency by using current-mode techniques (Hwang et al., 2009). Although the OTRA is commercially available in bipolar technology,

it does not provide a virtual ground at the input terminals and only allows the input current to flow in one direction [1].

Recent realizations have been suggested to design OTRA based circuits in multiple-mode (Lee, 2010), e.g. voltage, current, transconductance, and transresistance modes. Among the applications of OTRAs one can find implementations such as: instrumentation amplifiers, integrators, continuous-time filters, immitance simulators, waveform generators, bistable multivibrators, oscillators and amplification of signals from current-source transducers. These applications using OTRAs overcome the finite gain-bandwidth product associated to conventional opamps. Additionally, both the inputs and outputs of the OTRA are low impedance terminals, that way, all parasitic capacitors will have little effect and the time response limitations incurred by parasitic capacitors can be minimized (Chen et al., 2001). On the other hand, since the OTRA is a high gain current-input voltage-output device, it can be considered as a current-to-voltage converter and its behavior can be modeled by using a current-controlled voltage source (CCVS). This CCVS can be modeled using nullors, so that once again, as already shown in the previous section, we are able to apply the symbolic NA method to generate symbolic behavioral models of OTRA based circuits.

In this section, a new nullor-based model for the OTRA, which is composed by four nullors and three grounded resistors is introduced. In this manner, the symbolic NA method can easily be applied to compute small-signals characteristics of OTRAs-based analog circuits. The nullor-based model not only reduces the admittance matrix size, if it is compared with the element stamp method, but also analog circuits with both inputs currents flowing toward the OTRA can easily be analyzed.

The OTRA is a three-terminal analog building block, where its input-output terminals are characterized by low impedances, and its behavior can be described as already shown in (Hwang et al., 2009). Since external negative feedback is required for OTRA based analog circuits, it is better to design an OTRA with high DC open-loop gain.

To show the usefulness of the nullor equivalent of the OTRA, lets us consider the OTRAs-based oscillator shown in Fig. 7. The system of equation by applying the symbolic NA method is given by (9). The evaluation of the determinant of the admittance matrix generates the characteristic equation given by (10).

$$\begin{bmatrix} -sC_1 & 0 & 1 & 0 \\ \frac{1}{R_{m1}} & -\frac{1}{R_1} & 1 & 0 \\ -\frac{1}{R_2} & -sC_2 - \frac{1}{R_s} & 0 & 1 \\ 0 & \frac{1}{R_{m2}} - \frac{1}{R_4} & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{3,9} \\ v_{6,13} \\ v_{7,8} \\ v_{11,12} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{9}$$

$$s^2 + \left(\frac{1}{R_{m1}C_1} + \frac{1}{R_{m2}C_2} + \frac{1}{C_2}\left(\frac{1}{R_s} - \frac{1}{R_4}\right)\right)s + \frac{1}{R_1R_2C_1C_2} + \frac{1}{R_{m1}C_1C_2}\left(\frac{1}{R_{m2}} + \frac{1}{R_s} - \frac{1}{R_4}\right) \tag{10}$$

Since the gain of the OTRA is finite the two-pole behavioral model can be described by (11). Where ω_{p1} and ω_{p2} are the angular frequencies of the first and second pole and R_{m0} is the DC gain of the OTRA.

[1] National Semiconductors Corp., Designing with a new super fast dual norton amplifier. Linear Applications Data Book, 1981.
National Semiconductors Corp., The LM 3900: a new current differencing quad of the input amplifiers. Linear Applications Data Book, 1986.

$$R_m(s) = \frac{R_{m0}}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} \tag{11}$$

For middle frequency applications, the transfer of the OTRA denoted by $R_m(s)$ can be expressed by (12). Therefore, since $|s = j\omega| << \omega_{p2}$ (10) is approached by (13).

$$R_m(s) = \frac{1}{sC_m(1+\frac{s}{\omega_{p2}})}; \quad C_m = \frac{1}{R_{m0}\omega_{p1}} \tag{12}$$

$$s^2 + \frac{1}{C_2+C_{m2}}(\frac{1}{R_s} - \frac{1}{R_4})s + \frac{1}{R_1R_2(C_1+C_{m1})(C_2+C_{m2})} \tag{13}$$

That way, the condition and frequency of oscillation are given by (14).

$$R_3 = R_4, \quad \omega_o = \frac{1}{\sqrt{R_1R_2(C_1+C_{m1})(C_2+C_{m2})}} \tag{14}$$

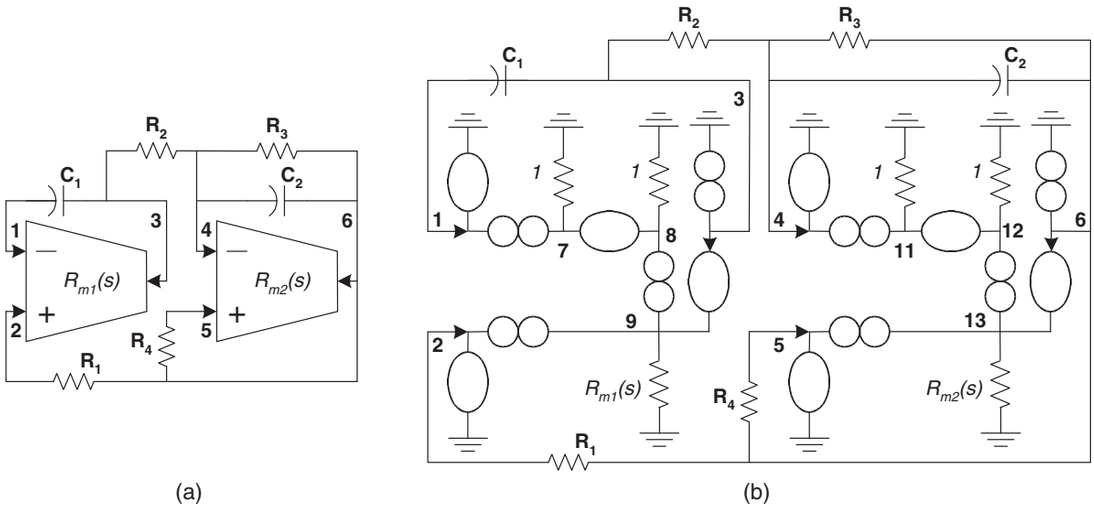


Fig. 7. (a) OTRAs-based oscillator taken from (Salama & Soliman, 2000), and (b) nullor equivalent.

The oscillator in Fig. 7 was designed and simulated using HSPICE to verify its behavior at several frequencies. By choosing R_1=R_2=2kΩ, R_3=R_4=10kΩ, the value of the frequencies of oscillation are shown in Fig. 8 as:

f_1=2.65MHz (Dashed-line) with C_1=C_2=24pF,
f_2=6.29MHz with C_1=C_2=6.46pF (Dotted-line), and
f_3=12MHz (Solid line) with C_1=C_2=0.1pF,

The parasitic capacitances were calculated by applying (12) so that they were approximated to C_{m1}=C_{m2}=6.46pF. On the other hand, the calculation of the frequencies of oscillation for very high frequency applications, needs to be performed by applying the approximation given in (15). In this manner, we obtain f_1=2.61MHz, f_2=6.16MHz and f_3=12.1MHz which are in good agreement with the simulated results.

$$R_m(s) = \frac{\omega_{p2}}{s^2 C_m} \tag{15}$$

From Fig. 8 one can observe that the maximum frequency of oscillation (f_3=12MHz) is limited by $C_{m1,2}$=C_{Z2} according to (12), with R_{m0}=R_{Z2}, where R_{Z2} and C_{Z2} are the parasitic resistance and capacitance associated to the Z terminal of the commercially available AD844AN.

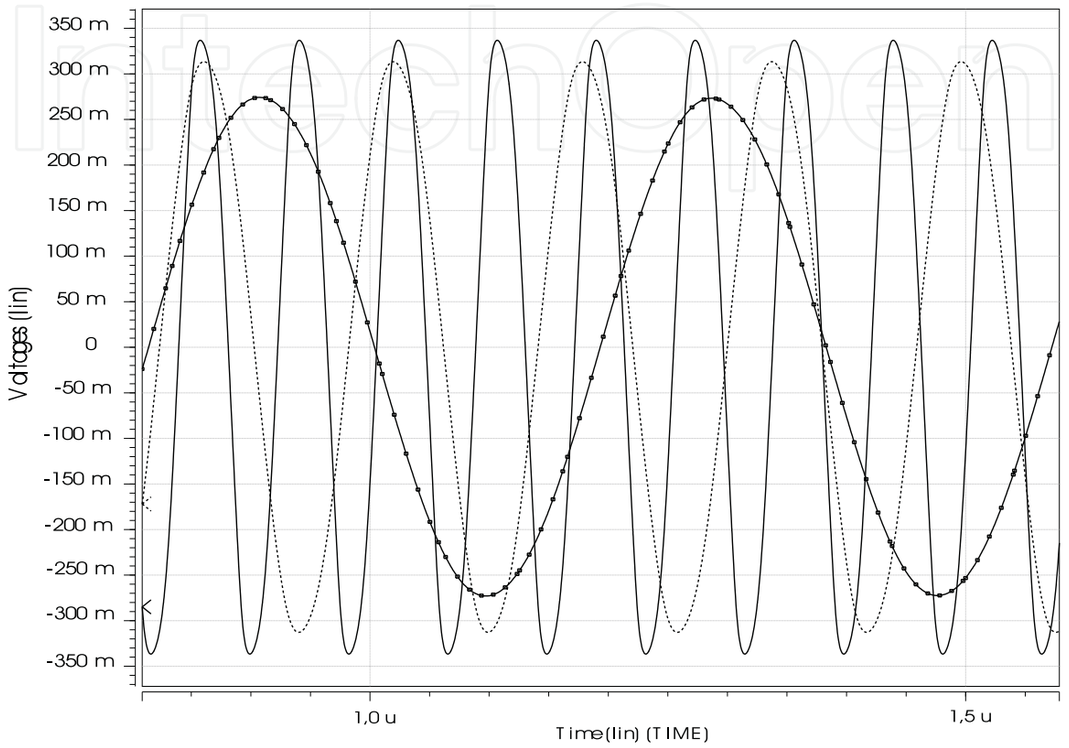


Fig. 8. Time responses of the OTRA-based sinusoidal oscillator

6. Noise and distortion behavioral modeling

Symbolic analysis has been demonstrated its usefulness in computing second order effects such as noise and distortion, some works can be found in (Fakhfakh et al., 2010). For the noise behavioral modeling approach, the nature of the equations in noise analysis allows applying determinant decision diagrams (DDD)s (Shi & Tan, 2000), to improve the calculation of noise expressions (Martinez-Romero et al., 2010).

The generation of behavioral expressions for noise figure, input and output noise for analog circuits is presented in (Tlelo-Cuautle & Sánchez-López, 2004). In this section we show the results of the calculation of the output noise for the three stages uncompensated low voltage amplifier shown in Fig. 3. As already shown in (Martinez-Romero et al., 2010), the behavioral noise expression is compared with Hspice simulations using the level zero Spice 2 models.

The equivalent circuit for noise analysis of the three stages amplifier is shown in Fig. 9. The details on the formulation of the system of equations is provided in (Martinez-Romero et al., 2010). It generates an admittance matrix of order 5×5, which can be easily solved by applying DDDs. The symbolic behavioral expression of the output noise is also given in (Martinez-Romero et al., 2010), while the comparison between HSPICE and the evaluation

of the symbolic expression is given in Fig. 10. The error can be minimized by addition of other noisy elements but the symbolic expression can increase. Other examples related to symbolic noise behavioral modeling are provided in (Fakhfakh et al., 2010).

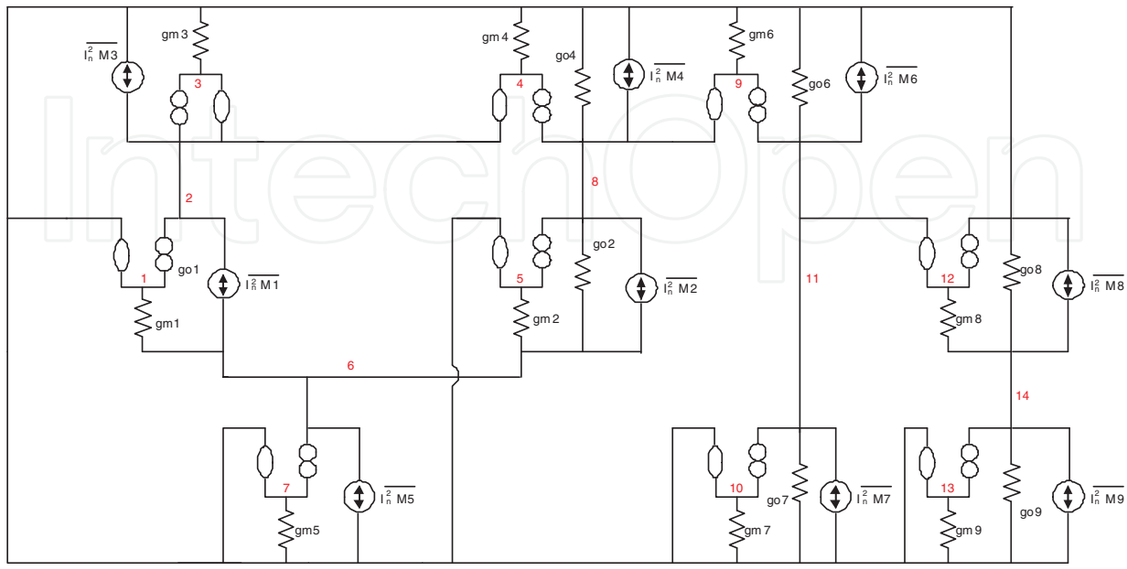


Fig. 9. Nullor equivalent from Fig. 3.

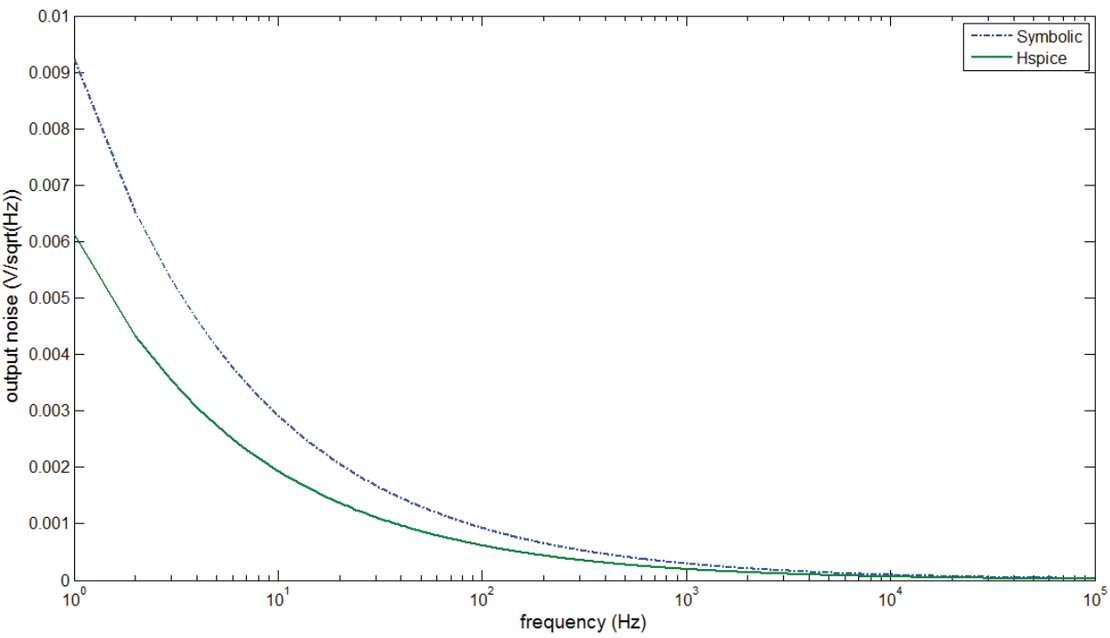


Fig. 10. Symbolic and HSPICE noise responses for the uncompensated amplifier.

For the symbolic distortion behavioral modeling, an analysis approach is presented by (Floberg, 1997), it deals with bipolar transistor circuits. However, due to the difficulty to generate analytical expressions in circuits with hard-distortion and at high-frequencies

(Wambacq et al., 1999), the distortion analysis is generally performed for weakly nonlinear circuits (Li & Pileggi, 2005). In this case, the application of symbolic analysis for behavioral model generation is suitable for the distortion analysis in single-, two- and three-stage amplifiers (Hernes & Sansen, 2005).

Combinations of symbolic methods with numerical analysis for nonlinear circuits are presented in (Daems et al., 2002; Manthe et al., 2003). Besides, recent developments are oriented to nonlinear Model Order Reduction of Analog/RF Circuits.

For instance, abstracting transistor-level circuit details that include important weakly nonlinear effects into a compact macromodel can be instrumental in assisting the analysis and design of analog and RF circuits. For many such applications, while circuit blocks often exhibit weak nonlinearities, the design specification for linearity is often extremely important and very stringent. Hence, it is important to be able to model distortions in a compact and accurate way.

Along this line, a number of research attempts have emerged in the literature. Symbolic modeling of weakly nonlinear circuits has been used to build system-level models (Wambacq et al., 2000; Wambacq & Sansen, 1998), by using the notation of Volterra series. Neural network and time series models have also been proposed for nonlinear modeling (Root et al., 2003). Nonlinear reduction techniques have been studied, which may target only strongly nonlinear behaviors, or may include both weakly and nonlinear aspects (Dong & Roychowdhury, 2003; Rewienski & White, 2001).

For many applications where weakly nonlinear distortions are important aspects of design specifications, Volterra series provides a good choice for system description. In (Phillips, 2000; Roychowdhury, 1999), the projection-based nonlinear model order-reduction frameworks for weakly nonlinear systems were first developed by extending moment-matching projection techniques used for interconnect modeling. Here the basic idea is to view a weakly nonlinear system as a set of interconnected linear networks and then each of such linear circuits is reduced via model order reduction.

While the concept of projection-based model order reduction is highly relevant for nonlinear distortion modeling, it is worthy noting that the reduced model compactness is critical for effective nonlinear model reduction. Without proper handling, resulting size of a projection-based nonlinear reduced model tends to grow rapidly.

To this end, the most general matrix-form nonlinear transfer functions, or in other words, frequency-domain Volterra kernels, are used as a starting point for nonlinear model order reduction (Li & Pileggi, 2003; 2005). In this so-called NORM algorithm, to disclose the problem structure of nonlinear model order reduction, moments of nonlinear transfer functions and associated Krylov subspaces have been derived in the matrix form. With this, relationships between Krylov subspace projection and nonlinear transfer function moment matching are understood. Using this as a basis, the model size is further optimized for a targeted number of matched moments, leading to significant improvements on the model compactness. The reduced order model structure can be tailored by controlling the moment matching orders for different orders of nonlinearity in a coherent fashion. Furthermore, it is shown that multipoint expansions for projection-based nonlinear model order reduction is advantageous in terms of model compactness at the expanse of additional computational cost (Li & Pileggi, 2003; 2005). Under the same based framework, weakly nonlinear distortions of time-varying RF circuits can be also captured.

7. Conclusion

We have presented the symbolic behavioral model generation of mixed-mode circuits. It was shown that the use of the nullor properties allows us not only to describe the dominant behavior of active devices, but also to add or remove parasitic elements in order to generate simplified analytical expressions. Furthermore, the nullor equivalent of a mixed-mode circuit is suitable to formulate a compact system of equations by applying nodal analysis.
Several examples were presented to demonstrate the usefulness of the nullor models to generate symbolic behavioral expressions of mixed-mode circuits and of sinusoidal oscillators.
A new nullor-based model for the mixed-mode device named operational transresistance amplifier (OTRA) was introduced and it was used to compute small-signal characteristics of a sinusoidal oscillator oriented to circuit design.
Some open research problems in the generation of symbolic behavioral models were listed along the chapter. That problems may be solved by using the properties of the nullor and nodal analysis, and by applying model order reduction (MOR) techniques. Finally, to generate a simplified behavioral model, it could be much better to combine numerical and symbolic approaches and to develop new MOR approaches to deal with analog VLSI circuits.

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9. References

Alvarado, J., Iniguez, B., Estrada, M., Flandre, D. & Cerdeira, A. (2010). Implementation of the symmetric doped double-gate MOSFET model in Verilog-A for circuit simulation, *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields* 23(2): 88–106.

and A. Bentrcia and S.M. Al-Shahrani, M. A. (2004). A novel mixed-mode current-conveyor-based filter, *International Journal of Electronics* 91(3): 191–197.

Ansari, M. & Maheshwari, S. (2009). Electronically tunable MOSFET-C mixed-mode quadrature oscillator, *International Multimedia, Signal Processing and Communication Technologies*, pp. 158–160.

Balik, F. (2009). A semi - symbolic method of electronic circuit design by pole and zero distribution optimization using time - constants approximation, *IEEE International Conference on Electronics, Circuits and Systems*, pp. 848–851.

Beelen, T., ter Maten, E., Sihaloho, H. & van Eijndhoven, S. (2010). Behavioral modeling of the dominant dynamics in input-output transfer of linear(ized) circuits, *Procedia Computer Science* 1(1): 347–355.

Bhadri, P., Srinivasan, R., Mal, P., Beyette, F. & Carter, H. (2005). Mixed mode integrated circuits, *IEEE Potentials* 24(1): 6–11.

Biolek, D., Senani, R., Biolkova, V. & Kolka, Z. (2008). Active elements for analog signal processing: Classification, review, and new proposals, *Radioengineering* 17(4): 15–32.

Chek, D., Tan, M., Ahmadi, M., Ismail, R. & Arora, V. (2010). Analytical modeling of high performance single-walled carbon nanotube field-effect-transistor, *Microelectronics Journal* 41(9): 579–584.

Chen, H. (2010). Single CCII-based voltage-mode universal filter, *Analog Integrated Circuits and Signal Processing* 62(2): 1573–1979.

Chen, J., Tsao, H. & Liu, S. (2001). Voltage-mode MOSFET-C filters using operational transresistance amplifier (OTRA's) with reduced parasitic capacitance effect, *IEE Proc. Circuits Devices Syst.* 148(5): 242–249.

Daems, W., Gielen, G. & Sansen, W. (2002). A fitting approach to generate symbolic expressions for linear and nonlinear analog circuit performance characteristics, *Design, Automation and Test in Europe*, pp. 268–273.

Daems, W., Verhaegen, W., Wambacq, P., Gielen, G. & Sansen, W. (1999). Evaluation of error control strategies for the linear symbolic analysis of analog integrated circuits, *IEEE Trans. Circuits and Systems I* 46(5): 594–606.

Diaz-Madrid, J., Hinojosa, J. & Doménech-Asensi, G. (2008). Fuzzy logic technique for accurate analog circuits macromodel sizing, *International Journal of Circuit Theory and Applications* 38(3): 307–319.

Dong, N. & Roychowdhury, J. (2003). Piecewise polynomial nonlinear model reduction, *Proc. ACM/IEEE Design Automation Conf.*, pp. 484–489.

Fakhfakh, M., Tlelo-Cuautle, E. & Fernández, F. (2010). *Design of Analog Circuits through Symbolic Analysis*, Bentham Sciences Publishers Ltd.

Fernández, F., Guerra, O., Rodriguez-Garcia, J. & Rodriguez-Vázquez, A. (1998). Symbolic analysis of analog integrated circuits: the numerical reference generation problem, *IEEE Trans. on Circuits and Systems - II* 45(10): 1351–1361.

Floberg, H. (1997). *Symbolic analysis in analog integrated circuit design*, Kluwer Academic Publishers.

Gaoua, S., S.ăAsadi, M.C.E.ăYagoub & F.A.ăMohammadi (2010). CAD tools for efficient RF/microwave transistor modeling and circuit design, *Analog Integrated Circuits and Signal Processing* 63(1): 59–70.

Guerra, O., Rodriguez-Garcia, J., Fernández, F. & Rodriguez-Vázquez, A. (2002). A symbolic pole/zero extraction methodology based on analysis of circuit time-constants, *Analog Integrated Circuits and Signal Processing* 31: 101–118.

Guerra, O., Rodriguez-Garcia, J., Roca, E., Fernández, F. & Rodriguez-Vázquez, A. (1998). A simplification before and during generation methodology for symbolic large-circuit analysis, *IEEE Int. Conf. on Electronics, Circuits and Systems*, pp. 81–84.

Haley, S. (1991). Modification-decomposition transformation in analog design, *Int. Journal of Computer Aided VLSI Design* pp. 427–428.

Hao, Z. & Shi, G. (2009). Symbolic techniques for statistical timing analysis of rcl mesh networks with resistor loops, *IEEE International Symposium on Integrated Circuits*, pp. 470–473.

Henning, E. (2002). Matrix approximation techniques for symbolic extraction of poles and zeros, *Analog Integrated Circuits and Signal Processing* 31: 81–100.

Hernes, L. & Sansen, W. (2005). Distortion in single-, two- and three-stage amplifiers, *IEEE Trans. on Circuits and Systems I* 52(5): 846–856.

Hsu, J. & Sechen, C. (1994). DC small signal symbolic analysis of large analog integrated circuits, *IEEE Trans. on Circuits and Systems, Part I* 41(12): 817–828.

Hwang, Y., Wu, D., Chen, J., Shih, C. & Chou, W. (2009). Design of current-mode MOSFET-C filters using OTRAs, *International Journal of Circuit Theory and Applications* 37(3): 397–411.

Krishna, S., Baghini, M. & Mukherjee, J. (2007). Behavioral models of basic mixed-mode circuits: practical issues and application, *Proceedings of European conference on circuit theory and design*, Spain, pp. 854–857.

Lee, C. (2010). Multiple-mode OTA-C universal biquad filters, *Circuits, Systems and Signal Processing* 29(2): 263–274.

Li, P. & Pileggi, L. (2003). NORM: compact model order reduction of weakly nonlinear systems, *Proc. of 40th IEEE/ACM Design Automation Conference*, pp. 472–477.

Li, P. & Pileggi, L. (2005). Compact reduced-order modeling of weakly nonlinear analog and RF circuits, *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems* 23(2): 184–203.

Li, X., McAndrew, C., Wu, W., Chaudhry, S., Victory, J. & Gildenblat, G. (2010). Statistical modeling with the PSP MOSFET model, *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems* 29(4): 599–606.

Lihong, Z., Jangkrajarng, N., Bhattacharya, S. & Shi, C. (2008). Parasitic-aware optimization and retargeting of analog layouts: A symbolic-template approach, *IEEE Tran. on Computer-Aided Design of Integrated Circuits and Systems* 27(5): 791–802.

Maheshwari, S., Mohan, J. & Chauhan, D. (2010). Voltage-mode cascadable all-pass sections with two grounded passive components and one active element, *IET Circuits, Devices & Systems* 4(2): 113–122.

Manthe, A., Zhao, L. & Shi, R. (2003). Symbolic analysis of analog circuits with hard nonlinearity, *IEEE/ACM Design Automation Conference*, pp. 542–545.

Martinez-Romero, E., Tlelo-Cuautle, E., Sánchez-López, C. & X.-D. Tan, S. (2010). Symbolic noise analysis of low voltage amplifiers by using nullors, *SM2ACD*, IEEE, Tunisia.

McAndrew, C. (2010). Integrated resistor modeling, *in* G. Gildenblat (ed.), *Compact Modeling: Principles, techniques and applications*, Springer, Netherlands, pp. 271–297.

McConaghy, T. & Gielen, G. (2009). Template-free symbolic performance modeling of analog circuits via canonical-form functions and genetic programming, *IEEE Tran. on Computer-Aided Design of Integrated Circuits and Systems* 28(8): 1162–1175.

Muñoz-Pacheco, J. & Tlelo-Cuautle, E. (2009). Automatic synthesis of 2D-n-scrolls chaotic systems by behavioral modeling, *Journal of Applied Research and Technology* 7(1): 5–14.

Phillips, J. (2000). Automated extraction of nonlinear circuit macromodels, *Proc. Custom Integr. Circuits Conf.*, pp. 451–454.

Pugliese, A., Amoroso, F., Cappuccino, G. & Cocorullo, G. (2010). Analysis of op-amp phase margin impact on SC sigma-delta modulator performance, *Microelectronics Journal* 41(7): 440–446.

Qin, Z., Tan, S. & Cheng, C. (2005). *Symbolic analysis and reduction of VLSI circuits*, Springer.

Rewienski, M. & White, J. (2001). A trajectory piecewise-linear approach to model order reduction and fast simulation of nonlinear circuits and micromachined devices, *Proc. IEEE/ACM Int. Conf. Computer-Aided Design*, pp. 252–257.

Rodriguez-Garcia, J., Guerra, O., Roca, E., Fernández, F. & Rodriguez-Vázquez, A. (1999). Error control in simplification before generation algorithms for symbolic analysis of large analogue circuits, *Electronic Letters* 35(4): 260–261.

Root, D., Wood, J. & Tufillaro, N. (2003). New techniques for nonlinear behavioral modeling of microwave/RF ICs from simulation and nonlinear microwave measurements, *Proc. ACM/IEEE Design Automation Conf.*, pp. 85–90.

Roychowdhury, J. (1999). Reduced-order modeling of time-varying systems, *IEEE Trans. on Circuits and Systems II* 46(10): 1273–1288.

Ruiz-Amaya, J., de la Rosa, J., Fernández, F., Medeiro, F., del Rio, R., Pérez-Verdú, B. & Rodriguez-Vázquez, A. (2005). High-level synthesis of switched-capacitor, switched-current and continuous-time SD modulators using SIMULINK-based time-domain behavioral models, *IEEE Trans. on Circuits and Systems, Part I* 52(9): 1795–1810.

S. Steinhorst & L. Hedrich (2010). Advanced methods for equivalence checking of analog circuits with strong nonlinearities, *Formal Methods in System Design* 36(2): 131–147.

Saad, R. & Soliman, A. (2008). Use of mirror elements in the active device synthesis by admittance matrix expansion, *IEEE Tran. on Circuits and Systems I* 55(9): 2726–2735.

Saad, R. & Soliman, A. (2010). A new approach for using the pathological mirror elements in the ideal representation of active devices, *International Journal of Circuit Theory and Applications* 38(2): 148–178.

Salama, K. & Soliman, A. (2000). Novel oscillators using the operational transresistance amplifier, *Microelectronics Journal* 31(1): 39–47.

Sánchez-López, C., Fernández, F. & Tlelo-Cuautle, E. (2010). Generalized admittance matrix models of OTRAs and COAs, *Microelectronics Journal* 41(8): 502–505.

Sánchez-López, C., Moro-Frias, D. & Tlelo-Cuautle, E. (2008). Improving the formulation process of the system of equations of analog circuits, *International Workshop on Symbolic and Numerical Methods, Modeling and Applications to Circuit Design*, Erfurt, Germany, pp. 102–106.

Sánchez-López, C. & Tlelo-Cuautle, E. (2009). Symbolic behavioral model generation of current-mode analog circuits, *International Symposium on Circuits and Systems (ISCAS)*, IEEE, Taiwan, pp. 2761–2764.

Sánchez-López, C., Trejo-Guerra, R., Muñoz-Pacheco, J. & Tlelo-Cuautle, E. (2010). N-scroll chaotic attractors from saturated functions employing CCII+s, *Nonlinear Dynamics* 61(1-2): 331–341.

Sanchez-Sinencio, E. (2009). Low voltage amplifier design techniques, *Tutorial in IEEE Midwest Symposium on Circuits and Systems*, Cancun, Mexico.

Shi, C. & Tan, S. (2000). Canonical symbolic analysis of large analog circuits with determinant decision diagrams, *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems* 19(1): 1–18.

Shi, G., Hu, B. & Shi, C. (2006). On symbolic model order reduction, *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems* 25(7): 1257–1272.

Shi, G. & Meng, X. (2009). Variational analog integrated circuit design via symbolic sensitivity analysis, *IEEE International Symposium on Circuits and Systems*, pp. 3002–3005.

Smith, K. & Sedra, A. (1968). *Proceedings of the IEEE* 56(The current conveyor: a new circuit building block): 1368–1369.

Soliman, A. (2007). Voltage mode and current mode tow thomas bi-quadratic filters using inverting CCII, *International Journal of Circuit Theory and Applications* 35(4): 463–467.

Soliman, A. (2009). Applications of voltage and current unity gain cells in nodal admittance matrix expansion, *IEEE Circuits and Systems Magazine* 9(4): 29–42.

Sommer, R., Halfmann, T. & Broz, J. (2008). Automated behavioral modeling and analytical model-order reduction by application of symbolic circuit analysis for multiphysical systems, *Simulation Modeling Practice and Theory* 16(8): 1024–1039.

Sommer, R., Henning, E., Droge, G. & Horneber, E. (1993). Equation-based symbolic approximation by matrix reduction with quantitative error prediction, *Alta Frequenza* 5(6): 317–325.

Suissa, A., Romain, O., Denoulet, J., Hachicha, K. & Garda, G. (2010). Empirical method based on neural networks for analog power modeling, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 29(5): 839–844.

Tan, S. & He, L. (2007). *Advanced Model Order Reduction Techniques in VLSI Design*, Cambridge University Press.

Tan, S. & Shi, C. (2004). Efficient approximation of symbolic expressions for analog behavioral modeling and analysis, *IEEE Tran. on Computer-Aided Design of Integrated Circuits and Systems* 23(6): 907–918.

Tlelo-Cuautle, E., Duarte-Villaseñor, M., Garcia-Ortega, J. & Sánchez-López, C. (2007). Designing SRCOs by combining SPICE and Verilog-A, *International Journal of Electronics* 94(4): 373–379.

Tlelo-Cuautle, E., Duarte-Villaseñor, M. & Guerra-Gómez, I. (2008). Automatic synthesis of VFs and VMs by applying genetic algorithms, *Circuits, Systems and Signal Processing* 27(3): 391–403.

Tlelo-Cuautle, E., Martinez-Romero, E., Sánchez-López, C. & X.-D. Tan, S. (2009). Symbolic formulation method for mixed-mode analog circuits using nullors, *International Conference on Electronics, Circuits, and Systems (ICECS)*, IEEE, Mexico, pp. 856–859.

Tlelo-Cuautle, E., Martinez-Romero, E., Sánchez-López, C. & X.-D. Tan, S. (2010). Symbolic behavioral modeling of low voltage amplifiers, *International Conf. on Electrical Engineering, Computing Science and Automatic Control (CCE)*, IEEE, Mexico, pp. 510–514.

Tlelo-Cuautle, E., Moro-Frias, D. & Duarte-Villaseñor, M. (2008). Synthesis of CCII-s by superimposing VFs and CFs through genetic operations, *IEICE Electron. Express* 5(11): 411–417.

Tlelo-Cuautle, E. & Sánchez-López, C. (2004). Symbolic computation of NF of transistor circuits, *IEICE Trans on Fundamentals of Electronics, Communications and Computer Sciences* E87(9): 2420–2425.

Tlelo-Cuautle, E., Sánchez-López, C., Fakhfakh, M. & Loulou, M. (2007). Designing SRCOs by symbolic-behavioral-modeling of unity-gain cells, *IEEE International Conference on Electronics, Circuits and Systems*, Marrakech, pp. 1035–1038.

Tlelo-Cuautle, E., Sánchez-López, C., Martinez-Romero, E. & Tan, S. (2010). Symbolic analysis of analog circuits containing voltage mirrors and current mirrors, *Analog Integrated Circuits and Signal Processing* 65(1): 89–95.

Tlelo-Cuautle, E., Sánchez-López, C. & Moro-Frias, D. (2010). Symbolic analysis of (MO)(I)CCI(II)(III)-based analog circuits, *International Journal of Circuit Theory and Applications* 38(6): 649–659.

Trejo-Guerra, R., Sánchez-López, C., Tlelo-Cuautle, E., Cruz-Hernández, C. & Muñoz-Pacheco, J. (2010). Realization of multiscroll chaotic attractors by using current-feedback operational amplifiers, *Revista Mexicana de Fisica* .

van der Horst, M., Linnenbank, A., Serdijn, W. & Long, J. (2010). Systematic design of a transimpedance amplifier with specified electromagnetic out-of-band interference behavior, *IEEE Trans.on Circuits and SystemsŮI* 57(3): 530–538.

Vasilevski, M., Aboushady, H. & Louerat, M. (2009). Automatic model refinement of Gm-C integrators for high-level simulation of continuous-time sigma-delta modulators, *International Symposium on Circuits and Systems*, IEEE, pp. 2769–2772.

Wambacq, P., Dobrovolny, P., Donnay, S., Engels, M. & Bolsens, I. (2000). Compact modeling of nonlinear distortion in analog communication circuits, *Proc. ACM/IEEE Design, Automation Test Eur. Conf.*, pp. 350–354.

Wambacq, P., Dobrovolny, P., Gielen, G. & Sansen, W. (1998). Symbolic analysis of large analog circuits using a sensitivity-driven enumeration of common spanning trees, *IEEE Trans. Circuits and Systems - II* 45(10): 1342–1350.

Wambacq, P., Fernández, F., Gielen, G., Sansen, W. & Rodriguez-Vázquez, A. (1995). Efficient symbolic computation of approximated small-signal characteristics of analog integrated circuits, *IEEE J. Solid-State Circuits* 30(3): 327–330.

Wambacq, P., Fernández, F., Gielen, G., Sansen, W. & Rodriguez-Vázquez, A. (1996). A family of matroid intersection algorithms for the computation of approximated symbolic network functions, *IEEE International Symposium on Circuits and Systems*, pp. 806–809.

Wambacq, P., Gielen, G., Kinget, P. & Sansen, W. (1999). High-frequency distortion analysis of analog integrated circuits, *IEEE Trans. on Circuits and Systems II* 46(3): 335–345.

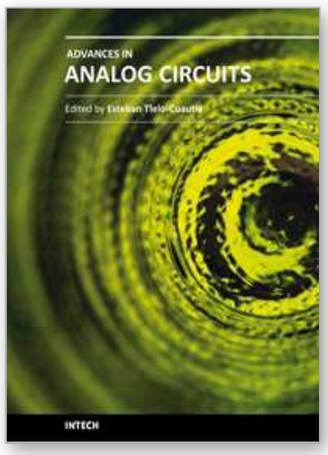
Wambacq, P. & Sansen, W. (1998). *Distortion Analysis of Analog Integrated Circuits*, Norwell, MA: Kluwer.

Yu, Q. & Sechen, C. (1995). Efficient approximation of symbolic network functions using matroid intersection algorithms, *IEEE International Symposium on Circuits and Systems*, pp. 2088–2091.

Yu, Q. & Sechen, C. (1996). A unified approach to the approximate symbolic analysis of large analog integrated circuits, *IEEE Trans. on Circuits and Systems I* 43(8): 656–669.

Yu, Q. & Sechen, C. (1997). Efficient approximation of symbolic network functions using matroid intersection algorithms, *IEEE Trans. on Computer Aided Design* 16: 1073–1081.

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