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Analog CMOS Design Automation Methodologies for Low-Power Applications

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1. Introduction

The design automation of analog CMOS integrated circuits (ICs) is a demanding task in microelectronics industry, because of the crescent necessity for low-power design and reduced time-to-market. Nowadays, most analog sizing designs are done manually - with some aid of simulation tools and equation-based models - and the quality of the resulting circuit is dependent on the expertise of the designer. A system-on-chip (SOC) design has analog and digital parts, each one designed with different methodologies and tools. The analog design time must be compatible with the highly automated digital design time, which employs advanced design automation tools (Gielen & Rutenbar, 2000).

The automation of fundamental analog design steps is extremely relevant for the success of a project. The transistor sizing stage is, perhaps, the most difficult to automate due to the large and highly non-linear design space. This stage is time consuming and might induce significant delays relating to time-to-marketing. Nowadays, there is no analog circuit sizing tools fully automatic searching the entire design space and taking advantage of state-of-the-art fabrication technologies. Also, layout generation of analog blocks is error-prone and time demanding.

An analog integrated circuit design is composed by transistors with different gate widths and lengths, requiring complex techniques of layout generation to minimize variations and improve matching. A traditional analog design methodology includes poor automated calculations with electrical models based on first order equations, several iterations of spice simulations and analysis, and full-custom layout generation. The experience of the designer is fundamental for the quality of the resulting design and for the amount of time spent.

In general, the entire design space is rarely explored, mainly in transistor weak and moderate inversion regions, which are the most appropriated for power-constrained applications. The design space for the automatic synthesis of analog CMOS integrated circuits is highly nonlinear. There are tens of free variables in the design of a typical analog integrated block (such as an operational transconductance amplifier), related to gate dimensions (W and L), bias currents or inversion levels. As the relation between transistor sizes and circuit specifications (design objectives) is sometimes conflicting, the problem of finding an optimum solution point is difficult to be exactly solvable. Some works have been done in this theme describing the development of tools for analog design automation (ADA), using different meta-heuristics and algorithms (Liu et al., 2009) (Vytyaz et al., 2009). The goal is always the automation of time-consuming tasks and complex searches in highly non-linear design

spaces (Xu et al., 2009) (de Smedt & Gielen, 2003) (Hershenson et al., 2001). Basically all of them can be categorized as equation-based or simulation-based automatic designs. In the equation-based design strategy, analytical equations are used for modeling device electrical characteristics, such as drain current, inversion level or small-signal parameters. These models are often simplified or manipulated in order to fit certain limitations imposed by optimization heuristics. The simulation-based strategy is based on results of electrical simulations of the circuit to extract device parameters and design characteristics. The simulation can be automated and performed several times until reaching the design objective. Both strategies have demonstrated limitations but, together with powerful optimization meta-heuristics, they are very promising for finding near-optimum design solutions in an acceptable computational time. The goal of this text is to compare two different techniques for automatic sizing of analog integrated amplifiers. The first one exploits the analytical gm/I_D methodology, in which the transconductance (gm) to drain current (I_D) ratio of the transistors are free variables and gate width and length are defined in terms of the technology independent gm/I_D versus $I_D/(W/L)$ curve; and the second one is numeric, based on an automated sequence of simulations of a spice netlist with W and L as free variables. We employed Genetic Algorithms (GA) as optimization heuristics. Both methodologies were implemented for sizing a power-constrained design of a two-stage Miller operational transconductance amplifier for three different gain-bandwidth requirements.

2. Operational amplifier sizing optimization

The design of analog integrated circuits requires extensive design practice with a given technology to correctly size transistors in order to achieve the required performance. Analytical knowledge-based equations describe the relations between the transistors (design parameters), design specifications (e.g. slew-rate grater or equal $10V/\mu s$) and design objectives (such as minimum power, area, noise, etc, or a combination thereof). These equations are topology-specific and can be used within an automatic synthesis methodology, which must perform the resolution of a system of non-linear equations. This system usually has more independent variables than equations, returning a wide solution space. As a design example using the two design methodologies here described, we used a two-stage CMOS Miller operational transconductance amplifier (OTA). The circuit schematic of this amplifier is shown in fig. 1. The Miller OTA is composed by an input differential pair and a current mirror with active load in the first stage. The second stage is composed by an inverter amplifier. Between the first and second stages is connected a compensation capacitor for stability purposes. Chosen the analog IC cell topology, the initial task of the optimization is to define search variables, specifications, and constraints in an appropriate manner. The free variables can be the channel lengths and widths of MOS transistors, transistor inversion levels, bias currents, capacitor values, etc.

As design specifications, we can include slew rate (SR), low frequency voltage gain (A_{V0}), gain bandwidth product (GBW), phase margin (PM), input common mode range ($ICMR$), power dissipation and silicon area (Allen & Holberg, 2002). The slew rate (SR) is calculated using the following equation:

$$SR = \frac{I_7}{C_f} \tag{1}$$

Here, I_7 is the drain current of $T7$ and C_f is the compensation capacitance. The low-frequency voltage gain of this amplifier is the product of first gain stage and the second gain stage and is given by

$$A_{v0} = \frac{gm_1}{gds_2 + gds_4} \cdot \frac{gm_5}{gds_5 + gds_6} \tag{2}$$

where gm is the gate transconductance and gds is the output conductance of MOSFETs transistors. The Gain Bandwidth Product (GBW) is calculated using the transconductance gm_1 and the capacitance C_f:

$$GBW = \frac{gm_1}{C_f} \tag{3}$$

The minimum and maximum values for the input common-mode range ($ICMR$) are evaluated using the large signal model, given by eq. 4 and 5, respectively.

$$ICMR^+ = V_{DD} - \sqrt{\frac{I_7}{\beta_2}} - |V_{T2}| - V_{DS7(sat)} \tag{4}$$

$$ICMR^- = V_{SS} + \sqrt{\frac{I_7}{\beta_4}} + V_{T4} - V_{T2} \tag{5}$$

Here, V_T is the threshold voltage, V_{DS} is the voltage between the drain and source terminals and β is a factor which depends on transistor size, carrier mobility (μ_0), gate oxide thickness (T_{ox}) and silicon oxide permittivity (ϵ_{ox}), given by

$$\beta = \mu_0 \cdot \frac{\epsilon_{ox}}{T_{ox}} \cdot \frac{W}{L} \tag{6}$$

The circuit power dissipation is given by the product between the supply voltage and total current consumption.

$$P_{diss} = (V_{DD} - V_{SS}) \cdot I_{DD} \tag{7}$$

The area occupied by the circuit is also an important specification. It cannot be exactly calculated in the design sizing stage because it depends on the layout strategy to be used in the physical synthesis design stage. However, an approximation considering gate area as the main parameter can give a good indication of the circuit total area.

$$A_{gate} = \sum_{i=1}^{k} W_i \cdot L_i + A_{C_f} \tag{8}$$

Here, k is the number of transistors in the circuit. We also include the area occupied by the compensation capacitor (A_{C_f}), which is proportional to its capacitance value (in general, it is implemented with double poly in CMOS technology).
The optimization strategy relies on minimizing a cost function, given as

$$f_c = \sum_{i=1}^{n} \alpha_i \hat{p}_i(X) + \sum_{j=1}^{m} \beta_j \hat{c}_j(X) \tag{9}$$

where α_i is the weighting coefficient for performance parameter $\hat{p}_i(X)$, which is a normalized function of the vector of independent design parameters X (free variables). This function

allows the designer to set the relative importance of competing performance parameters, such as, for example, a weighted relation between power and area. The parameter $\hat{c}_j(X)$ is a constraint normalized function, which limits the design space to feasible solutions of design specifications. The coefficient β_j indicates how closely the specification must be pursued. The constraint function, for specification of a minimum, has the following form:

$$\hat{c}_j(X) = \begin{cases} \frac{c_{j_{ref}}}{c_j(X)} & \text{if } c_{j_{ref}} > a \cdot c_{j_{ref}} \quad \text{or} \quad c_{j_{ref}} < c_j(X), \\ 0 & \text{if } c_{j_{ref}} \leq c_j(X) \leq a \cdot c_{j_{ref}}. \end{cases} \tag{10}$$

So, once the constraint value is achieved, it does not contribute for the increasing of the cost function value. The constant a means a percentage of the constraint overvalue that is considered accepted and it is necessary for avoiding an overestimation of a determined parameter during the optimal point search procedure. For a specification of a maximum, the constraint function has the inverse form. If $c_j(X)$ is inside a given specification, $\hat{c}_j(X)$ is set to zero. The cost function is computed in every iteration in the optimization loop. The correct design space exploration is directly related to the cost function formulation (Koza et al., 1997)(Alpaydin et al., 2003).

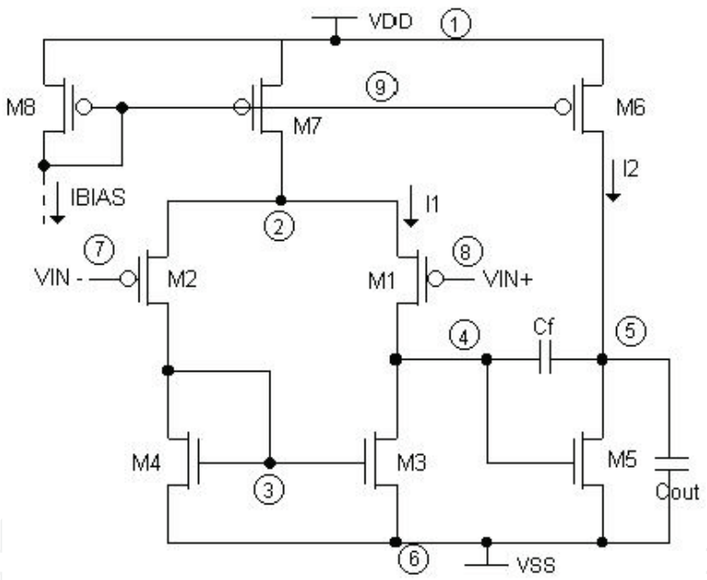


Fig. 1. Schematics of a two-stage Miller OTA.

The genetic algorithm, used in this work, is a heuristic for non-linear optimization based on the analogy with biologic evolution theories (Venkataraman, 2001). It is a non-deterministic algorithm and it works with a variety of solutions (population), simultaneously. The population is a set of possible solutions for the problem. The size of the population is defined in order to maintain an acceptable diversity considering an efficient optimization time. Each possible solution of population is denominated a chromosome, which is a chain of characters (gens) that represent the circuit variables. This representation can be in binary number, float or others. The quality of the solution is defined by an evaluation function (cost function). The algorithm receives an initial population, created randomly, some recombination and mutation operators and the MOSFET technology model parameters. The population is evaluated using a conventional SPICE electrical simulator. Based on valuation and roulette

method the parent chromosomes are selected for generating new chromosomes. The new chromosomes are created including recombination and mutation - analogy with biology. In the recombination, the chromosomes of two parents are divided and the union of the parts produces a recombination. By the other side, mutation is a random error that happens in a chromosome. The probability of mutation is defined by the user and it is compared with a random value. If this random value is smaller than the probability value then a gene on chromosome is randomly changed. In the case of analog design, it means that a random variation is created over a certain design parameter. The next step is the exclusion of parents and evaluation of new chromosomes, using again the electrical simulator and a cost function. Based on these values, new chromosomes are introduced in the population. At the end of each iteration, the stopping condition is tested and, if true, then the optimization is finished. Otherwise, new parents are selected and the process is repeated. The stopping condition can be the number of generations (iterations), minimal variation between variables or cost function, or others. In GA, the number of individuals in the population is very relevant, because it deals with several solutions simultaneously. Larger population increases the diversity of solutions but also increases the optimization time. Then, the number of population individuals must be chosen according to criteria of assuring solution diversity but maintaining a practical optimization time. The implementation of GA used in this work was GAOT (Genetic Algorithms Optimization Toolbox) for Matlab™(Houck et al., 1996).

3. Simulation-based methodology

The simulation-based strategy for automatic sizing of analog circuits is based on the results obtained by electrical simulations of the target circuit. Several runs of simulations must be performed, each one with different values for the circuit free variables. Variable perturbation is defined by the optimization meta-heuristic and the convergence for an optimal solution point depends on the correct search of the design space.

The sizing tool receives design specifications and technology model as parameters. Design specifications are the required values of circuit specifications. These values are used as objective and constraints in the optimization flow. The technology parameters and device models are used for the electrical circuit simulation of MOS transistors. Knowing the input values, the solution (population) is generated using an initialization function in the genetic algorithm. This function generates a population of possible solutions for the circuit. In the initialization function the initial solutions are generated randomly and evaluated by means of electrical simulations. The solution evaluation function analyses the constraints and the specification of the circuit to be optimized, as, for example, power dissipation, circuit area, noise or others. The design flow of simulation-based strategy using Genetic Algorithms is shown in fig. 2. The next step is to select solutions (parents) for generating a new set of solutions using the techniques of crossover and mutation previously described. The new solutions are evaluated using the electrical simulation and the evaluation function. After each iteration, new solutions are inserted in the population and the old members (old solutions) are excluded. The end of the optimization process happens when a stop condition is satisfied. The stop condition can be a maximum number of population generations (iterations) or the minimum variation of the cost function value (evaluation function).

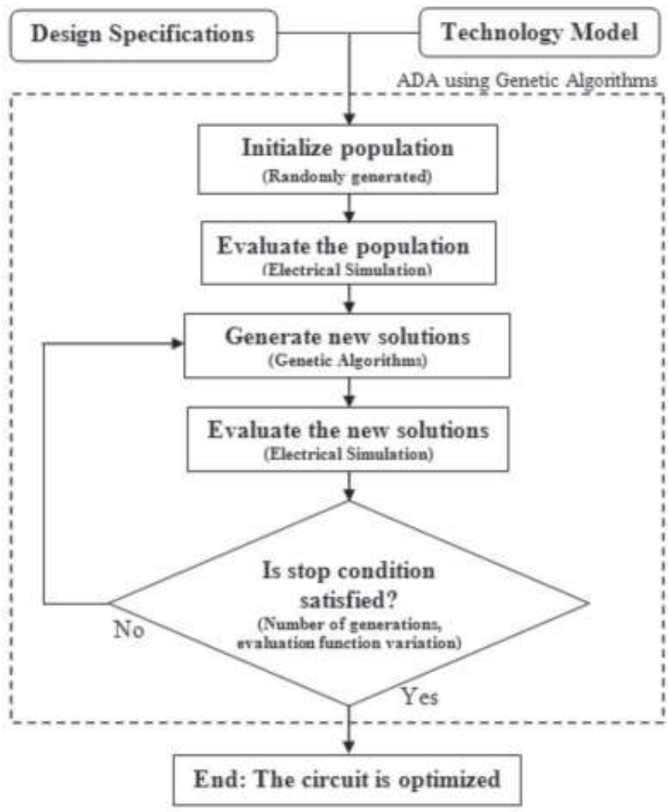


Fig. 2. Simulation-based design flow using genetic algorithms.

4. gm/I_D methodology

In the design procedure herein described, a methodology called gm/I_D is used for the circuit performance evaluation. This methodology considers the relationship between the ratio of the transconductance gm over DC drain current I_D and the normalized drain current $I_n = I_D/(W/L)$ as a fundamental design parameter (Silveira et al., 1996), such as the curve shown in fig. 3. The gm/I_D characteristic is directly related to the performance of the transistors, gives a clear indication of the device operation region and provides a way for straightforward estimation of transistors dimensions. The main advantage of this method is that the $gm/I_D x I_n$ curve is unique for a given technology, reducing the number of electrical parameters related to the fabrication process. Additionally, its analytical form covers all transistor operation regimes, from weak to moderate to strong inversion. The $gm/I_D x I_n$ curve can be automatically evaluated by electrical simulation or by measurement data. The analog circuit modeling for using with genetic algorithms is straightforward. Fig. 4 shows the proposed optimization design flow. The user enters the design specifications, technology parameters and configures the cost function according to the required design objectives and specifications. The optimization loop performs perturbations on the design variables, whose amplitude is defined by the algorithm. These variables are defined by the user, and are always related to the transistor geometry, large and small-signal parameters, such as W, L, I_D, gm and gm/I_D. Following, the design properties evaluation is performed by the calculation of the circuit characteristics such as voltage gain, cut-off frequency, phase

margin, dissipated power, input common-mode range, etc. This is done using circuit-specific analytical equations, the gm/I_D versus I_n curve and a transistor model for calculation of transconductances, drain-source saturation voltages and currents. If the circuit is feasible, i.e., transistor sizes are within an allowed range, the cost function can be evaluated and the solution is accepted if the cost decreased. The final solution returns the devices dimensions.

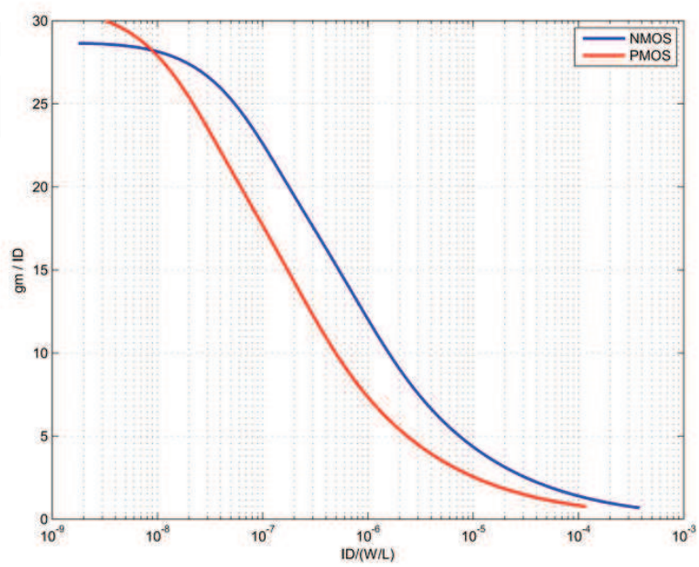


Fig. 3. gm/I_D x $I_D/(W/L)$ curves for 0.35μm CMOS technology.

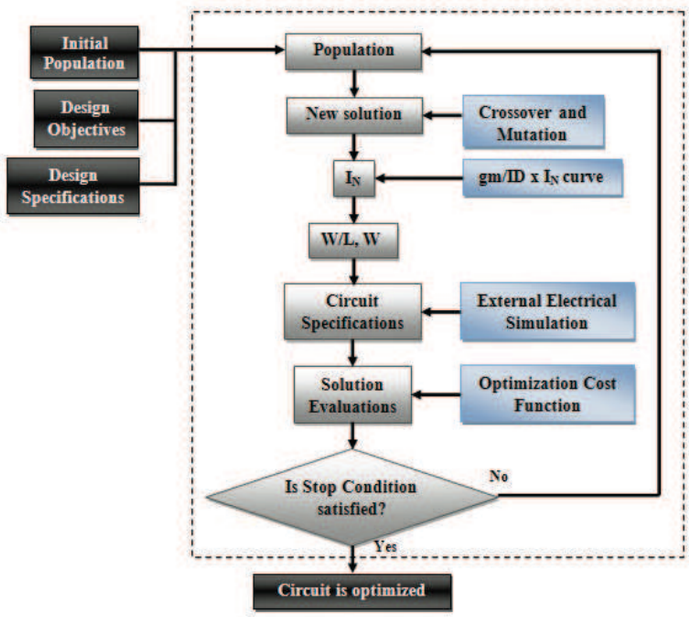


Fig. 4. Design flow for the gm/I_D design methodology.

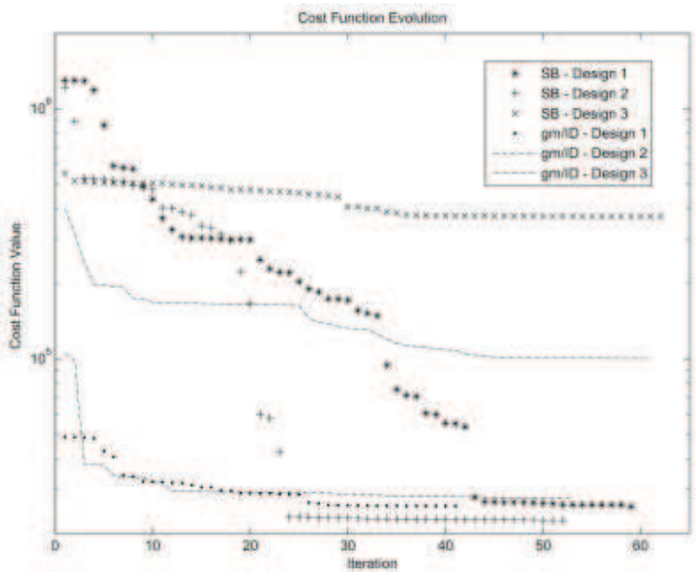


Fig. 5. Cost function evolution.

5. Design example

In order to compare both previously described automatic synthesis strategies, three corner designs were implemented for a Miller OTA, for three different specifications of gain-bandwidth product (GBW): 0.1, 1 and $10MHz$. The slew-rate, directly proportional to GBW, was also defined as 0.1, 1 and $10V/\mu s$. These designs are named Design 1, Design 2 and Design 3, respectively. The other design constraints were held unchanged for the three designs and are shown in table 1. The design objective is to minimize power consumption and area, i.e., minimize I_1 and I_2 currents according to the schematics of fig. 1, since supply voltage is constant, keeping gate dimensions as smaller as possible. The cost function equation has the same format as shown in eq. 11. Here, the performance parameter is given by

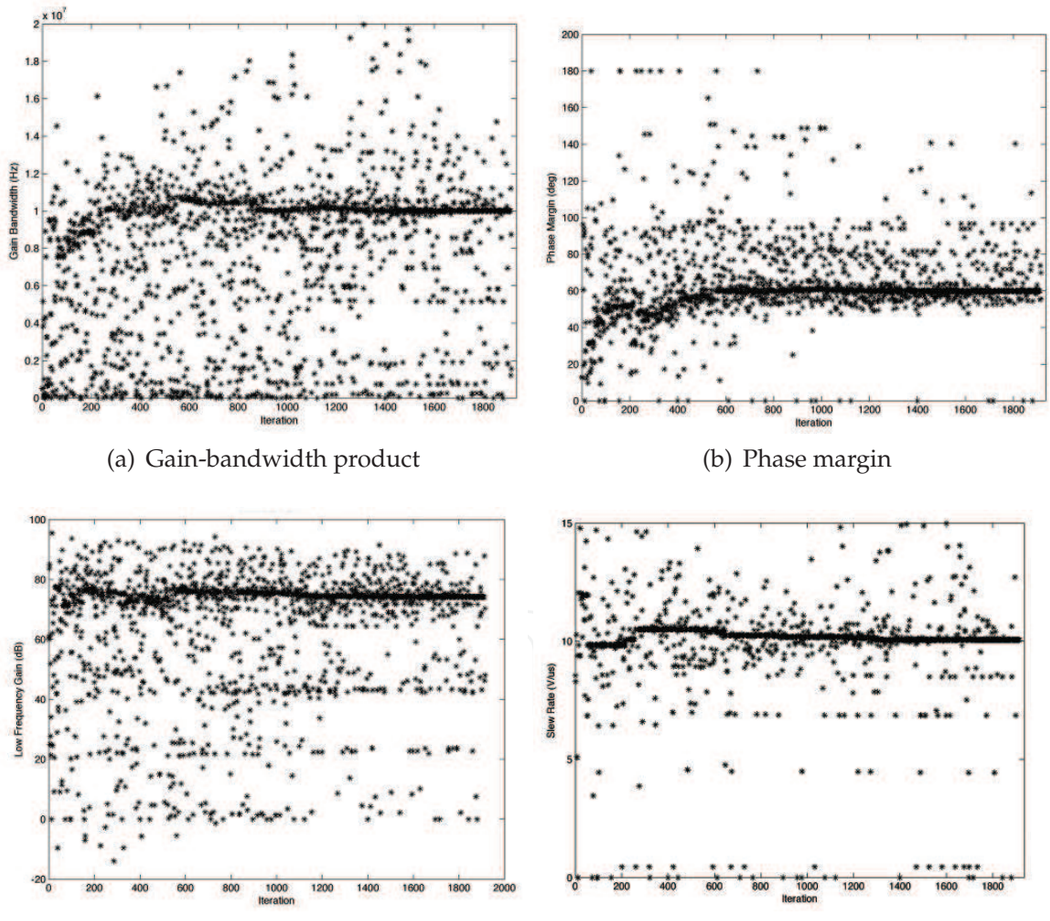
$$\hat{p}(X) = \frac{P_{diss}}{P_{diss(ref)}} + \frac{A_{gate}}{A_{gate(ref)}} \tag{11}$$

where P_{diss} and A_{gate} are the DC power consumption and gate area, respectively - estimated for each iteration - and $P_{diss(ref)}$ and $A_{gate(ref)}$ are reference values for normalization purposes. Design constraints include minimum gain-bandwidth product (GBW), minimum voltage DC gain (A_{v0}), minimum phase margin (PM), minimum slew rate (SR) and the minimum and maximum input common mode range ($ICMR^+$ and $ICMR^-$).

Both design strategies implemented used the same set of design constraints. Also, as a topology characteristic of Miller amplifier of fig. 1, some transistors need to be matched, such as the input differential pair $M1$-$M2$ and the current mirrors $M3$-$M4$ and $M7$-$M8$ (multiplication factor of 1), diminishing the number of design free variables. The AMS CMOS $0.35\mu m$ was the target fabrication technology. Transistor lengths were limited in the range between $0.35\mu m$ and $10\mu m$ and the widths between $1\mu m$ and $500\mu m$ for avoiding infeasible solutions. The value of C_{out} was fixed in $10pF$ and VDD and VSS in 1.65V and -1.65V, respectively. Next subsections describe the optimization setup for both methodologies and the comparison of results.

5.1 Methodology 1: Simulation-based

In the simulation-based (SB) methodology with genetic algorithms, the design space exploration was performed with a population of 1000 individuals. The specifications were estimated by SPICE electrical simulations using the ACM transistor compact model (Cunha et al., 1998), guaranteeing the exploration of weak, moderate and strong inversion regions. Different types of SPICE analysis need to be generated for complete performance estimation. For estimation of low frequency voltage gain, GBW and phase margin, the AC analysis is executed, generating the Bode Diagram. For the $ICMR$ evaluation a DC analysis is necessary. For slew rate, DC currents and large and small signal parameters estimation it is used the operation point (OP) analysis. Design specifications are calculated based on the simulation results. In this design, 11 design free variables were selected, including the transistor dimensions (W and L) and the bias current I_{bias}. These variables suffer a perturbation by the algorithm at each iteration and the values are updated in the circuit netlist. Fig. 6 shows the evolution of GBW, phase margin, low-frequency voltage gain and slew-rate for Design 3 in relation to the iteration number using SB methodology.



(a) Gain-bandwidth product

(b) Phase margin

(c) Low-frequency voltage gain

(d) Slew-rate

Fig. 6. Evolution of 4 design specifications for Design 3 with Simulation-Based methodology.

5.2 Methodology 2: gm/I_D

In this design strategy, the independent variables are the gm/I_D relationships and channel lengths of each transistor. All design equations are put in terms of these parameters. The drain current for these transistors can be calculated with the information about the transconductance-to-current ratio:

$$I_{Di} = \frac{gm_i}{\left(\frac{gm}{I_D}\right)_i} \tag{12}$$

With the ACM transistor model we can estimate the Early voltage according to the transistor length. The free variables subjected to perturbations by the genetic algorithm are: $L_1 = L_2$, $L_3 = L_4$, L_5, L_6, $L_7 = L_8$, $(gm/I_D)_1 = (gm/I_D)_2$, $(gm/I_D)_3 = (gm/I_D)_4$, $(gm/I_D)_5$, $(gm/I_D)_6$, $(gm/I_D)_7$, and the dependent parameters are $W_1 = W_2$, $W_3 = W_4$, W_5, W_6, $W_7 = W_8$, C_f and bias current. The range of gm/I_D is well known from device physics and behaves smoothly over a wide range of transistor biases, which is advantageous for the search robustness. Moreover, the design space is limited by values of gm/I_D between zero and $28V^{-1}$, which is the theoretical maximum gm/I_D of bulk MOS transistors. Design objectives and design specifications are evaluated in terms of free variables $(gm/I_D)_i$ and L_i. The same occurs with the dependent variables such as W_i and I_{D_i}. So, the transistor width can be calculated as:

$$W_i = \frac{I_{D_i} \cdot L_i}{I_{n_i}} \tag{13}$$

where I_{n_i} is the normalized current of the i^{th} device, given by the $gm/I_D x I_n$ curve. The design characteristics calculation is straightforward. The low-frequency gain, for example, is given by

$$A_v = \left(\frac{gm}{I_D}\right)_1 \cdot \frac{VA_1 \cdot VA_3}{VA_1 + VA_3} \cdot \left(\frac{gm}{I_D}\right)_5 \cdot \frac{VA_5 \cdot VA_6}{VA_5 + VA_6} \tag{14}$$

VA is the Early Voltage, directly dependent on gate length.

5.3 Comparison results

Table 1 shows the results of the performance obtained for designs 1, 2 and 3 using both described methodologies. Table 2 shows the transistor sizes, inversion levels and the values obtained for the bias current and compensation capacitor. Although each methodology used a totally different approach for finding an optimum design, they achieved similar results. In Design 1, with a target GBW of $100kHz$, the gm/I_D methodology provided a power consumption of $3.52\mu W$, against $4.48\mu W$ achieved by the simulation-based methodology. The values of gm/I_D of the input differential pair ($M1$ and $M2$) achieved similar values in both methodologies, located in the weak inversion region. The same is valid for Designs 2 and 3, with GBW in $1MHz$ and $10MHz$, respectively, in which the input pair biasing was also located in moderate or weak inversion. In Design 2, the SB methodology achieved the best result, with power consumption of $47.8\mu W$. In Design 3, however, the gm/I_D approach achieved a power consumption of about a third from that obtained by the SB methodology, at the expense of larger gate area.

	A_{v0} $[dB]$	GBW $[MHz]$	PM [°]	SR $[V/\mu s]$	$ICMR$ $[V]$		P_{diss} $[\mu W]$	A_{gate} $[\mu m^2]$
					+	-		
Design 1								
Spec.	70.0	0.1	60	0.1	-0.70	0.70	min.	min.
gm/I_D meth.	73.5	0.1	63	0.1	-1.64	1.32	3.52	740.8
SB meth.	73.4	0.1	61	0.1	-1.65	1.32	4.48	4420.0
Design 2								
Spec.	70.0	1.0	60	1.0	-0.70	0.70	min.	min
gm/I_D meth.	70.1	1.0	61	1.0	-1.62	1.35	58.2	502.3
SB meth.	70.0	1.0	60	1.1	-1.65	1.34	47.8	5200.0
Design 3								
Spec.	70.0	10.0	60	10.0	-0.70	0.70	min.	min
gm/I_D meth.	76.0	10.0	98	10.0	-1.64	1.31	296	6678.2
SB meth.	72.8	11.0	60	10.0	-1.59	1.44	852	2370.0

Table 1. Miller OTA synthesis results using gm/I_D and simulation-based (SB) design methodologies.

Parameter	Design 1		Design 2		Design 3	
	gm/I_D meth.	SB meth.	gm/I_D meth.	SB meth.	gm/I_D meth.	SB meth.
$(W/L)_{M1,M2}$	31.1/4.9	97.0/6.0	113.0/2.2	296.0/3.1	126.0/0.9	217.0/0.4
$(W/L)_{M3,M4}$	3.9/4.7	208.0/5.4	154.5/4.6	463.0/3.4	97.9/0.7	208.0/5.0
$(W/L)_{M5}$	35.2/3.8	600.0/1.6	143.8/0.5	673.0/0.4	335.1/0.4	306.0/0.4
$(W/L)_{M6}$	35.9/4.3	5.6/1.0	59.0/3.8	3.8/4.1	25.1/1.8	5.0/1.0
$(W/L)_{M7,M8}$	3.7/4.9	3.2/4.8	1.0/0.6	1.0/5.0	4.4/2.3	1.0/3.4
$(gm/I_D)_{M1,M2}$	25.1	28.8	23.5	27.3	17.4	26.9
$(gm/I_D)_{M5}$	20.4	28.7	25.5	28.5	21.9	18.8
$(gm/I_D)_{M6}$	14.8	8.34	7.8	2.18	2.9	0.48
I_{bias} $[\mu A]$	0.27	0.23	3.10	2.42	30.26	24.6
C_f $[pF]$	2.71	2.20	2.91	2.20	3.02	2.20

Table 2. Miller OTA transistor sizes synthesized with gm/I_D and simulation-based (SB) automatic design methodologies. (gm/I_D values are in V^{-1} and W and L are in μm.)

6. Conclusion

There are several techniques for automating analog integrated circuit design. The automation has advantages over manual design, exploiting more effectively the design space and searching for close to optimum solutions. However, circuit modeling and cost function formulation have great impact on the final optimization solution. This work presented the implementation of two different automatic design methodologies for sizing a two-stage Miller OTA: analytical gm/I_D methodology and numerical simulation-based methodology with Genetic Algorithms. Considering exactly the same conditions for both methodologies - same technology parameters, design objectives and constraints -, three power-constrained corner designs were executed for three values of GBW: 0.1, 1 and 10MHz. As the optimization results showed, both design methodologies achieved similar results, exploring weak, moderate and strong inversion regions. The slightly differences in the results demonstrate that both

methodologies, even though using distinct design strategies, are adequate for the automatic design of OTAs, with advantages over manual design. Genetic algorithms are very suitable for analog design automation by the fact that the convergence of the final solution is not directly dependent on the initial solution, and it is not necessary a deep knowledge by the human designer about the circuit characteristics. However, it is very important to determine the size of population (number of individuals) because it is directly related to the quality and to the amount of time expended by the optimization process.

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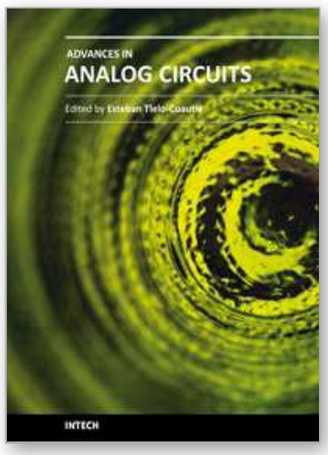
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This book highlights key design issues and challenges to guarantee the development of successful applications of analog circuits. Researchers around the world share acquired experience and insights to develop advances in analog circuit design, modeling and simulation. The key contributions of the sixteen chapters focus on recent advances in analog circuits to accomplish academic or industrial target specifications.

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