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Integrated High-Resolution Multi-Channel Time-to-Digital Converters (TDCs) for PET Imaging

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1. Introduction to TDC

PET with time-of-flight (TOF) capability has been shown to provide a better reconstructed image compared to conventional positron tomography. The increase in SNR mainly depends on the size of the patient being imaged Conti (2009), the intrinsic resolution of the detector and the resolution of the TOF. In TOF-PET approach, for each detected event, the measurement of the time of flight difference between the two 511 keV photons provides an approximate value for the position of the annihilation. The approximation is directly limited to the capability of measuring the arrival time of the two photons.
In the 1980s, TOF-PET were built with an achieved timing resolution of 500 ps Moses (2007). At that time, the electronics available drastically reduced the performances of the TOF-PET. Nowadays, electronics operating in the GHz range is routine and the application-specific integrated circuits (ASIC) are commonly used Ollivier-Henry et al. (2007). The ASIC needs to include a high-precision time-to-digital converter (TDC) for each detector element to reach the required time resolution(*i.e.*, less than 100 ps)with good stability.
The objective of this chapter is to review the state-of-the-art of the TDC techniques and to select proper architecture for PET imaging systems. Both the conventional TDCs and the novel TDCs are presented. The comparison of the TDC architecture is given as well.

1.1 Conception of a TDC

A TDC is an essential electronics which quantizes small time differences between two signals (defined as ”Start” and ”Stop”) and provides digital representations of this time interval. The funtion of a TDC is simular with an ADC. The TDC deals with the time difference rather that voltage or current differences in the ADCs, as shown in Figure 1(a). The measured time is defined as the phase difference between the positive edges of Start and Stop(Figure 1(b)). Figure 1(c) shows the transfer characteristics of a 3-bit TDC. The input is continuous time signals. The outputs are digital codes. Since the influence of the mismatches and the noise, the real transfer curve will deflect the ideal curve and generate quantization errors.
The relationship between measured time and outputs digital codes is given as

$$T_{in} = T_{LSB} \cdot \sum_{k=0}^{k=n-1} D_k \cdot 2^k \tag{1}$$

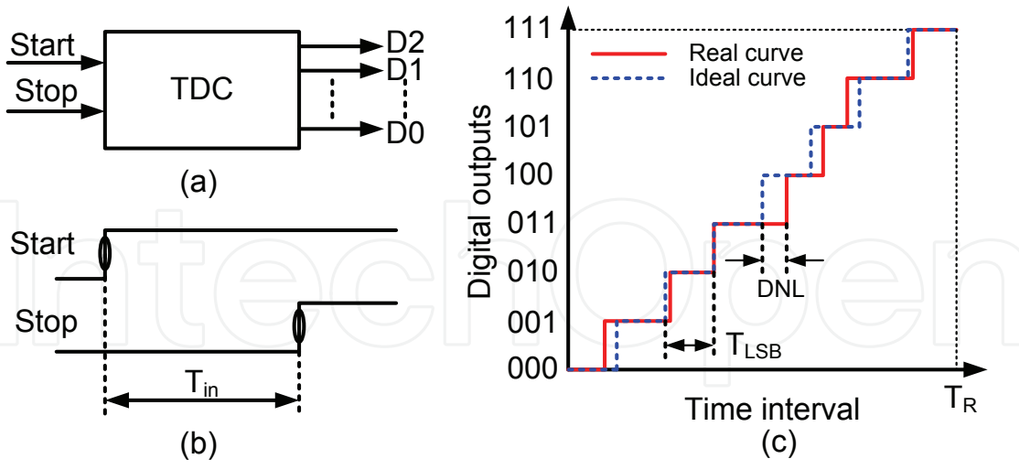

Fig. 1. Basis of time-to-digital conversion.

where T_{in} is the measured time interval between Start and Stop. T_{LSB} is the minimum unit of time measurements. n and D are the number of bits and the digital codes of the TDC outputs, respectively.

1.2 Figure of merits

The operation of a TDC is familiar with that of an ADC. So the performance merits of the ADC can be directly applied to TDC circuits. The resolution, dynamic measured range, nonlinearity and conversion speed are important characteristics to evaluate a TDC. Meanwhile, power dissipation, dead time or hit rate, and single shot precision should be considered for a TDC design.

1.2.1 Resolution

As a tool to measure time intervals, the resolution is a key parameters. The resolution of a TDC can be defined as the minimum unit of the time measurments. The dependence of the resolution is upon the circuit characteristics and noise performances.
Assuming the measured rang is T_R, the number of bits is N, the resolution is given as

$$T_{bin} = \frac{T_R}{2^N} \tag{2}$$

where T_{bin} denotes the bin size of the TDC.

1.2.2 Dynamic range

Dynamic range is the another parameter to estimate the performance of the TDC. The dynamic range is the total measured range by using the TDC. If the resolution of TDC is given, we have

$$DR = 2^N \cdot T_{LSB} \tag{3}$$

where DR refers to the dynamic range. N is the number of bits of TDC outputs.

1.2.3 Nonlinearity

The nonlinearity performances include differential nonlinearity (DNL) and integrated nonlinearity (INL). The DNL is defined as the deviation of each step from its ideal value, namely T_{LSB}. We have

$$DNL_i = T_i - T_{LSB} \tag{4}$$

where DNL_i is the ith value of the differential nonlinearity. T_i is the width of the ith step in real transfer curve.

The INL refers to a macroscopic description of the bending of a converter characteristic. It is defined as the deviation of the step position from its ideal value normalized to one T_{LSB} S.Henzler (2007). The calculation of INL is given as

$$INL_i = \sum_{n=0}^{i-1} DNL_i \tag{5}$$

1.2.4 Conversion speed

Conversion speed is a performance parameter that evaluate the speed of signal processing and device delay at each conversion time window in a TDC. This parameter is very important for high-speed applications.

1.2.5 Power dissipation

Power dissipation include both static power and dynamic power. The static power depends on the product of static consuming current and the power supply voltage.

$$P_{static} = V_{dd} \cdot I_{static} \tag{6}$$

where V_{dd} is the power supply voltage. I_{static} is the total static current. The dynamic power is determined by the switched capacitor, the power supply voltage and the clock frequency. The value is given as

$$P_{dynamic} = \alpha C \cdot V_{dd}^2 \cdot f \tag{7}$$

where α is the active factor and $0 < \alpha < 1$. C is switched capacitance. f is the clock frequency.

2. Analog TDC - the first generation

An analog TDC consists of a time-to-amplitude converter (TAC) and a high-resolution high-speed ADC, which were introduced in Tanaka et al. (1991); Bigongiari et al. (1999); Napolitano et al. (2010). The architecture of such a TDC is illustrated in Figure 2. The TAC is generally implemented by the current-integration circuit consisting of a charge-pump and a capacitor. A sample-and-hold circuit is required to provide a stable voltage signal. A high-resolution ADC digitizes this sampled voltage signal to binary codes which are the time words for the TDC.

Assuming the input time interval is T_{in}, the capacitor (C_c)is charged from zero, the amplitude of the integrated voltage is given as

$$V_{tac,amp} = \frac{1}{C_c} \int_0^{T_{in}} I_{cp} dt \approx \frac{I_{cp}}{C_c} \cdot T_{in} \tag{8}$$

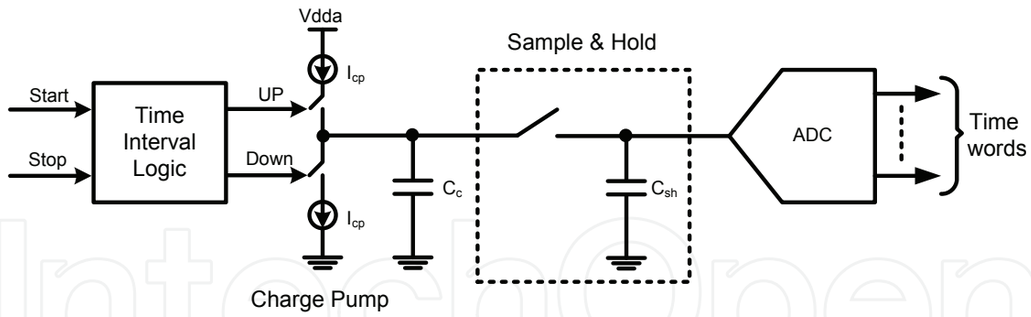

Fig. 2. Architecture of a TDC using current integration and analog-to-digital conversion.

where C_c is the charged capacitance. T_{in} is input time interval which generated from the Start and Stop signal. I_{cp} is the charging current. If I_{cp} is constant, the amplitude of the integrated voltage can be rewritten as

$$V_{tac,amp} \approx \frac{I_{cp}}{C_c} \cdot T_{in} \tag{9}$$

It illustrated that the voltage amplitude is propotional to the T_{in} with a slope of $\frac{I_{cp}}{C_c}$.
With a high-performance sample-and-hold amplifier, $V_{tac,amp}$ can be accurratly stored in C_{sh} and digitized by the ADC. Thus, we have

$$V_{tac,amp} = V_{LSB} \sum_{k=0}^{n-1} D_k \cdot 2^k + \epsilon \tag{10}$$

where V_{LSB} is the minimum resoved voltage. D_0 to D_{n-1} are the digital outputs of the ADC. ϵ is the total errors such quantization error, circuit error and noise error. From Equation 9 and 10, negalecting the errors ϵ, the relationship between the input time interval and the time words is given as

$$T_{in} \approx \frac{C_c \cdot V_{LSB}}{I_{cp}} \sum_{k=0}^{n-1} D_k \cdot 2^k \tag{11}$$

This equations means that performances of the TDC using current integration and ADC depends on both integrated precision ($\frac{C_c}{I_{cp}}$) and the resolution of ADC (V_{LSB}). Generally, with a high-resolution ADC, high-precision TDCs can be obtained.
However,the TAC and the ADC are mainly implemented by analog circuits which are not suitable for technology scaling. The design of high-performance analog and mixed-signal circuits is very complicated. Moreover, the analog circuit dissipates large static power consumption.

3. Digital TDC - the second generation

3.1 Counter-based TDC

A counter-based circuit would be the oldest and the simplest scheme. The measured time equates to the counted number multiplied by the period of the clock. The counter-based circuits have their advantages on the wide-range measurement and easier design in several technologies such as CMOS/BiCMOS process, field-programmable gate array (FPGA) Bogdan et al. (2005), and GaAs superconductive process Kirichenko et al. (2001).

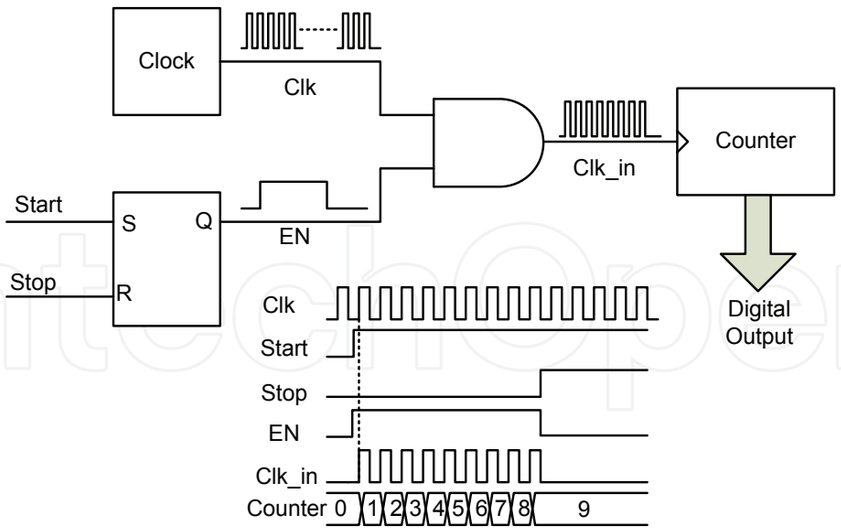

Fig. 3. The first class of the counter-based TDC Spieler (2005). The last number of the counter is the digital output which is propotional to the time difference between Start and Stop.

Two architectures of counter-based TDC have been developed. Figure 3 shows the first class of counter-based TDC. The Start and Stop signals are processed by a RS latch to generate a enable signal. This enable signal controls the width of the clock which drives the counter. The counter starts to count number when the enable signal is set to High. Thus, the last number of

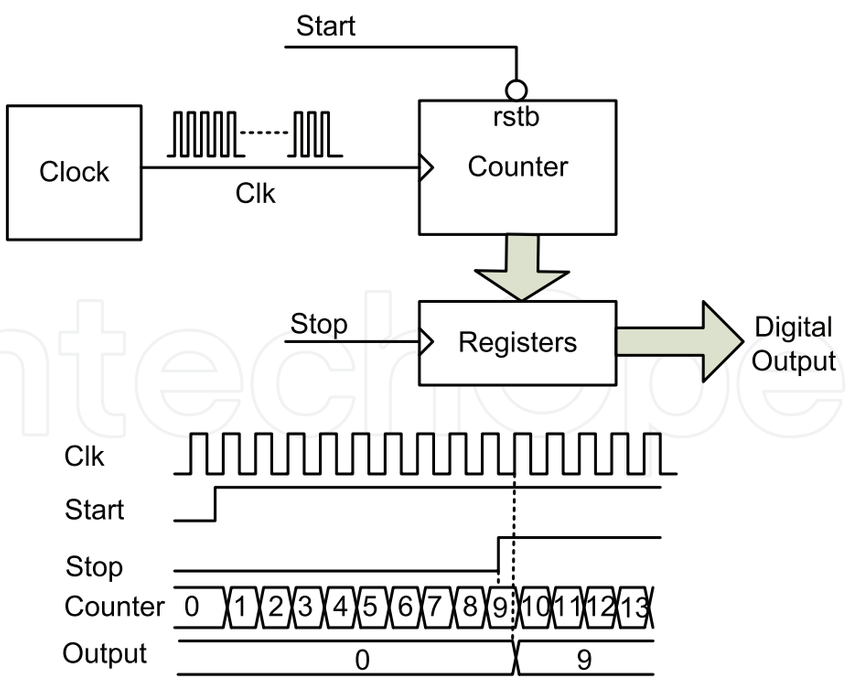

Fig. 4. The second class of the Counter-based TDC. The counter is drived by the clock and reset by the Start. The outputs of the counter is sampled by Stop. The sampled data are the digital output which is proportional to the time difference between Start and Stop.

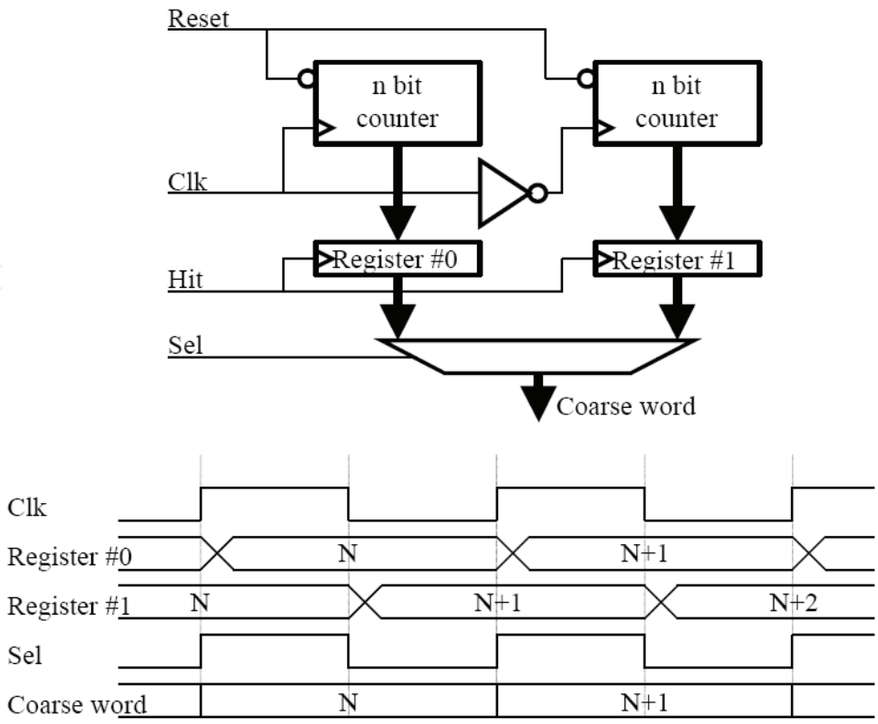

Fig. 5. The TDC using dual counters to overcome the metastability of D flip flop in the digital counters Mota (2000). Two counters operate simultaneously by using both the positive edge and the negative edge of the reference clock. Two sampled register can store the outputs of both counters. The correct data can be selected by the Sel signal.

the counter is the digital output which is proportional to the time difference bewteen Start and Stop. The counter in this architecture operates only when the Clk_in is fluctuated. Thus, low power dissipation can be achieved. However, since the RS latch and NAND gate can introduce noise on the time information from Start and Stop signals, the precision of the conversion is affected, in particular, in a high speed situation.

The second class of counter-based TDC is illustrated in Figure 4. In this architecture, the counter is drived by the clock and reset by the Start. The outputs of the counter are sampled by Stop signal. The sampled data are then stored into the registers. The stored number is proportional to the time difference between Start and Stop. This architecture can overcome the problem in the TDC shown in Figure 3. Nevertheless, the counter that operates in a continued way dissipates with large dynamic power.

Both architectures suffer from the metastability of the D filp flops in the counter. Due to the clock jitter and electronics noise, the conversion is limitted. However, the architecture shown in Figure 4 can be optimized by using Gray-code counter or dual-counter architectures. In Christiansen (1996); Mota (2000), a dual-counter was introduced of reduce the metastability. The schematic and the operational principle is depicted in Figure 5. In this architecture, two counters operate simultaneously by using both the positive edge and the negative edge of the reference clock. Two sampled register can store the outputs of both counters. The correct data can be selected by the Sel signal.

The relationship of the measured time, the converted number, the time difference and the reference clock is given by

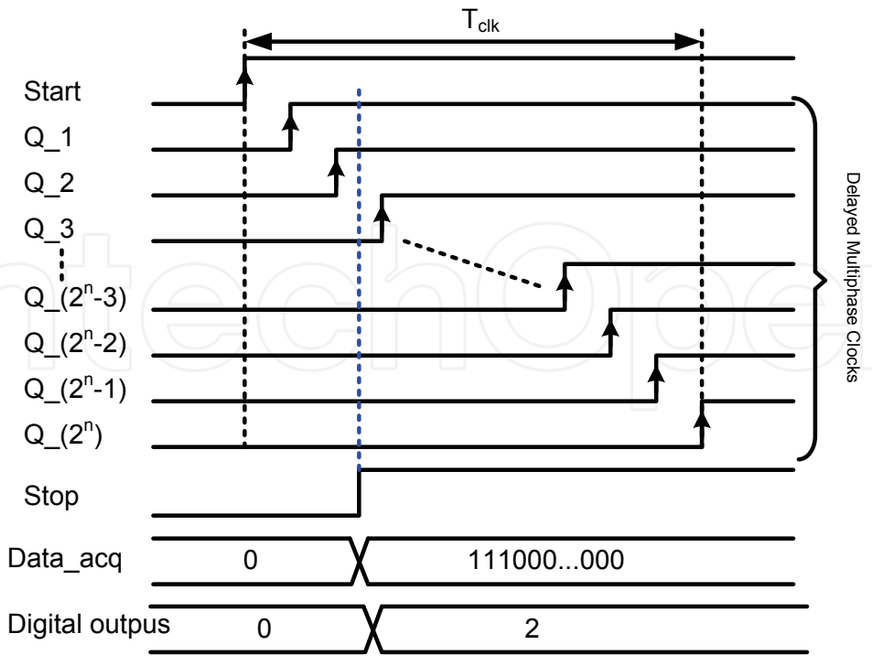

Fig. 6. The timing of the multiphase sampling.

$$T_{tdc,cnt} = T_{clk} \cdot \sum_{i=0}^{n-1} 2^{D_i} \tag{12}$$

where $T_{tdc,cnt}$ is the measured time. T_{clk} is the period of the clock. n is the number of bits for the counter. D_i is the ith digital output of the TDC. According to Equation 12, the measured range of the counter-based TDC is determined by the number of bits for the counter. Since the linearity of the conversion can not be affected by the externsion of the number of bits, the counter-based TDCs can achieve large measured range. However, the resolution is limited by the frequency of the reference clock and its conversion time depends on counted periods. These drawbacks limit its application in high-precision time interval measurement. The counter-based TDCs combined with time interpolations are usually used.

3.2 Multiphase sampling TDC

The timing of the flash sampling is shown in Figure 6. A Start signal is synchronized to the positive edge of the reference clock. The delayed clocks are generated from the Start signal with a fixed delay. The states of these delayed clocks are sampled by a common Stop signal. The acquired data are themometer codes which can be easily converted to the binary codes.
The schamatic of the flash sampling is shown in Figure 7. The delay elements with the same delay are usually implemented by the stardard gate with the delay time of T_1. The resolution is determined by T_1. In this sampling method, 2^n delay clocks are required to generate n-bit binary code.
The bin size of the time measurement is given by

$$T_{bin,mps} = T_1 = \frac{T_{clk}}{2^n} \tag{13}$$

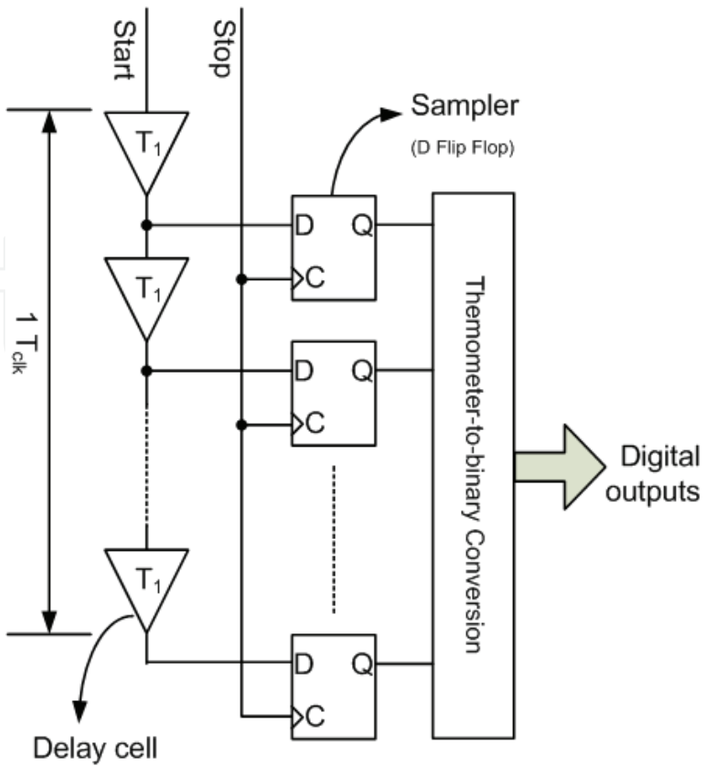

Fig. 7. The implementation of the multiphase flash sampling.

where T_1 is the delay time of each delay cell. T_{clk} is the period of the reference clock. n is the number of bits for the digital outputs. The measured time equates to the digital outputs multiplied by this bin size. Thus,

$$T_{tdc,mps} = T_{bin,mps} \cdot \sum_{i=0}^{n-1} 2^{D_i} \tag{14}$$

where $T_{tdc,mps}$ is the measured time. D_i is the ith bit of the digital outputs.

4. Sub-gate delay TDC - The third generation

The delay chain using digital gates can only deal with the resolution of gate delay which is limitted by the fabricated technology. Sub-gate delay time can be achieved by using analog delay cells built-in a delay locked loop. The multiphase sampling techniques are employed as well. However, the time interpolation such as the DLL array, the Venier delay line (VDL), and the multi-hit sampling can be used to obtain smaller time taps.

4.1 TDC based on a single DLL

The key technique of the flash sampling is to generate required delay time. The standard digital gate such as an inverter or a buffer can be employed as a delay cell. The TDCs based on gate delay were suitable for technology scaling due to its full-digital organization. However, the resolution was limited by the gate delay time. One way to get smaller time taps is to develop analog delay cells such as current-starved delay cells Swann, Blalock, Clonts, Binkley, Rochelle, Breeding & Baldwin (2004) and differential delay cells . The voltage-controlled delay

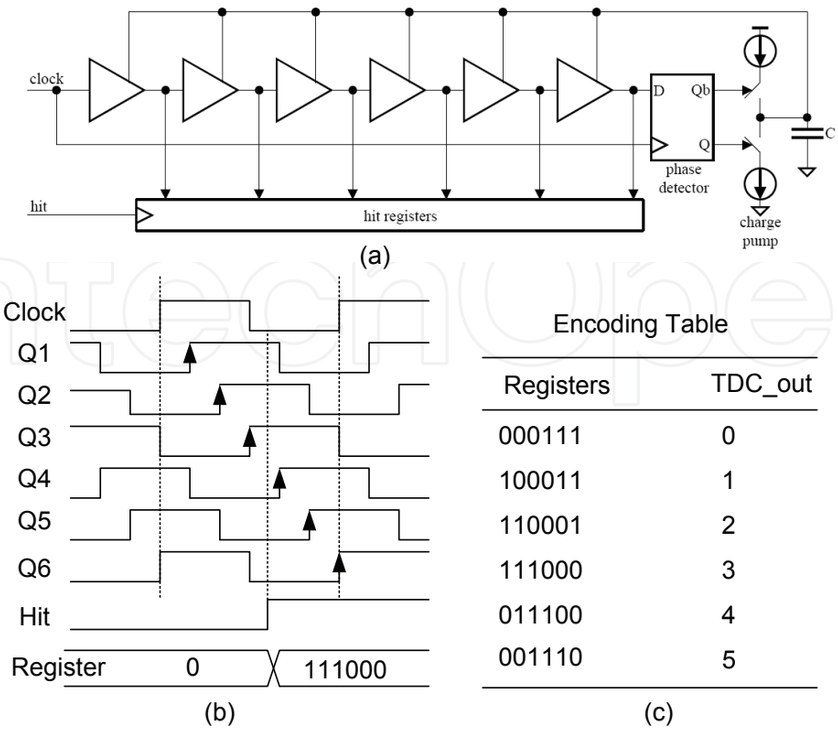

Fig. 8. TDC based on a single DLL.(a)Schematic of the TDC based on a single DLL Mota (2000).(b)The timing of the flash sampling. (c)The encoding table.

line (VCDL) embedded in a delay-locked loop (DLL) can easily generate multiphase delayed clocks in one clock period Changv et al. (2002); Baronti et al. (2001). As shown in Figure 8(a), six delay cells are embedded into a charge-pump DLL. Thus, six-phase delayed clocks can be generated. A hit signal is employed as a sampling clock. When a positive edge of the hit is coming, the state of six clocks are sampled into the hit registers. The timing is illustrated in Figure 8(b). The sampled data are fake theremometer codes which should be converted to binary codes. The encoding table is shown in Figure 8(c).
The resolution of the TDC using a single DLL is given by

$$T_{bin,dll} = \frac{T_{clk}}{N} \tag{15}$$

where, $T_{bin,dll}$ denotes the bin size of the TDC. T_{clk} is the period of the clock. N is the number of delay cells in the DLL. The dependence of the resolution of the TDC based on a single DLL is upon T_{clk} and N. Since T_{clk} is limitted by the used technology, increasing N is the unique method. However, since the minimum delay time of the delay cell is limitted by the used technology as well, N has a upper limit in the practical circuits. Moreover, the mismatch of the delay cell do not allow to integrate large number of delay cells. To improve the time resolution of this architectuer, one can try to further divide the delay of the delay cells by performing phase interpolation using an array of DLLs or other time intepolation techniques.

4.2 TDC using an array of DLL

The time interpolation using an array of DLL is one of the most effective methods to improve the resolution. Two kinds of DLLs are used to construct the array. The resolution depends on

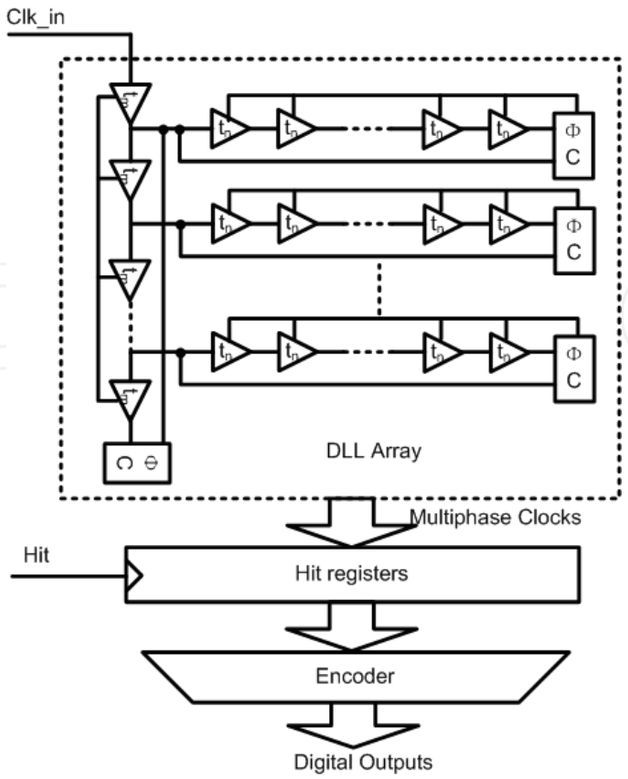

Fig. 9. TDC based on an array of DLL Christiansen (1996); Mota (2000).

the time difference of the delay cells in both DLLs. The reference clock is propogated by the array of DLLs. Smaller time taps can be obtained by using larger die area. The architecture of the TDC based on the DLL array is shown in Figure 9.
The bin size of the TDC based on the DLL array is given by

$$T_{bin,adll} = T_m - T_n = T_{clk}\left(\frac{1}{m} - \frac{1}{n}\right) = \frac{T_{clk}}{n \cdot F} \tag{16}$$

where $T_{bin,adll}$ represents the bin size of the TDC. T_m and T_n are the delay time of the delay cell in both DLLs. m and n are the number of the delay cells with the delay time of t_m and t_n. F is the number of the DLLs with the N delay cells. The bin size can be reduced by decreasing the time difference of T_m and T_n via increasing n and F. This difference can be achieved as few picoseconds. However, the jitter and the offset of the DLLs in the array limit the resolution improvement. It is very difficult to obtain the bin size of sub-picoseconds.
The principle of the time interpolation using a DLL array is, in fact, phase shift. The shift states can be illustrated in Figure 10. In this example, m, n and F are 28, 35 and 4, respectively. Thus, $T_m = 5\Delta t$ and $T_n = 4\Delta t$. Since the clock signal is continued, the positive edge of the delay clocks can be intepolated to form a time difference of Δt.
An unfortunate feature of the TDC based on the DLL array is that the array scheme is unable to produce the multiphase clocks with a number of a power of 2. This results in the digital outputs with pseudo binary codes. However, the measured result can be easily processed by off-line programming.
Since several DLLs are employed in the array, the static power dissipation is large than that in the TDC using a single DLL. Thus, low-power design should be taken into account.

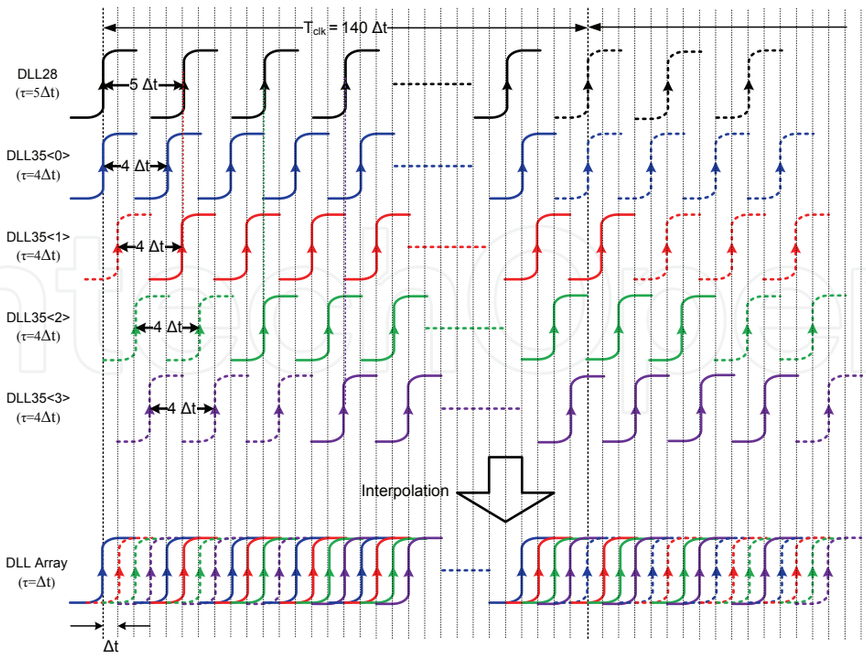

Fig. 10. Phase shift of the array of DLLs. In this example, m, n and F is 28, 35 and 4, respectively. Thus, $T_m = 5\Delta t$ and $T_n = 4\Delta t$.

4.3 TDC using a single DLL and RC delay line

Compared to the TDC using a single DLL, another method of the resolution improvement is to use multiple sampling signals delayed by the *hit* signal. The multiple sampling signals can be generated from a resistor-capacitor (RC) delay line. Since the integrated capacitor of few pF can be achieved, if the resistance is constant, the delay time, which equotes to the product of the resitance and the capacitance, can vary in the order of picoseconds as well. Thus, the bin size of the single DLL can be futher interpolated by using multiple sampling signals. The RC delay line is realized by the integrated passive elements such as Poly-resistor, Well-resistor and MOS capacitor.

Figure 11 (a) shows the architecture of the TDC based on a single DLL and a RC delay line Mota & Christiansen (1999). Assuming the number of delay cells in the DLL is N, and the number of sampling signals generated by the RC delay line is M. A register array of $N \times M$ should be arranged to store the sampled data. These sampled data are then encoded to the binary codes as the digital outputs of the TDC. The resolution of such a TDC is given by

$$T_{bin,dllrc} = \frac{T_{clk}}{N \cdot M} \tag{17}$$

where $T_{bin,dllrc}$ is the bin size of the TDC based on a single DLL and a RC delay line. T_{clk} is the period of the reference clock. If T_{clk} is constant, the bin size mainly depends on the number of delay cells in the DLL and the delayed sampling signals in the RC delay line. Theoretically, the bin size can be achieved small enough as long as the small time tap of the RC delay line can be obtained.

The implementation of the RC delay line is shown in 11 (b). Due to the parasitic resitors and capactors, the delay of the RC delay element is basically limitted by the used technology. Since the model of the parasitic parameters for resitors and capactors is not accurate, a digital

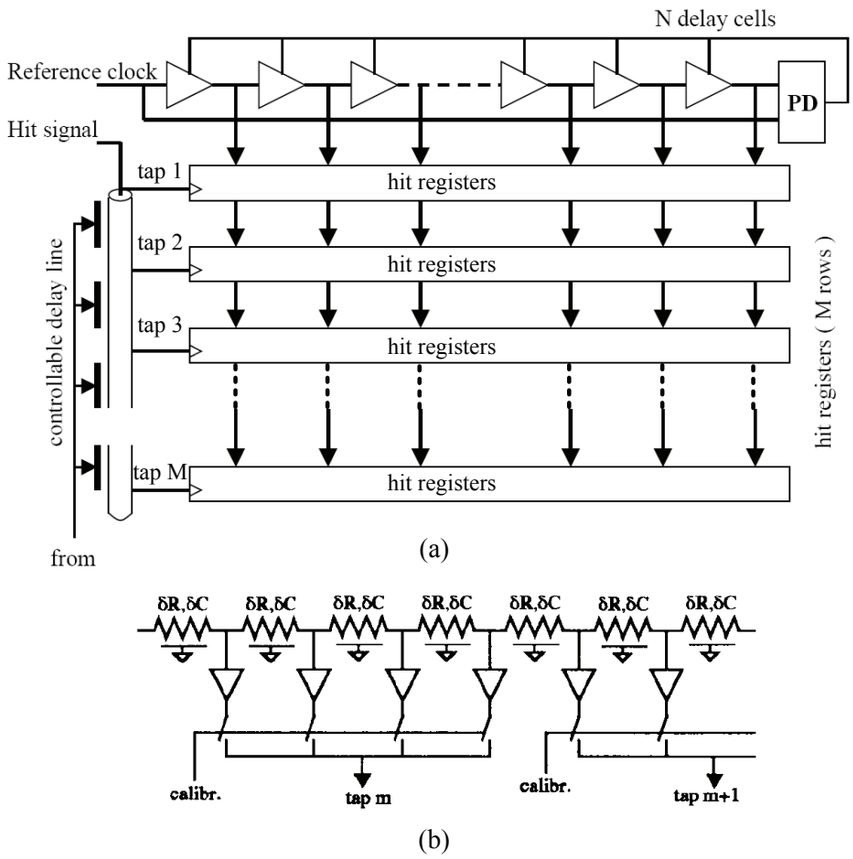

Fig. 11. TDC based on a single DLL and a RC delay line Mota & Christiansen (1999).(a) The architecture of the TDC. (b)The implementation of the RC delay line with a digital calibration circuit.

calibration circuit is required to adjust the delay time which should be compatible with the proper delay. Generally, the picoseconds-level resolution can be obtained.

4.4 TDC using Venier delay line

The Vernier sampling is shown in Figure 12. The principle of the measurements originates from the Vernier ruler. Two delay lines are required. The delay time of the delay cell in two delay lines is defferent. By using the Vernier method, the small time difference can be measured. The key point is the delay difference of the delay cell in two delay lines which should be exactly equivalent to the clock period divided by number of delay cells. In reality, the sampling process can be equivalent to the flash sampling.
The bin size of the Vernier sampling is given by

$$T_{bin,vdl} = T_1 - T_2 = \frac{T_{clk}}{2^m} \tag{18}$$

where T_1 and T_2 are the delay time of the delay cell in two delay line, respectively. m is the number of bits for digital outputs. Setting the suitable values of T_1 and T_2, the delay difference of T_1 can be interpolated by $T_{bin,vdl}$. However, the Vernier method uses multiple sampled clocks which generated from the delay line with the delay time of T_2.

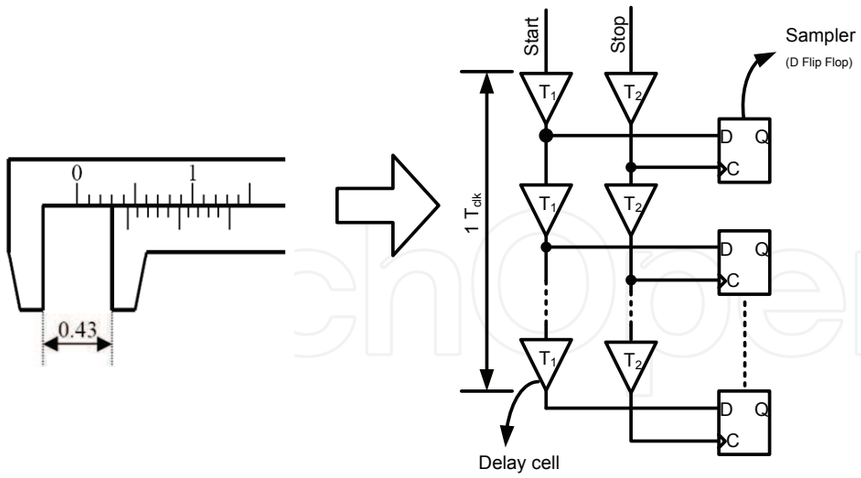

Fig. 12. Multiphase sampling using Vernier delay line Dudek et al. (2000).

To realized the TDC using vernier delay line, two DLLs should be employed. Thus, the synchronization of the multiphase clock is very important for such a circuit.

5. Sub-picosecond TDCs - the fourth generation

With the development of microelectronics and VLSI, the circuits dedictated to sub-picosecond TDC have been realized. The examples are cyclic TDCs using pulse-shrinking delay line, gated-ring-oscillator TDCs, and the TDCs using time amplifier.

5.1 Cyclic TDC using pulse-shrinking delay line

Cyclic TDC using pulse shrinking delay line Chen et al. (2000; 2005) is a low power TDC which can achieve the resolution of few picoseconds with good linearity. This TDC uses the inhomogeneity of the gates in cyclic delay line to implement the pulse shriking mechanism.
The architecture and the operational principle is shown in Figure 13. In this architecture, a Reset signal is required to ensure the T_{out} at Low level in the initial state. The input time inteval is shrinked in the delay line with a fixed width. The output of the delay line is then feedback to the input NAND gate for circular operation on the pulse shrinking until T_{out} without positive edges. A high-resolution counter is driven by T_{out} and generates digital outputs which are proportional to the measred time interval.
In the pulse-shrinking delay line, two kinds of inverters are required. One can be the standard NOT gate with the gain of one unit. The other is the inverter with the gain of β unit. Due to the difference of the input capacitance and equivalent ON resistance, the pulse will be shrinked in a fixed time interval. This shrinked delay interval depends on the dimension of the transistors, threshold voltage, power supply, temperature and other parameters. However, the influence of the temperature is an import factor for the cyclic TDC. A temperature compensation circuit is proposed in Chen et al. (2005).
Assuming the shrinked time interval is Δt, the measured time by a cyclic TDC is given by

$$T_{tdc,cyclic} = \Delta t \cdot \sum_{i=0}^{n-1} 2^{D_i} + T_{offst} \tag{19}$$

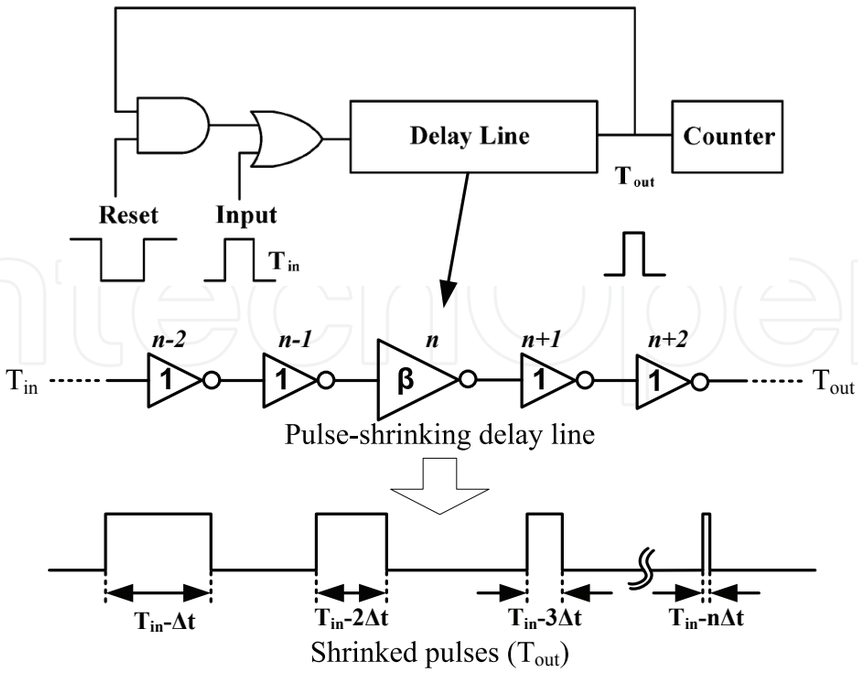

Fig. 13. Cyclic TDC using pulse-shrinking delay line Chen et al. (2000; 2005).

where $T_{tdc,cyclic}$ is the total measured time. n is the number of bits of the counter. D_i is the i^{th} digital output of the counter. T_{offst} is the offset time interval of the TDC. This offset time interval usually exists in such a TDC. The reason is that the CMOS transistor has a cut-off frequency so that the tiny pulse can not be processed by CMOS digital circuits. The value of the offset time interval is about few picoseconds in submicron CMOS technology. Thus, the measured time of the cyclic TDC is given by both the bin size (Δt) and the offset time interval. Since it consists of pure digital circuits, the cyclic TDC finds its applications on many fields. A strong recommondation is to use a cyclic TDC as a digital phase detector Liu et al. (2008) for all-digital PLL which can be used for microprocessors, high-speed interfaces, and data recovery circuits. Moreover, the cyclic TDC can be implemented not only in standard CMOS technology but also in FPGA whose cost is lower than that of a CMOS fabrication. Futhermore, the power dissipation is low for the cyclic TDC. This is an attractive feature for some low-power portable electronics.
Cyclic TDCs using pulse shrinking can obtain a resolution of few picoseconds or several hundreds femtoseconds.

5.2 Gated-ring-oscillator TDC

For high-reslution TDCs using multiphase sampling, the resolution is mainly determined by the mismatches of delay cells. Gated-ring-oscillator (GRO) TDCs Straayer & Perrott (2009) which are a novel techique can overcome this issue and achieve sub-picoseconds level precision. The architecture and principle of the GRO TDC is depicted in Figure 14.
The GRO TDC is similar to the oscillartor-based TDC Nissinen et al. (2003) which uses the multiple outputs of the oscillator for phase measurements. However, the GRO TDC only allows the oscillator to have the phase transition during a given interval measurement. It means that the gated ring oscillator operates only when the ”Enable” signal (refers to ”the

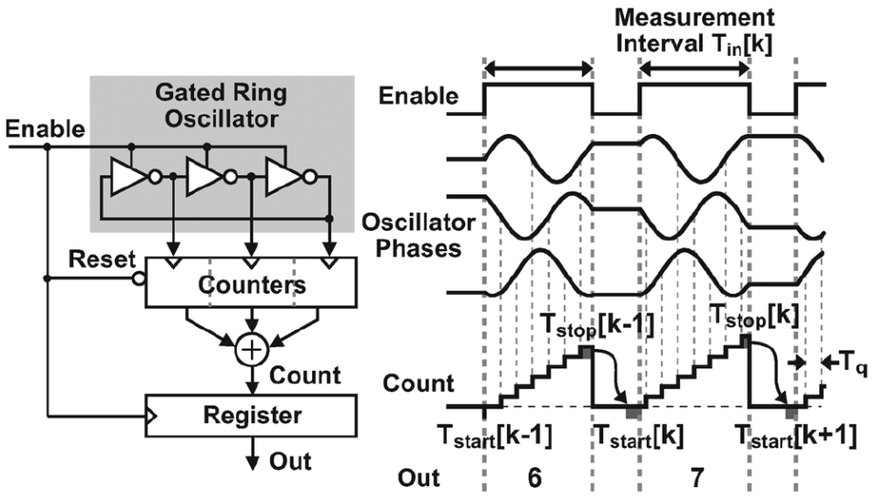

Fig. 14. Architecture and principle of gated-rign-oscillator TDCs Straayer & Perrott (2009).

measured time interval ") is high level and stops when this signal is low level. The outputs of the gated ring oscillator can be used as the clocks which drive the counter to counting numbers. One notes that the the counter is reset when the "Enable" signal is low level. Thus, the total numbers of all counters can be obtained by an binary adder. The sum of the counted number is proportional to the measured time interval.

The benefit of gating the oscillator is that the residue occurring at the end of a given measurement interval can be transferred to the next measurement interval Straayer & Perrott (2009). We have

$$T_{start}[k] = T_{stop}[k-1] \tag{20}$$

This feature can be utilized for continuous time interval measurements. Thus, the overall quatization error of the time interval measurement is given as

$$T_{error}[k] = T_{stop}[k] - T_{start}[k] = T_{stop}[k] - T_{stop}[k-1] \tag{21}$$

where T_{start} and T_{stop} are the start time interval and the stop time interval, respectively. k is the ordinal number of the measurements. This equation illuastrates that $T_{stop}[k]$ corresponds to a first-order noise shaping in the frequency domain.

Since the resolution of the GRO TDC is independent on the mismatch of the inverters, the precision can be achieved as 100 fs or less. To construct a subpicoseconds-level TDC, GRO-based architecture can be a very good choice. Moreover, GRO TDCs are realized by digital circuits which are very suitable for the technology scaling. This also introduces low static power dissipation.

However, the gated ring oscillator may suffer from non-oscillation when the time interval is enable. Thus, the design of gated ring oscillator becomes an important issue. Moreover, GRO TDCs suffer from the electronic noise and metastability as well as counter-based and delay-based TDCs.

The state-of-the-art of GRO TDCs can obtain a resolution of 100 fs.

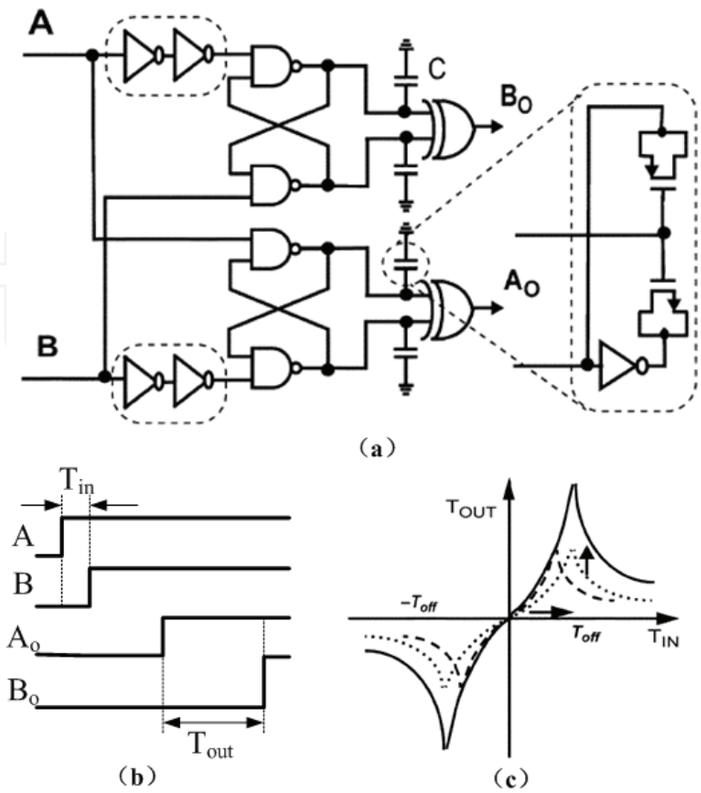

Fig. 15. Time amplifier.(a)Schematic of a time amplifier;(b)Conception of the time amplifier;(c)Characteristic of the time amplifier.

5.3 TDC based on time amplifier

It is a big challenge to measure the time interval with picoseconds-level resolution. The reason is that the performances of TDCs are mainly determined by the finite SNR and the mismatch of integrated elements. The conception of the time amplification is an effective solution for this issue. The schematic of a time amplifier (TA) which was proposed in Lee & Abidi (2007) is shown in Figure 15(a). The operation is similar with an voltage amplifer. The difference is that the TA processes a tiny time difference and outputs a larger time difference. The conception of the TA is shown in Figure 15(b). However, the circuit techniques of the TA is under developed. The state-of-the-art of the time amplifiers only can process a finite range of time interval. As shown in Figure 15(c), the transfer characteristics of the TA is not linear. Thus, the use of a TA should be based on the test results in the present age. However, the idea of time amplification gives a new research direction of TDC techniques, which needs to be optimized in the future work.

The architecture of a TA-based TDC is illustrated in Figure 16. The function of a time amplifier is simular to the preamplifier in the front-end electronics. In the neighborhood of the center point, the gain of the TA is monotone increasing, thus the behaviour of the TA is given as

$$T_{out} = K_{TA} \cdot T_{in} \tag{22}$$

where T_{in} and T_{out} are the input and output time interval, respectively. K_{TA} is the gain of the TA. Since K_{TA} is not linear, a calibration circuit is required. The TDC core could be a

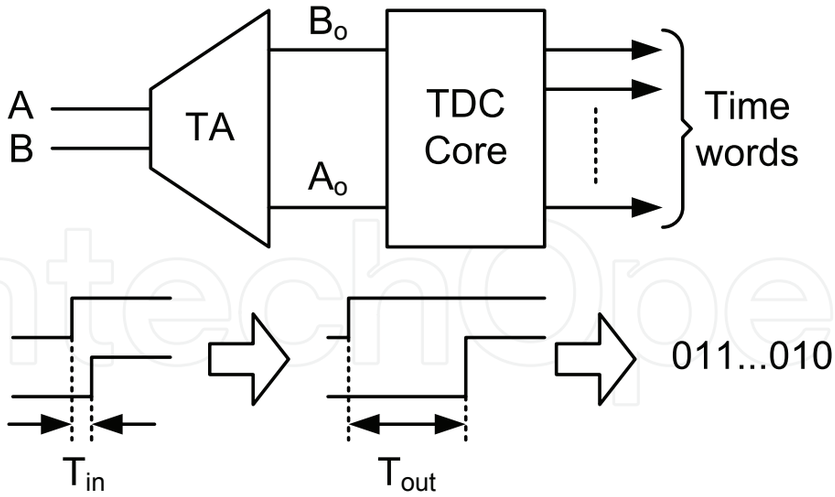

Fig. 16. Architecture of TDCs based on a time amplifier. The function of a time amplifier is simular to the preamplifier in the front-end electronics. The TDC core could be a counter-based TDC, a delay-based TDC, a GRO TDC or a TDC using a TAC and ADC.

counter-based TDC, a delay-based TDC, a GRO TDC or a TDC using a TAC and ADC. The relationship between the digital outputs of the TDC core and T_{out} is given as

$$T_{out} = T_{bin} \cdot \sum_{k=0}^{n-1} D_k 2^k \tag{23}$$

where T_{bin} is the bin size of the TDC. D_k is the digital bit. n is the number of bits for the digital outputs. From Equations 22 and 23, we have,

$$T_{in} = \frac{T_{bin}}{K_{TA}} \cdot \sum_{k=0}^{n-1} D_k 2^k \tag{24}$$

This equation means that the performances of the TA-based TDC depend on both the high-learity gain of the TA and the precision of the TDC core. With a TA, the objective of femto-second level time measurement will be realized.
The state of the art of the TA-based TDC can achieve a resolution of 1.25 ps Lee & Abidi (2007). However, the conception of time amplification can be applied to femtoseconds level time measurement.

5.4 TDCs using hybrid architecture

According to the previous disscussion, the idea of time measurement and digitizing can be categorized into three groups. First, the counter-based TDCs are used to obtain the wide measured range. Second, the TDCs using time-interpolation and multiple sampling techniques are proposed for high precision. Third, the current integration with high-resolution ADCs is introduced to profile the existed intelligent-poverty (IP) blocks (if had). However, specific applications demand custom TDC architecture with different performances. This is a motivation to develop TDCs with hybrid architecture. The mostly used hybrid architecture is counter-based TDC with time interpolation relized by a single DLL or a DLL array to persuit for both wide range and high resolution. In addition, the multiphase flash sampling together with Vernier delay line is another popular architecture for the sake of

Architecture	Counter-based	Single DLL	DLL Array	DLL+RC	VDL
Resolution	∼ns	∼100 ps	∼50 ps	∼20 ps	∼10 ps
Meas. Range	+++++	++	+++	+++	+++
Conv. speed	++	+++++	+++++	++++	++++
Power diss.	+	++	++++	++	+++
Nonlinearity	++++	++++	+++	++++	+++
Complexity	+	++	++++	+++	+++
Multi-channel	+++++	+++++	++++	+++	++++
Outputs	binary	binary	pseudo-binary	binary	binary

Table 1. Comparison of the existed TDC architectures(1)

high precision. Moreover, the time amplification can be used to these two hybrid architecture to achieve the resolution of sub-picoseconds.

6. Comparison of the TDC architectures

The performances of the existing TDC architecture are compared via the qualitative analysis. The results are listed in Table 1 and 2. The performances such as resolution, measured range, conversion speed, power dissipation, nonlinearity are considered. In addition, the design complexity, the form of digital outputs, the availible technology and the setup of multiple channels are analyzed.

From Table 1 and 2, the TDC can be divided into four groups according to the resolution. The first one is the sub-picosecond TDCs which include GRO TDC and the TDC using time amplifier. The available measured precision can be reduced 100 fs which is realized by GRO TDC. The TDC using time amplification can achieve the precision of 1 ps. The second group is picoseconds-level TDCs including the TDC using a DLL and RC delay line, VDL-based TDCs, cyclic TDC. These TDCs can achieve a resolution of about 20 picoseconds. Besides, the TDCs based on the DLL array and the TDCs using current integration and ADC techniques can be categoried to the third group which can obtain a resolution of about 50 ps $\sim$ 200 ps. The last is the nanoseconds and sub-nanosecond TDCs consisting of counter-based TDCs and the TDC using single DLL.

Among the existing TDCs, counter-based TDCs can achieve large meaured range. A 10-bit counter with a 100 MHz clock can operate in a dynamic range of 10.24 μs. The measured ranges of DLL-based TDCs including TDCs using a single DLl, TDCs based on a DLL array,

Architecture	GRO	Cyclic	Time Amp.	TAC+ADC	Hybrid
Resolution	∼100 fs	∼ps	∼1 ps	∼50 ps	ps ∼ ns
Meas. Range	++	+++	+	++++	++++
Conv. speed	+	++	+++	+++	+++
Power diss.	++	+	++	+++++	++++
Nonlinearity	+++++	++++	+	++	++
Complexity	+++	+++	++++	++++	+++++
Multi-channel	++	+	++++	+++	+++
Outputs	binary	binary	non-binary	binary	N/A

Table 2. Overall performances comparison of the existed TDC architectures(2)

TDC using a DLL and RC delay line, the VDL-based TDCs are determined by the clock period. The range is about several tens nanoseconds. The measured ranges of GRO TDCs, Cyclic TDCs and TDCs using current integration and ADC are larger than that of DLL-based TDCs. The value can be several picoseconds to several microseconds.
The conversion speed of TDCs depends on the measured methods. Due to flash sampling mechanisms, the counter-based TDCs and DLL-based TDC can construct flash TDCs which have high conversion speed. GRO TDCs and Cyclic TDCs require counting numbers so that the conversion time depends on the product of the counted number and the clock period. TDCs using current integration and ADC is determined by the sampling rate of the ADC.
The power dissipation of TDCs is determined by the circuit implementation of the blocks. Since the counter-based TDC and cyclic TDCs consist of counters and other digital circuits. It dissipates small static power consumption. Due to more counters required by GRO TDCs, they dissipate higher power than counter-based TDC and cyclic TDCs. DLL-based TDCs have moderate power consumption. However, since a DLL array is used, TDCs based on a DLL array consume very high power dissipation. TDCs using current integration and ADC mainly depends on the power of the used ADC.
Linearity is a very important performance parameter for TDCs. The dependence of this performance is upon both the architecture and the circuit techniques. Generally, GRO TDCs and cyclic TDCs can obtain very good performances on the linearity cause the measurement is independent on the mismatch. On the contrary, DLL-based TDCs suffer from the jitter due to the mismatch. The linearity of DLL-based TDCs is worse than that of GRO TDCs and cyclic TDCs but better than TDCs using the time amplifier and current integration. The linearity of counter-based TDCs is determined by the metastability of D flip flops. The value is better than DLL-based TDCs.
The design complexity is an issue that should be considered. Counter-based TDCs can be easily realized in modern CMOS technologies. However, the TDCs involving complex architecture and using mixed-signal circuits are difficult to be implemented. For example, the DLL-based TDCs that require low-jitter DLL techniques to generate precise multiphase clocks are typical mixed-sigal circuits. Except counter-based TDCs and TDCs using a single DLL, the design complexity of other TDCs is basically in the same level.
In the front-end electronics, the integration of multi-channel TDCs has become a trend to provide compact size, low power and high precision. Counter-based TDCs and DLL-based TDCs can be easily extended to multiple channels. However, the circuits should reused to construct multple channel architecture for GRO TDCs, cyclic TDC and TDCs using current intetration.
The specifications of hybrid TDCs can be customized according to specific applications. For example, the counter-based TDC with a DLL can obtain both high resolution and wide measured range. Thus, a hybrid TDC can obtain optimized performances via the tradeoff of resolution, speed, power, linearity and design complexity.

7. TDCs dedicated to PET imaging

In the field of PET imaging, few contributions are dedicated on the high-resolution TDC. The characteristics of these TDC are reviewed in the following items.

– A TDC that performed coincidence detection in a liquid Xenon PET prototype was introduced in Bourrion & Gallin-Martel (2006). The TDC architecture was based on dual counters and a DLL with 128 delay cells. The TDC, designed in 0.35 μm CMOS technology, was able to operate at 150 K and obtain a resolution of better than 250 ps.

– A 100-ps time-resolution CMOS TDC for PET imaging application was proposed in Swann, Blalock & et al. (2004). The TDC architecture combines an accurate digital counter and an analog time interpolation circuit to make the time interval measurement. The dynmaic range can be programmable without any timing resolution degradation by using a coarse counter. The fine conversion utilizes a time-to-amplitude converter followed by an 5-bit flash ADC. The bin size was 312.5 ps with a DNL of under $\pm$0.2 LSB and INL less than $\pm$0.3 LSB. The proposed subnanoseconds TDC was the first realization for the PET imaging applications.
– A fine resolution and process scalable CMOS time-to-digital converter (TDC) architecture was presented in Yousif & Haslett (2007). The TDC architecture uses a hierarchical delay processing structure to achieve single cycle latency and high speed of operation. The TDC had a 31 ps timing resolution and power consumption of less than 1 mW.
– A TDC based on Vernier method with 1.3ns timing resolution was realized by using only one FPGA (Kang, X., Wang, S. & et al., **?**. A simple smart time-to-digital convertor based on vernier method for a high resolution lyso micropet, Vol. 4, pp. 2892 2896). The obtained resolution can meet the demand for the coincidence measurement of LYSO PET detectors with a 9 ns $\sim$ 15 ns coincidence-timing window.
– A full-custom 16-channel 625 ps TDC was proposed in Ollivier-Henry et al. (Oct. 2008) at IPHC, in 2007. The coarse conversion of the TDC was realized by dual 10-bit counter with a reference clock of 50 MHz. The dynamic range is 10 us. The fine conversion is based on the multiphase sampling techniques based on a charge-pump DLL with 32 delay cells. The TDC was designed in 0.35 μm CMOS technology.

8. Conclusions

This chapter reviews the techniques of integrated TDCs. The conception and figure of merits of a TDC is firstly given. Four generations of TDC techniques are then disscussed in detail. A comparison of these TDCs is given. At last, the TDCs dedicated to PET imaging are listed. The results show that the counter-based and time interpolation are widely used in the TDC design. Such a TDC is very suitable for the proposed PET imaging which requires a multi-channel fast TDC with a sub-nanosecond resoultion.

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