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Principle Operation of 3–D Memory Device based on Piezoacousto Properties of Ferroelectric Films

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1. Introduction

At present, the main driving forces for rapidly growing the market of nonvolatile memory devices and nonvolatile memory technology are portable electronics. Technical innovations will continue to drive the increase of memory density and speed in the future. For traditional nonvolatile memory devices like NOR flash, scaling could stop even before the 32nm node, while scaling of mass storage devices like NAND flash, is going to be very difficult beyond the 20nm node, too.

In recent years, more research efforts have been devoted to finding a new memory technology able to overcome performance and scalability limits of currently memory devices. However as lithographic scaling becomes more challenging. Novel architectures are needed to improve memory device performances in embedded as well as stand-alone memory applications. It is now generally recognized that 3–D integration and vertically stacking are possible alternatives to scaling. In order to realize stacked memory cells a novel physical principle operation of a memory element is needed.

Many new ideas have been proposed to find out the solution of such problems. Recently, it were developed a rewriteable 3–D NAND flash memory chip called Bit Cost Memory (BiCS) in which it stacked memory arrays vertically (Fukuzumi & et al., 2007) and 3–D double-stacked multi-level NAND flash memory (Park & et al., 2009). However, there is a cross talk between neighbouring memory cells in the same plane and between vertical neighbours in adjacent planes, too. It is a new challenge in addition to scaling issues. The major limitation, however, is likely to be power dissipation where 3–D designs are not efficient at dissipating heat. More over 3–D architectures are required to overcome a tyranny of interconnects.

From physical point of view, a memory device based on ferroelectric phenomena is more suitable for creating 3–D architectures of universal memory devices. Ferroelectric materials can be electrically polarized in certain direction. Then, the polarization is retained after the polarizing field is removed. Therefore, these materials have intrinsic memory. Ferroelectric random access memory (FeRAM) is widely considered as an ideal nonvolatile memory with high write speeds, low-power operation and high endurance (Scott, 2000; Pinnow & Mikolajick, 2004). FeRAM also have an added significant advantage, which is high radiation hardness. FeRAM are inherently radiation-hard making it very suitable for space applications. The FeRAM with lowest active power is a voltage-controlled device as

opposed to a magnetic, a phase change and a switchable resistor type of memory, which are current-controlled devices with high power consumption. In scaled memory device, current-driven devices have not survived. There is needed a low resistance material for a nanoscale signal-line.

In order to realize all good performance of ferroelectric memory devices and to simplify a problem of creating 3–D memory devices a novel physical principle of memory device operations are needed. The one of the advantages a physical principle of ferroelectric memory device operation is Acousto-Ferroelectric Memory Device (AFeRAM) has been published recently (Krieger, 2008, 2009). The new universal memory device is called Acousto-Ferroelectric RAM (AFeRAM) makes use of acoustic method of detecting the direction of the spontaneous polarization of the ferroelectric memory cells. The physical principle of AFeRAM device operations is based on a polarization dependent of an acoustic response from a ferroelectric memory cell under the action of applied electrical field pulse. In this chapter, it will be presents physical principle, 3–D architectures and operation modes of the new type of universal memory devices based on piezoacusto properties of ferroelectric materials.

2. Ferroelectric random access memory (FeRAM)

Ferroelectric Random Access Memory (FeRAM) has been studied for over fifty years. The FeRAM devices are divided into two categories based on the readout technique: destructive read-out (DRO) FeRAM and non-destructive read-out (NDRO) FeRAM (Scott, 2000). The first one is capacitor-type, where ferroelectric capacitors are used to store the data and FeRAM with 1T/1C (or 2T/2C, etc.) configurations. This structure is composed of a ferroelectric capacitor (C) to store data and a transistor (T) to access it similar to a DRAM cell. The read operation is based on reading current, which results from changes in polarization when voltage is applied to the cell. Accordingly, the data stored in the cell are destroyed in each read cycle. In other words, the read operation is destructive. Therefore, the data needs to be re-written in each cycle. Another main issue of FeRAM memories with 1T/1C or 2T/2C configuration is that it cannot be easily scaled down. The absolute value of the ferroelectric polarization is important for capacitor-type FeRAM. It is necessary to look for new ferroelectric materials with the high intrinsic remanent polarization and using high program voltage. At the same time, ferroelectric memory cells based on ferroelectric materials with the high remanent polarization are usually characterised by low endurance as a consequence of fatigue phenomena in ferroelectric films. Moreover this FeRAM device based on ferroelectric materials with a high remanent polarization, as a rule, have bad endurance and fatigue property, which don't allow to use this type of FeRAM as DRAM device. Therefore, many companies have suspended development of this type of memory.

The second type of memory is transistor-type (like Flash), in which ferroelectric-gate field effect transistors (FeFET-type) are used to store the data (Miller, 1992; Scott, 2000). Ferroelectric-gate field effect transistors, in which the gate insulator film is composed of a ferroelectric material, have attracted much attention because the ferroelectric gate area can be scaled down in proportion to the FeFET size. Thus, FeFET has high potential for use in large-scale FeRAM with 1 Gigabit or higher density. In other words, charge density (charge per unit area) of the ferroelectric polarization is an important parameter to achieve non-volatility in transistor-type FeRAM, whereas the absolute value of the ferroelectric polarization is important for capacitor-type FeRAM.

Typical values of remanent polarization for the ferroelectric gate material are extremely different from those for FeRAM with 1T/1C configuration. The latter require remanent polarization of 20–40 μC/cm², whereas the ferroelectric-gated FeFETs can function well with 100-200 times lower remanent polarization (0.1–0.2 μC/cm²) (Miller, 1992; Dawber, 2005). However, FeFET memory devices generally have short data retention times due to leakage, depolarization, or both.

Another main issue of FeFET memory is high program voltage. In order to prevent the chemical reaction between the Si substrate and the ferroelectric film, an insulator buffer layer must be inserted between them. For this reason, the program voltage becomes large due to voltage drop on the buffer layer between Si and ferroelectric films. Nonetheless, the FeFET type memory continues to attract much interest. It is well recognized that only non-destructive read-out (NDRO) of ferroelectric memory cells should realize all good performance of ferroelectric memory devices. By the way another important feature of FeFET is its high sensitivity to intrinsic remanent polarization of the ferroelectric gate that can be used for detecting mechanical stress or acoustic waves (Greeneich & Muller, 1972; Greeneich & Muller, 1975). At the same time, the information about ferroelectric gate polarization is not lost and can be extracted by heating (pyroelectric approach) or mechanical deformation (piezoacousto approach) of ferroelectric memory cell (Krieger, 2009).

Ferroelectric materials display a number of physical phenomena (pyroelectricity, piezoelectricity), which allow us to obtain information about the intrinsic remanent polarization by generating additional charge in the ferroelectric film, which is proportional to the value and polarity of the intrinsic remanent polarization. In general, all ferroelectric materials in their ferroelectric phase are pyroelectrics and piezoelectrics. Table 1 lists based properties of some of the more commonly used ferroelectric materials (Settera, 2006).

Materials	$LiNbO_3$	SBT	$BiFeO_3$	PZT	PMN-PT
$\boldsymbol{\varepsilon/\varepsilon_0}$	28	200–300		400–1700	5000–7000
$\mathbf{2P_r}$ (μC/cm²)	1.2	10–30	80–120	30–60	42
$\mathbf{d_{33}} \cdot 10^{-12}$ (m/V^{-1})	6–23	15–20	60–80	300–600	2000–3000
p C/(Kcm²)10^{-10}	83	71	14,7	260	300

Table 1. The properties of the commonly used ferroelectric materials: $\boldsymbol{\varepsilon/\varepsilon_0}$ —dielectric constant, $\mathbf{2P_r}$—remanent polarization, and $\mathbf{d_{33}}$ —piezoelectric charge constant, p-pyroelectric charge constant

There are three general methods for determining a value and polarity of the intrinsic remanent polarization of ferroelectric film which is associated with intrinsic memory. They are a charge generation by electrical fields, charge generation by heating or cooling (pyroelectricity), and charge generation by mechanical stress (piezoelectricity). The electrical field approach is used in conventional FeRAM devices.

One of the advantageous methods to obtain information about the intrinsic remanent polarization of ferroelectric films is piezoacousto approach. Below we present piezoacousto approach which should allow us to extract information about ferroelectric polarization of memory cells by detecting an acoustic response from a ferroelectric memory cells under applied reading electrical pulse.

3. Physical principle AFeRAM device operation

Ferroelectric crystals are a subgroup of piezoelectric materials. It means that all ferroelectric materials are piezoelectric. Some ferroelectrics are excellent piezoelectrics (see Table 1). It is known that piezoelectric materials can generate useful output under simple input signal. For example, piezoelectric material will generate an electric field with the input of stress or vice versa.

The piezoelectric effect is a natural ability of piezoelectric materials to produce an electric charge, which is proportional to an applied mechanical stress. This is termed the direct piezoelectric effect. By reversing the direction (from tension to compression) of the stress applied to piezoelectric material, a sign of the created electric charge is reversed as well. The piezoelectric effect is also reversible. When an electric charge or voltage is applied, a mechanical strain is created. This property is called the inverse piezoelectric effect. In other words, when piezoelectric film is stressed electrically by voltage, its dimensions change and generate acoustic wave. When it is stressed mechanically by force or acoustic wave, it generates an electric charge. If electrodes are not short-circuited, voltage associated with the charge appears. Both piezoelectric effects are used in AFeRAM devices.

A basic characteristic of piezoelectric materials is the piezoelectric charge constant (**d**). The piezoelectric charge constant, **d** (C/N), is the polarization generated per unit of mechanical stress applied to a piezoelectric material or, alternatively, the piezoelectric charge constant, **d** (m/V), is the mechanical strain experienced by a piezoelectric material per unit of applied electric field (1).

$$\mathbf{d} = \frac{\text{Charge density}}{\text{Applied mechanical stress}}\left(\text{C}/\text{N}\right) = \frac{\text{Strain developed}}{\text{Applied electric field}}\left(\text{m}/\text{V}\right) \tag{1}$$

In general, since piezoelectric charge constant is a second-rank tensor value, it is correct to write **d** in the equations as the tensor components; in the case of polycrystalline thin films we deal with the effective value of piezoelectric charge constant, $\mathbf{d}_{\text{eff}}$. Sometimes notation d_{33} is also used to represent piezoelectric charge constant measured in the direction perpendicular to film surface.

Piezoelectric charge constant ($\mathbf{d}_{33}$) is an important characteristic of the material's suitability for AFeRAM device. Others are Young's (or elastic) modulus (**Y**), electromechanical coupling factor (**K**), and dielectric constant (**ε**). Y is an indicator of the stiffness (elasticity) of a material. Typical value of the bulk piezoelectric charge constant, $\mathbf{d}_{33}$ (C/N) for several fully poled conventional ferroelectric materials are tabulated in Table 1. At the same time, it is known that piezoelectric charge constants of ferroelectric thin films (100 nm or less) increase in several times for feature sizes of cells with lateral dimensions below 300 nm (Buhlmann, & et al, 2002).

There are two methods for determining a value and polarity of the intrinsic remanent polarization of memory cells by piezoacousto approach. The first one, the ferroelectric memory cell is stressed mechanically by pulse force or acoustic solitary wave and then the momentarily generated electric charge in the ferroelectric memory cell is measured by conventional methods or with the use of FeFET as memory element.

The second method is to measure the generated acoustic elastic solitary wave, when the ferroelectric memory cell is stressed electrically by the reading voltage pulse with special waveform. As it was mentioned before, the field effect transistor with piezoelectric gate can

be used for detecting the acoustic solitary wave, which is generated by the ferroelectric memory cell under the action of the reading voltage pulse.
The most obvious advantage of the second method is that the memory cells are not directly connected to the access and sensitive and measuring transistor by conductor wires, but exchange data with the access transistor by acoustic solitary waves. It means that there is an acoustic interconnection between the ferroelectric memory cells and the access transistor, which allows creating 3–D structure of memory device without using additional metal interconnections.

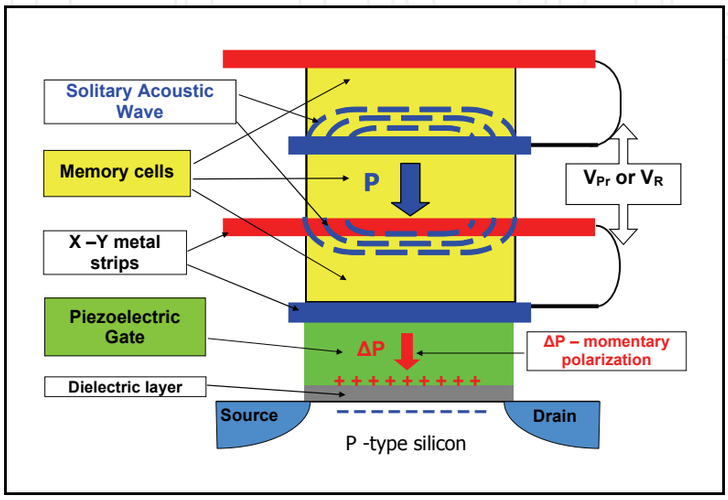

Fig. 1. Simplified structure and principle operation of AFeRAM element

In simple case, the AFeRAM element has a columnar structure (Fig. 1). The structure of the AFeRAM element can be implemented using two well know devices: a) ferroelectric capacitor or capacitors which acts as ferroelectric memory cell where two binary logic states "0" and "1" are represented by the direction of the spontaneous polarization as well as piezoacoustic transmitter; b) field effect transistor with piezoelectric or polarized ferroelectric gate which acts as acoustic sensor and access transistor. The memory cell or cells are stacked above the transistor with the piezoelectric-ferroelectric gate. The memory cells are merged with the access transistor with ferroelectric/ piezoelectric gate to form AFeRAM element. At the same time, memory cells have no electrical link to the access transistor. Ferroelectric memory cell and the access transistor exchange the information by an acoustic elastic solitary deformation wave (Fig. 1).
There is vague similarity between the AFeRAM element and piezoelectric transformer. The direct and converse piezoelectric effects are used in AFeRAM memory element as well as in the piezoelectric transformer, where voltage from one unit (in our case, from memory cell) to another (in our case, to transistor gate) is transformed acoustically.
The memory cell can be programmed in accordance with the conventional method by applying high negative electrical field (state of "0") or positive electrical field (state of "1") to the memory cell (Fig. 1).
In order to read the stored information, reading pulse voltage (V_R^{MC}) weaker than the coercive voltage is applied to the memory cell, and two types of acoustic elastic solitary deformation waves can be generated. For example, the reading electrical field, additive to the ferroelectric memory cell polarization (state "1"), will produce a tensile stress. The

reading electrical field, opposite to the ferroelectric memory cell polarization (state "0"), will produce a compressive stress. In turn, these stresses produce the acoustic solitary wave, which produces stress on the piezoelectric-ferroelectric gate of the access transistor. This stress produces a momentary "polarization" (ΔP) of the transistor piezoelectric-ferroelectric gate and controls channel conductivity of the transistor. Positive piezoelectric charges increase the effective donor concentration, reducing thickness of the surface depletion layer. Therefore, the conductivity of the semiconductor channel can be altered by the momentary piezoelectric charge due to acoustic solitary wave when it goes through the ferroelectric gate. The reading operation is thus carried out by identifying whether the current flows from the source to the drain of the transistor (state "1") or not (state "0") or vice versa. The memory cells exchange data with the access transistor by means of acoustic solitary waves. The momentary generated charges or polarization can be relatively easily calculated in terms of piezoelectric and elastic constants. Equation for the value of the momentary generated charges or polarization is as follows:

$$\mathbf{\Delta P} = \mathbf{d}_{33}^{TG} \cdot \mathbf{d}_{33}^{MC} \cdot \mathbf{Y}^{MC} \cdot \mathbf{V}_R^{MC}; \quad (2)$$

Here $\mathbf{\Delta P}$ (μC/cm²) is the momentarily generated charge or polarization within the transistor gate; $\mathbf{d}_{33}^{TG}$ and $\mathbf{d}_{33}^{MC}$ are the piezoelectric charge constants for the transistor gate (TG) and memory cell materials (MC), respectively; $\mathbf{Y}^{MC}$ is the Young modulus for the memory cell materials and $\mathbf{V}_R^{MC}$ is the reading voltage applied to the memory cell. The momentary polarization calculated within the transistor gate for different materials of the fixed memory cell and the transistor gate are presented in Table 2.

Typical thicknesses of the memory cell and the transistor gate film are 100 nm, and the reading voltage ($\mathbf{V}_R^{MC}$) is about 0.5 V. As shown in Table 2, the momentary polarization of the piezoelectric gate can exceed several times the critical value of polarization (0.1–0.2 μC/cm²) required for the transistor functioning (Miller, 1992; Dawber, 2005).

Materials for ferroelectric transistor gates	Materials for ferroelectric memory cells			
	$LiNbO_3$	SBT	$BiFeO_3$	PZT
PZT	0.25–1.72	0.47–1.0	1.22–2.25	2.25–9.0
PMN-PT	1.50–2.25	2.80–4.30	7.50–11.25	15.0–45.0

Table 2. Momentary polarization $\mathbf{\Delta P}$(μC/cm²) generated within the ferroelectric-piezoelectric transistor gate by solitary acoustic wave

It shows a very high acoustic wave sensitivity of FeFET with ferroelectric/piezoelectric gate which allows using a broad assortment of the ferroelectric materials with low value of an intrinsic remanent polarization of ferroelectric memory cells and low temperature deposition for memory cells as well as for ferroelectric/piezoelectric gate; to create 3–D structure of memory device with many memory cell layers stacked above the access transistor and to operate on a multi-bit mode to store more than one bit per memory cell (Kimura H., Hanyu T. & Kameyama M. 2003).

Another advantageous way to detect the acoustic solitary wave is to use an access and acoustic sensing transistor based on ferroelectric or piezoelectric semiconductors (e.g. GaAs,

GaN, AlN) or their heterostructure (e.g. GaAs/AlGaAs, GaN/AlN) which characterised fast the channel transit time (Kang Y., Fan Q., Xiao B. & et al., 2006; Lu S. S. & Huang C.L., 1994; Wu & Singh, 2004). In both cases the transistor channel charge and current are controlled by the gate voltage and/or by acoustic solitary wave.
Ferroelectric materials with high piezoelectric charge constants for transistor gate, like PZT or PMN-PT; and "fatigue-free" ferroelectric materials with relatively small piezoelectric charge and dielectric constant for memory cell, like $LiNbO_3$ or SBT, can be recommended.
The most obvious advantage of detecting direction and value of the polarization of ferroelectric memory cells by acoustic solitary wave is that the memory cells are not directly connected to access and acoustic sensing transistor by conductor wires. It allows easy creating 3–D structure of memory device by stacking the several layers of memory cells above array of the access transistors without using additional metal interconnections.
One of the main issues of AFeRAM devices is the echo phenomena. This problem can be eliminated and neglected by using composite packed materials with high acoustic absorption factor and acoustical impedance value equal to the silicon acoustical impedance.

4. 3-D architectures of Acousto-Ferroelectric RAM

There are several types of the AFeRAM memory storage element structures and operation modes. Basically, the AFeRAM element consists of two parts: saving (memory) area (ferroelectric memory cell or cells) and reading area (a ferroelectric field transistor) (Fig. 2, 3). There is perfect analogy between reading area of AFeRAM element and FeFET memory devices. It means that FeFET can be used as a parent element of AFeRAM memory devices. Moreover design problems for AFeRAM are already known very well and have been solved by FeFET and other FeRAM device solutions (Wang S. & et al. 2009). Furthermore, the new principle for ferroelectric memory operation does not have great demands to the remanent polarization and conductivity of the submicron ferroelectric film. It allows easy finding of new candidate ferroelectric materials for AFeRAM devices (Settera, 2006).
One of promising structures of memory elements (resembling the NAND Flash configuration) are shown in Fig. 2. In these structures, the memory area consists of cross point memory ferroelectric cells and the memory cell size is determined by crossing array between the top and bottom electrodes (Fig. 2). This memory area is relatively simple to manufacture, as one involve only three layers of metal and two ferroelectric layers sandwiched between metal strips. In this case, patterning of a submicron ferroelectric film is not needed for the memory cells. It is easy to create two levels and inexpensive memory device. Fig. 2a shows an equivalent electrical circuit of the two-layer memory area. The reading area of this type of AFeRAM element consists of FeFET with an elongated conductance channel and multi metal gate.
Another promising structure of a three-layer memory element is shown in Fig. 3. Fig. 3a shows an equivalent electrical circuit of the three-layer memory area. In these structures, the memory area also consists of cross point ferroelectric memory cells which are separated by dielectrics with different values of acoustical impedance and dielectric constant. It allows creating acoustic channels, improving anisotropy of solitary acoustic wave propagation in the stratified structure and eliminates acoustic cross talk. In these cases the reading area of AFeRAM element also consists of the piezoelectric/ferroelectric field transistor with the elongated conductance channel and the multi-metal gate.

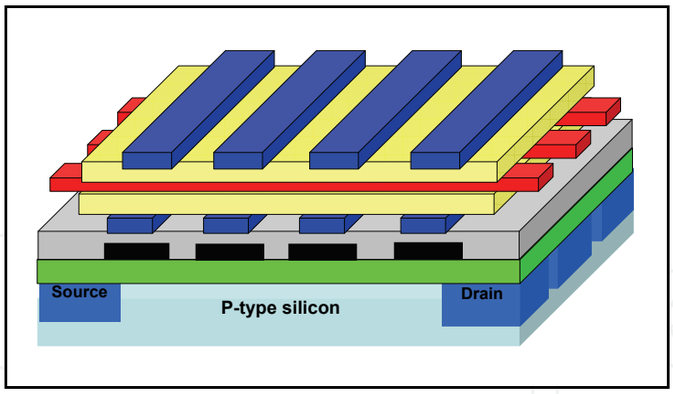

Fig. 2. Two-layer AFeRAM structure with elongated conductance channel. The memory cell size is defined by crossing strips

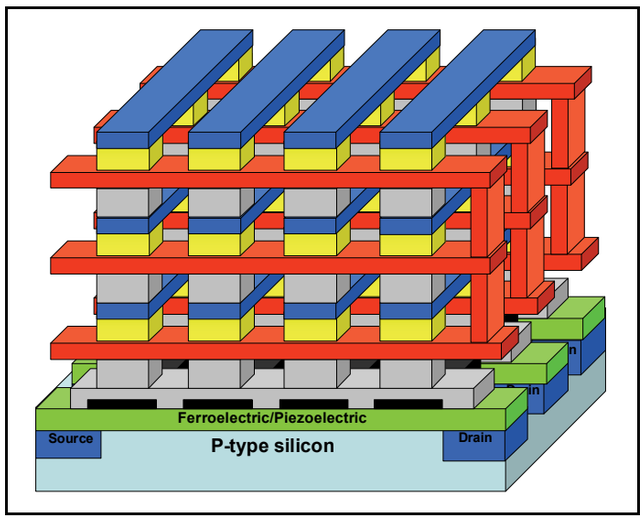

Fig. 3. Three-layer AFeRAM structure with elongated a conductance channel of access transistors. The memory cells are separated by different type of dielectrics and form acoustic channels

This type of memory element allows creating practically unlimited number of memory cell layers and can be easily scaled down to tens of nanometers electrode stripe width and use nano-ferroelectric materials (Scott , 2006).

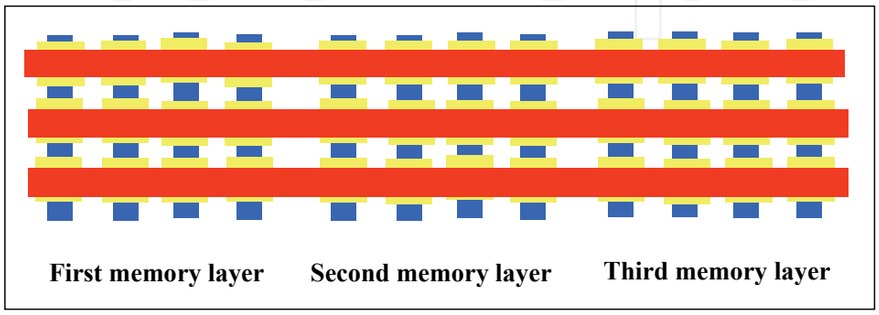

Fig. 3a. Equivalent electrical circuit for the three-layer memory area

The AFeRAM element architecture allows stacking more than one layer (four or six layers) of memory arrays (3–dimensional stacking), offers scalability, the simplest and lowest cost technology and the highest integration density (~10 Gbit/cm² for F=90 nm or ~100 Gbit/cm² for F=32 nm and four layers of memory arrays, where F denotes the smallest feature size limited by lithography resolution). The additional increase in info density can be reached by means of a multi-bit mode to store more than one bit per memory cell (Kimura, Hanyu & Kameyama, 2003).

5. Operation modes of Acousto-Ferroelectric RAM

A memory area of all type of AFeRAM elements consist of cross point ferroelectric memory arrays. The cross point memory arrays are relatively simple to manufacture, as they only involve two layers of metal and some ferroelectric layer sandwiched between. They typically have high density. The electrodes are typically arranged in an X and Y conductive strips, with each cell of the cross point array being located at the points in the ferroelectric materials where the X and Y strips cross over each other. The data bit stored in each cell has a value determined by the polarity of the ferroelectric material at that point. The polarity is controlled by application of voltages on the X and Y strips. Typically, the X strips are referred to as word lines and the Y strips are referred to as bit lines. Write operations and read operations are normally accomplished by applying voltages to the word line and bit line of the cell. In this case, ferroelectric capacitors can form a ferroelectric memory array in the same way as magnetic cores form a core memory.

5.1 Writing operation modes

Writing operation modes will be illustrated by the example of the two-layer AFeRAM structure with elongated conductance channel (Fig. 2). As it was mentioned above, the ferroelectric memory cells of AFeRAM element can be programmed with conventional method (Fig. 2a) by applying a high negative electrical field (state of "0") or positive electrical field (state of "1") to the memory cell. In order to program the ferroelectric memory cell, the program voltage (V_{Pr}) across the ferroelectric capacitor must exceed the coercive voltage (V_C), hence, $V_{Pr} >= V_C$.

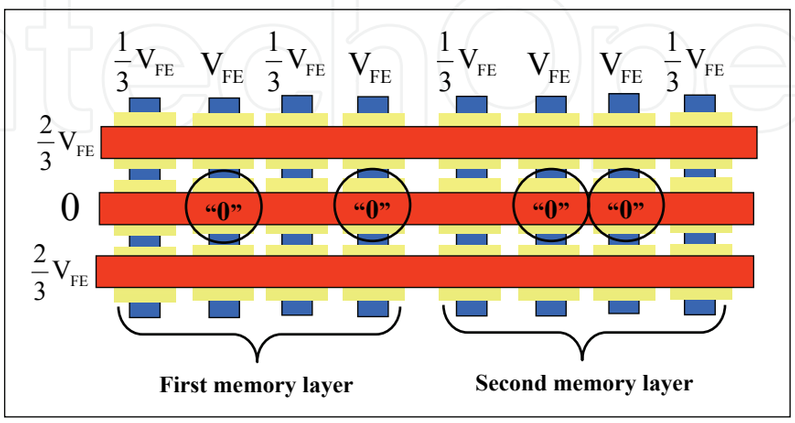

Fig. 2a. Equivalent electrical circuit for the two layer memory area and writing mode (program "0" state)

There are two voltage pulse protocols to write information into the ferroelectric memory cells which are the 1/2V protocol and the 1/3V protocol. Despite the fact that passive memory array is relatively small, a voltage pulse protocol based on the 1/3 voltage selection rule (1/3V protocol) should be used in order to keep disturb voltages at minimum (Fig. 2a). It is possible to write data to multiple cells in both schemes; word line by word line (Fig. 2a) or bit line by bit line, but this cannot be performed simultaneously for the "1" state and "0"states.

To write a "0" state by using the 1/3V protocol, the corresponding bit line of the cells to be written is connected to V_{Pr} and the corresponding word line to V=0. All other bit lines are connected to $1/3V_{Pr}$ and all other word lines to $2/3V_{Pr}$ as can be seen in Fig. 2a. The voltage drop on all non accessed cells is $1/3V_{Pr}$ or $-1/3V_{Pr}$, which means, that the distortion voltage is reduced in comparison to the 1/2V protocol. Writing a "1" is similar but this time the voltages of the word lines and bit lines are exchanged (Fig. 2b). The three-layer as well as multi-layers AFeRAM devices would operate in much the same manner as analogously to the two-layer AFeRAM elements.

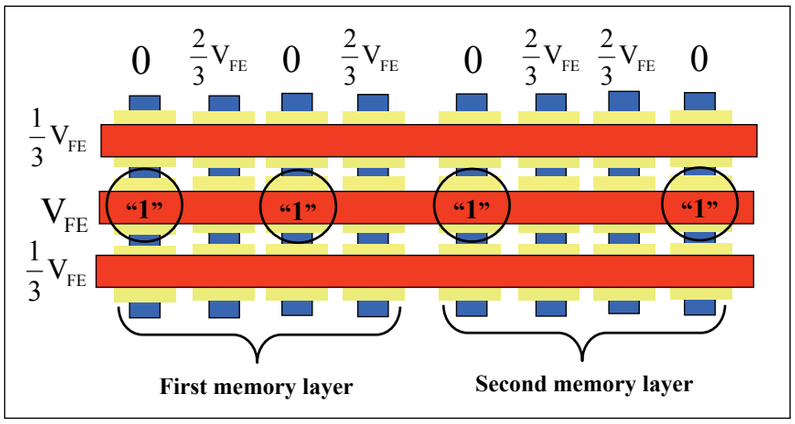

Fig. 2b. Equivalent electrical circuit for the two-layer memory area and writing mode (program "1" state)

As it was mentioned before, the one of important features of FeFET which uses as reader of the polarization memory cell is its high sensitivity to a mechanical stress or acoustic waves (Greeneich & Muller, 1975). It allows using a low voltage to program memory cell. Therefore, it should be possible to use value of the program voltage very closely to the coercive voltage V_C as soon as possible. As result endurance can be increase to up $10^{15\text{-}17}$ (Joshi, 2000). It allows using AFeRAM element as DRAM device. Moreover, the low switching voltages for programming is a definitive advantage for low-power applications, system management issues, and scalability.

5.2 Reading operation modes

Reading operation modes will be illustrated by the example of the three-layer AFeRAM structure with elongated conductance channel and multi-gate field effect transistor (Fig. 3). The reading operation mode of for the three-layer memory area of AFeRAM memory element is shown in Fig. 3b, 3c. In order to information read-out from AFeRAM element; the reading pulse voltage (V_R) weaker than the coercive voltage is applied sequentially to the memory cells (a, b, c, and d) (Fig. 3b, 3c).

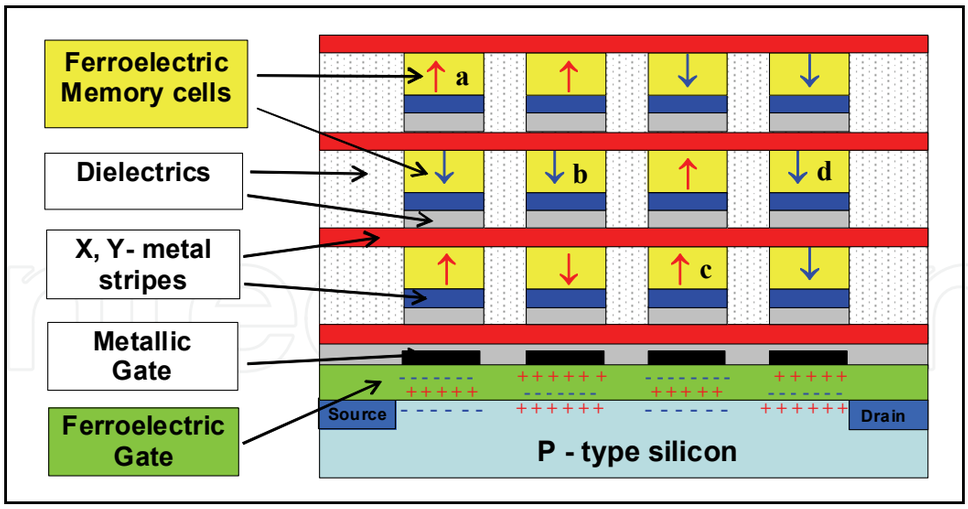

Fig. 3b. Cross section of three-layer 3-D structure memory element and reading mode of memory cells (**a**, **b**, **c** and **d**)

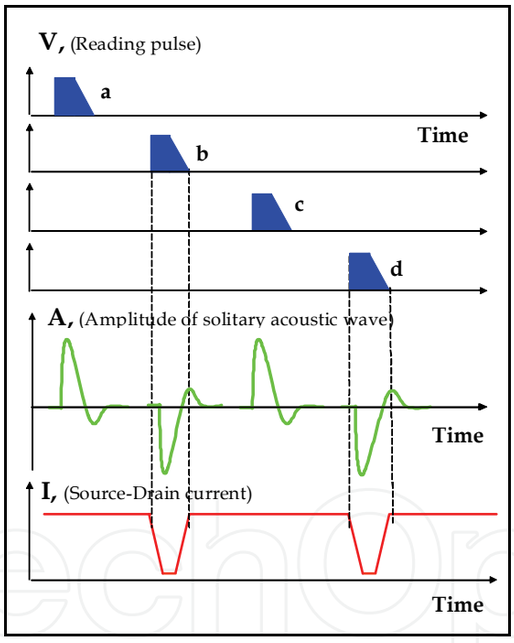

Fig. 3c. Timing diagram of the reading pulse voltages for each of the memory cells (a, d, c and d on Fig. 3b), amplitude of solitary acoustic wave generated by memory cells and the corresponding source-drain current through the semiconductor channel of the access transistor

Fig. 3c shows a timing diagram of the reading pulse voltages with special waveform for each of the memory cells, its acoustic response under the action of the reading pulse voltages and the corresponding current through the semiconductor channel of the access transistor. Initially, the access transistor is opened by metal gates and the maximum current flows easy from the source to the drain of the access transistor (Fig. 3c). Two types of acoustic elastic solitary deformation waves (or shock waves) can be generated (Fig. 3c) by

memory cells. Memory cell (state "1") will produce a tensile acoustic solitary wave and memory cell (state "0") will produce a compressive acoustic solitary wave under the action of the positive reading pulse (Fig. 3c). In turn, only compressive acoustic solitary wave which are generated (Fig. 3c) by memory cells (b and d) (state "0") produce the positive momentary "polarization" (**ΔP**) of the transistor ferroelectric gate and interrupts current through the semiconductor channel of the access transistor. The reading operation is thus carried out by identifying interrupt of current through the semiconductor channel of the access transistor by check out state "0" of memory cells (Fig. 3c).
The memory cells exchange data with the access transistor by means of acoustic solitary waves. The highest frequency exchange data between the memory cell and the sensitive transistor can extend to the GHz range (Greeneich & Muller, 1975) and is determined by the transistor frequency response and ultimately by the channel transit time.
The piezoacousto approach also allows us to use a parallel reading without distortion of nonselected cells, bit line by bit line (Fig. 2c, 3c). These modes effectively reduce the programming and reading time per byte by factor of 16 or 64 or more. This factor is determined by size of the memory array. It is also important to notice that the reading and programming periphery circuits of the passive memory array are the same.

6. Conclusion

In order to improve the performance and scalability of today's memory devices, a lot of new memory technologies are under investigation now. The goal these investigations to find the ultimate universal memory that combines fast read, fast write, non-volatility, low-power, unlimited endurance and high info density.
Forecasting the future of solid state memory leads us to the inescapable conclusion that lithographic scaling becomes more challenging and memory companies should be turning their sights to investigation of 3-D memory technology based on stackable cross-point memory arrays. At the same time, in 3-D memory architecture, current-driven memory devices with high power dissipation which is developing now can not be used.
Today it is known only one physical principle operation of a voltage-controlled memory device with low power consumption and dissipation; it is ferroelectric memory with intrinsic memory phenomenon. Unfortunately, reading operation mode of conventional FeRAM devices which are developed and manufactured now do not use all good performances of the ferroelectric memory phenomenon and its lithographic scaling becomes more challenging beyond the 90 nm node.
The AFeRAM concept uses the two physical properties of a ferroelectric film (two-in-one), the intrinsic memory phenomenon for information storage and piezoacousto property for effective read-out info. It allows the design and implementation of 3-D memory devices with universal characteristics of the inherent ferroelectric memory. Furthermore, there is no limitation in future AFeRAM miniaturization in the sense of the operational principle and can be shrunk down into the nanometer range that is a great advantage compared to current-controlled memory devices. Acoustic principle of ferroelectric memory operation does not require high remanent polarization value and value of conductivity of a submicron ferroelectric film. It allows us to easily find a new candidate among ferroelectric materials. Very high acoustic wave sensitivity of the FeFET with ferroelectric gate allows us to use a wide range of ferroelectric materials or use an access and acoustic sensing transistor based on ferroelectric or piezoelectric semiconductors, which characterised fast the channel transit

time. More over, the new type of memory device can be based on very well investigated and developed a ferroelectric or piezoelectric transistor which can be used as a parent element of AFeRAM device and a memory array with passive cross-point structure. Due to the many analogies between AFeRAM and 1T/1C FeRAM, FeFET FeRAM and Flash, several design issues for AFeRAM are already known and have been solved by applying prior Flash, FeRAM solutions.

The new operation principle of memory devices based on piezoacousto properties of ferroelectric films will help to realize all good performance of ferroelectric memory devices and to simplify a problem of creating 3–D memory devices for portable electronics with universal characteristics and low power consumption. The acoustical interconnection allows creating not only 3–D stand-alone or embedded ferroelectric memory device, but other implementations have been proposed. Specifically, it can be use for the fast exchange (GHz frequency range) info between memory zones and a microprocessor.

New electrically accessible and voltage-controlled AFeRAM device with universal characteristics, high density and low power dissipation should involve a revolution in computer architectures. The simplicity of having the ability to use a single memory type and having all computer memory in a nonvolatile system brings us back to the architectures used by system designers forty years ago, when simple memory cells based on magnetic cores was used. Acousto-Ferroelectric RAM would become the ultimate universal memory device compatible with the CMOS technology and can replace DRAM, Flash as well as HDD in modern portable electronic devices such as mobile phones and notebook computers.

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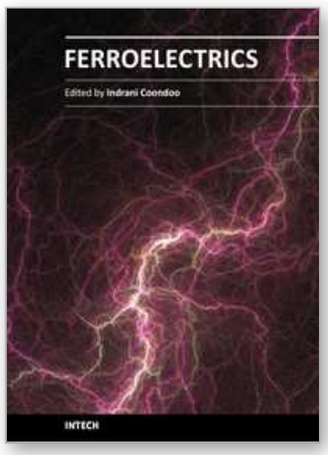

Ferroelectrics

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Ferroelectric materials exhibit a wide spectrum of functional properties, including switchable polarization, piezoelectricity, high non-linear optical activity, pyroelectricity, and non-linear dielectric behaviour. These properties are crucial for application in electronic devices such as sensors, microactuators, infrared detectors, microwave phase filters and, non-volatile memories. This unique combination of properties of ferroelectric materials has attracted researchers and engineers for a long time. This book reviews a wide range of diverse topics related to the phenomenon of ferroelectricity (in the bulk as well as thin film form) and provides a forum for scientists, engineers, and students working in this field. The present book containing 24 chapters is a result of contributions of experts from international scientific community working in different aspects of ferroelectricity related to experimental and theoretical work aimed at the understanding of ferroelectricity and their utilization in devices. It provides an up-to-date insightful coverage to the recent advances in the synthesis, characterization, functional properties and potential device applications in specialized areas.

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