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Ultra wideband oscillators

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1. Ultra Wideband Oscillators

1.1 Introduction

Ultra wideband (UWB) wireless technology has promoted designing devices covering wide bandwidth over several gigahertz. Among them are UWB oscillators that should achieve very wide tuning range along with low phase noise performance.

An effective solution to this has been to use multiple narrowband VCOs, each covering a portion of the required range. This solution requires high cost and increased design complexity. Alternatively, varactors, switched capacitors, variable inductors, and tunable active inductors are proposed to extend the tuning range of VCOs. However, there are several challenges in realizing integrated VCOs with these techniques.

This chapter deals with the analysis and design of integrated oscillator circuits, with emphasis on Ultra Wideband (UWB) application. First, VCO fundamentals are introduced and the impacts of wideband operation on VCO performance are discussed. After that, the general guidelines in doing layout for active and passive devices will be presented. Focus will be placed on the optimum RF performance of components. Then, the design considerations along with various tuning methods for wideband oscillation will be introduced. In each case, the achieved tuning range realized through these methods is mentioned. Finally, the design and implementation of two Ultra wideband (UWB) VCOs are described, with the experimental results in a 0.18-μm CMOS technology.

1.2 Specification of Oscillator Properties

The most critical performance specification for an oscillator is its spectral purity, usually characterized by phase noise. In a receiver, the phase noise of the local oscillator (LO) degrades the received signal-to-noise ratio (SNR) of the desired signal at IF by a process often referred to as reciprocal mixing. This limits the ability to detect a weak signal in the presence of a strong signal in an adjacent channel. Phase noise also corrupts the information present in phase-modulated signals by effectively rotating the symbol constellation, degrading the bit error rate (BER) of communication systems. In a transmitter, LO phase noise is modulated onto the desired signal and results in energy being transmitted outside of the desired band.

Since many wireless transceivers are battery-powered, it is required to minimize the power consumption in oscillator. There is a trade-off between phase noise and power consumption until the voltage swing is maximized. Beyond this swing level, raising the current will increase the phase noise, and will waste power.

1.3 Single Transistor Oscillator

Colpitts and Hartley oscillators are two most popular single transistor topologies, as illustrated in Figure 1. The Colpitts oscillator has a capacitively tapped resonator, with a positive feedback provided by an active device.

In Hartley oscillator, the LC network has two inductors and one capacitance. The NMOS amplifier is connected in a common gate configuration. The capacitance C3 has one port connected to L1 and the other port connected to L2. There is no way to replace this capacitance with the load capacitance.

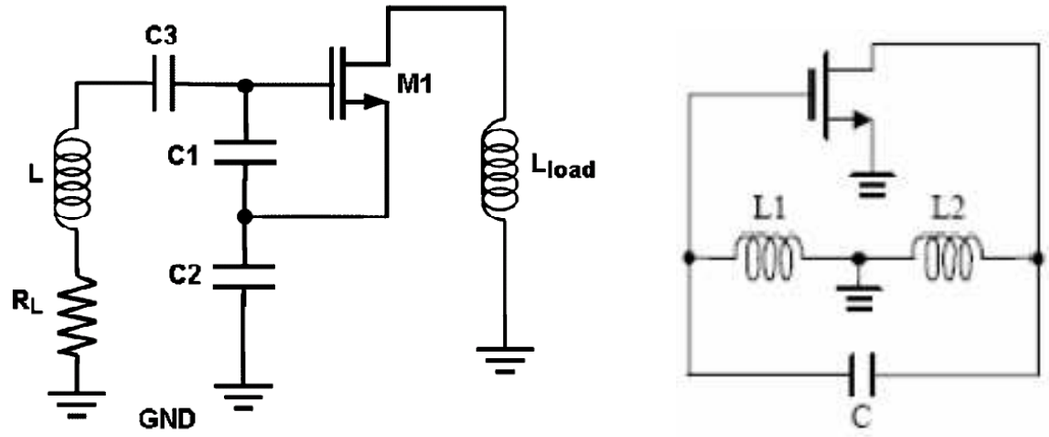


Fig. 1. AC equivalent circuit a) Colpitts VCO with a load inductor **b)** Hartley Oscillator

1.4 Differential Oscillators

The single-switch VCO (SS-VCO) and the double-switch VCO (DS-VCO) are two popular topologies used in the design of integrated oscillators. Figure 2 shows the simplified circuit schematic of both topologies. The transconductance in both circuits, which is set by the bias condition and the dimensions of the cross-coupled pair transistors, provides a negative resistance to compensate the losses in the resonator.

To control the negative resistance and hence set the oscillation amplitude, a tail current source is employed (transistor M3 in Fig. 2(a) and (b)). The presence of the tail current source, which reduces the oscillation headroom, affects the up-conversion of 1/f and thermal noise to phase noise as well [1].

In the SS-VCO two integrated inductors or a single center-tapped differential inductor may be employed, while a single center-tapped can be used in the DS-VCO. The parasitic capacitances associated with the transconductor cell are larger in the DS-VCO than in the SS-VCO. The parasitic capacitances reduce both the tuning range and the maximum oscillation frequency. The oscillation amplitude of the DS-VCO, for identical resonators and equal power consumption, is anticipated to be twice as large as in the SS-VCO [2]. Thus, DS-

VCO exhibits better phase noise performance compared to the SS-VCO. However, the former requires a larger supply voltage than the latter, due to the additional stacking of the PMOS pair.

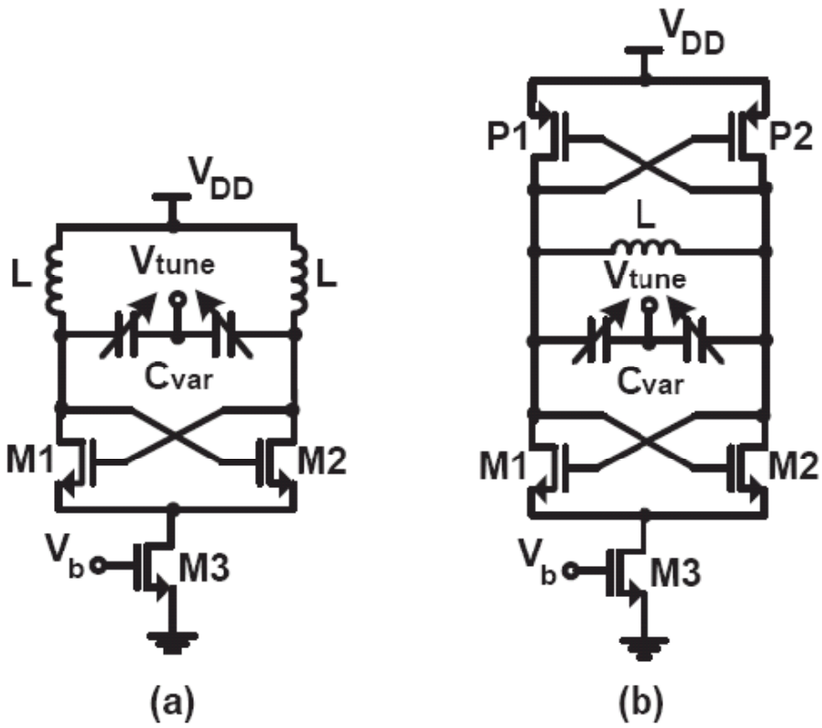


Fig. 2. Simplified circuits schematic of (a) the SS-VCO and (b) the DS-VCO.

1.5 Phase Noise

The most critical performance specification for an oscillator is its spectral purity. In any practical oscillator, the spectrum has power distributed around the desired oscillation frequency ω_0, known as *phase noise,* in addition to power located at harmonic frequencies, as shown in Figure 3.

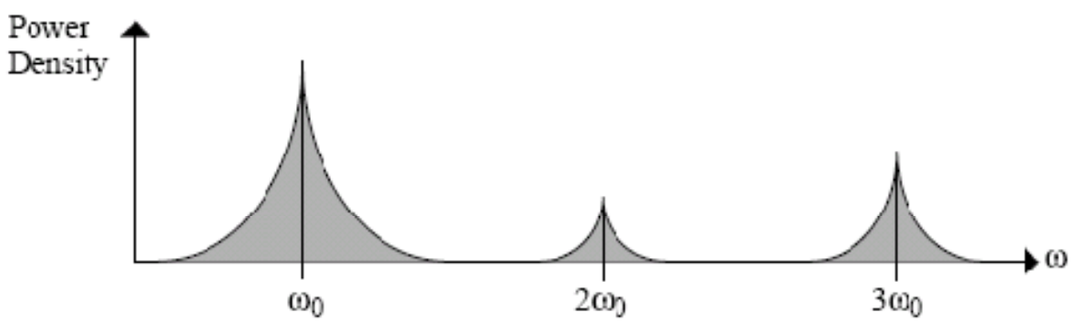


Fig. 3. Practical oscillator spectrum.

An oscillator can usually either be viewed as a single two-port feedback circuit, or as two one-port circuits connected together. Consider the linear feedback model depicted in Figure 4.

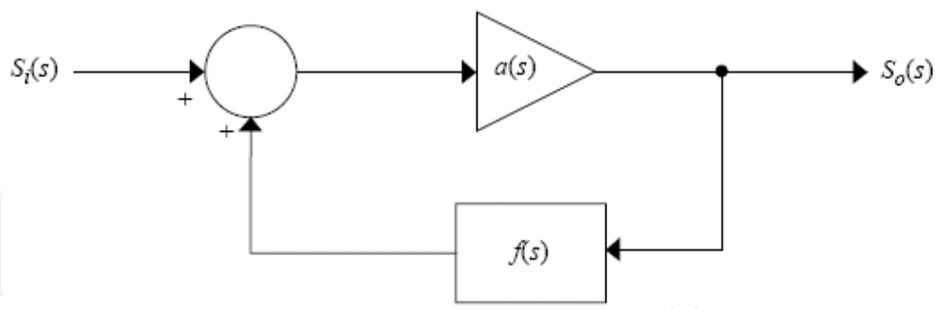


Fig. 4. Basic Oscillator feedback model

The overall transfer function from input to output is given by

$$\frac{S_o(s)}{S_i(s)} = \frac{a(s)}{1 - a(s)f(s)} \tag{1}$$

This system can have a non-zero output without any input as long as the quantity *a(s)f(s)*, i.e. the *loop gain*, is one and the phase shift around the loop is zero.
However, an initial loop gain magnitude greater than one is typically designed and then nonlinearities in the amplifier will reduce the magnitude to exactly one in steady-state operation.
Assuming *a(s)* has zero phase shift, we can implement *f(s)* as a resonator, realized with a parallel *LC* tank, having zero phase shift at the desired oscillation frequency.

Another way to view an oscillator is to break it up into two one-port networks, an active circuit and a resonator, as depicted in Figure 5. When the equivalent parallel resistance R_T of the resonator is exactly balanced by a negative resistance $-R_a$ of the active circuit, the negative resistance compensates the losses in the resonator and steady-state oscillation is achieved.

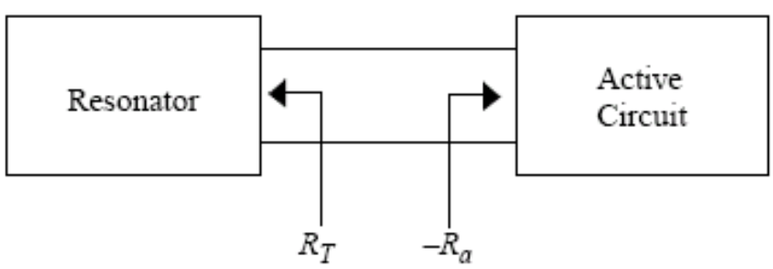


Fig. 5. Two One-port networks view of an oscillator.

1.5.1 One-Port View of Phase Noise

Figure 6 shows an equivalent one-port model of an *LC* oscillator, in which $i_n(\omega)$ denotes all noise sources in the circuit. Suppose the mean square noise current density is $\bar{i}_n^2/\Delta\omega$.

Assuming linear time-invariant behavior, total noise power density $P_n(\omega)/\Delta\omega$ can be calculated as [1]:

$$\frac{P_n(\omega)}{\Delta(\omega)} = \frac{\bar{\imath}_n^2}{\Delta(\omega)} \cdot |Z(\omega)| \tag{2}$$

where, $|Z(\omega)|$ is the tank's magnitude response.

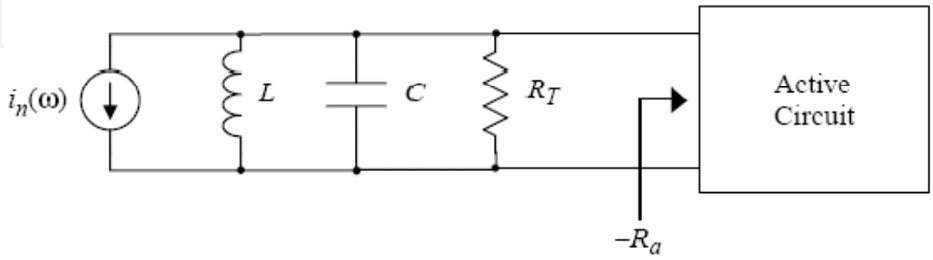


Fig. 6. One-port model of an LC oscillator.

Two ways to decrease phase noise are suggested by (2). First, we should use as few active devices as possible to minimize the number of noise sources in the oscillator. Second, the tank's magnitude response $|Z(\omega)|$ should be made as narrow as possible, i.e. a high quality factor (Q) should be employed for the LC-tank.

1.5.2 Two-Port View of Phase Noise

Returning to the two-port model shown in Figure 4, we now consider *f(s)* to be a parallel RLC tank as shown in Figure 7(a). The magnitude and phase responses of such a network are given in Figure 7 (b). As discussed before, we need zero degrees net phase shift around the feedback loop (any integer multiple of 360 degrees). Since noise sources in the oscillator circuit will cause temporary phase shifts in the feedback loop, the instantaneous oscillation frequency will be changing such that the tank produces a compensating phase shift, keeping the total phase shift around the loop equal to zero. Thus, phase noise can also be viewed as short-term instability in the frequency of oscillation [3].

The phase noise denoted by L{Δω}is defined as

$$L\{\Delta\omega\} = 10.\log\left[\frac{P_{1HZ}(\omega_0 + \Delta\omega)}{P_s}\right] \tag{3}$$

where, $P_{1Hz}(\omega_0 + \Delta\omega)$ represents the single sideband power measured in a 1-Hz bandwidth and located at a frequency offset Δω from the oscillation frequency ω_0. P_s represents the total signal power. A typical plot of L{Δω}is shown in Figure 8. Note the existence of regions of various slopes, as discussed in [1].

As mentioned above, to reduce the phase noise the magnitude response of the tank should be as sharp as possible, i.e. it should have a very narrow bandwidth or simply a high quality factor Q.

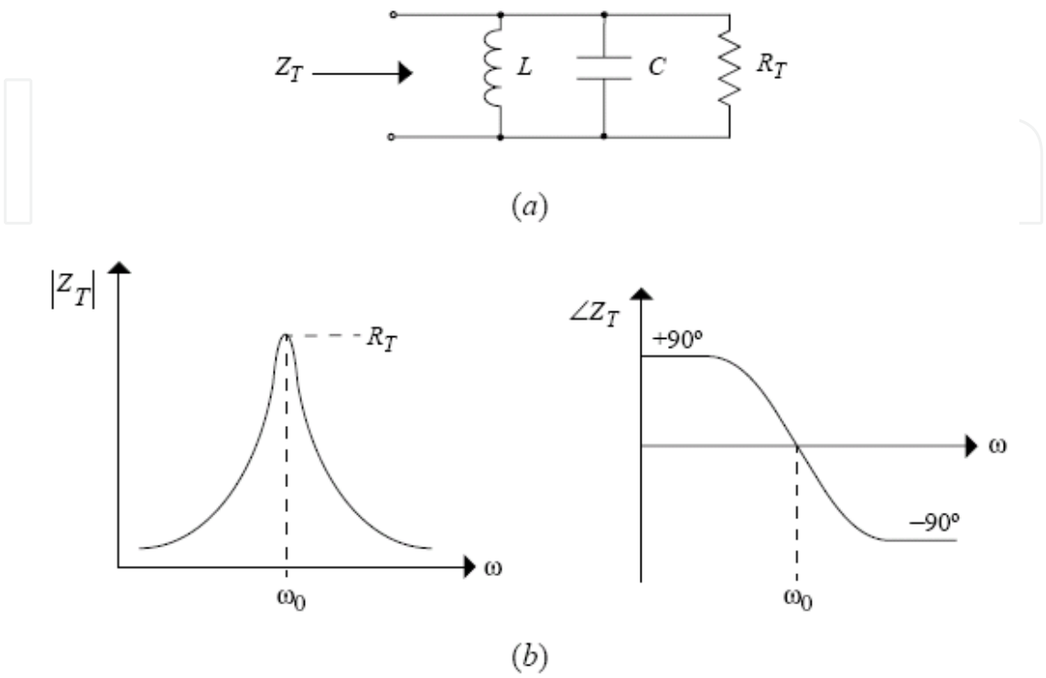


Fig. 7. (*a*) Parallel RLC tank. (*b*) Magnitude and phase response.

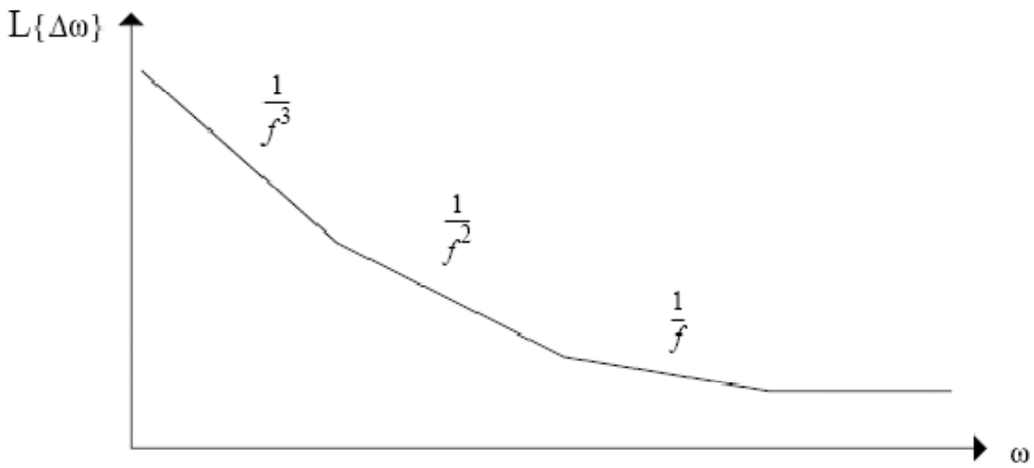


Fig. 8. General appearance of single-sideband phase noise.

I.5 Quality Factor

LC tanks, often referred as *LC* resonators, are represented as series or parallel *RLC* networks, since practical *LC* tanks contain additional resistive components. At resonance frequency, $\omega_0 = 1/\sqrt{LC}$, the tank impedance is purely resistive, and the phase of the impedance

response is exactly zero. At frequencies below (above) resonance, the tank impedance of the parallel RLC network is mainly inductive (capacitive). For series RLC networks, this scenario is exactly opposite.

The resonator's quality factor, Q, is generally defined as:

$$Q = \omega . \frac{Energy\ stored}{Average\ power\ dissipated} \tag{4}$$

The quality factor, which indicates the ability of the tank to retain energy, often determines the phase noise performance of LC VCOs. Also, Q indicates the steepness of the impedance near ω_0 or the sharpness of the peak impedance at ω_0. Therefore, Q can also be described by:

$$Q = \frac{\omega_0}{\Delta\omega_{-3dB}} \tag{5}$$

where, $\Delta\omega_{-3dB}$ is the −3dB bandwidth of the impedance response. Clearly, a larger Q results in a higher rejection of spectral energy away from the resonant frequency, leading to more purity of the oscillator output spectrum.

At resonance, the Q of the RLC networks is given by:

$$Q = \frac{R}{\omega_0 L} = \omega_0 RC \qquad (parallel\ RLC) \tag{6}$$

$$Q = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 RC} \qquad (series\ RLC) \tag{7}$$

where, the dual nature of series and parallel RLC networks is apparent.

In wide-band VCOs, the equivalent tank impedance changes considerably along the tuning range. Figure 9 shows the simulated Q of a standard available on-chip inductor in a 0.18µm CMOS technology [2]. It is observed that the Q is linearly increased with the operation frequency. Aiming for a wideband VCO operating between 3– 6GHz, it is of interest to have the maximum Q at the highest frequencies, since the phase noise increases with frequency and may be reduced with the gain in Q. However, the variations in Q cause unwanted effects on the output amplitude. This issue will be explored in more detail in section 1.7.3.3.

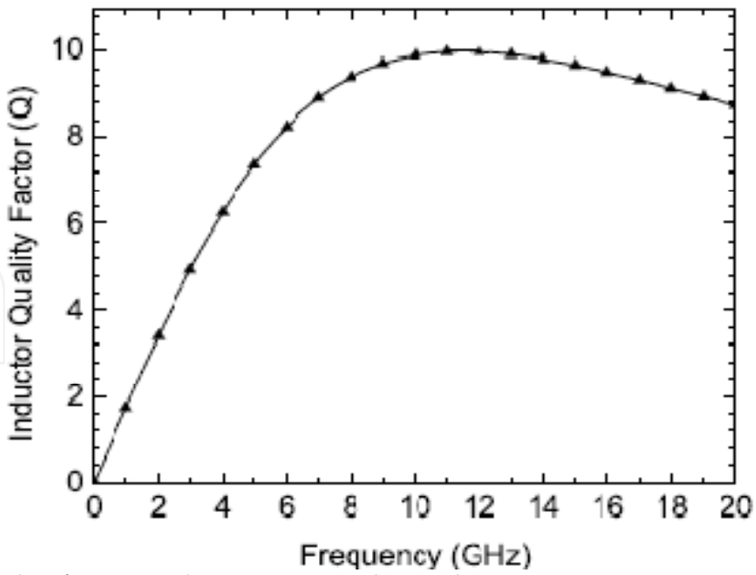


Fig. 9. Simulated Q for a circular 0.45nH on-chip inductor in a 0.18μm CMOS process [2].

1.6 Figure of Merit

Most oscillator designers usually report a figure of merit (FoM) value for their specific design. The most commonly used FoM in the RF community is the power-frequency-tuning-normalized (PFTN) figure of merit (FOM), as defined in [4, 6]:

$$FoM = 10.log\left(\frac{KT}{P}\left(\frac{\omega_{o,max}-\omega_{o,min}}{\Delta\omega}\right)\right) - L\{\Delta\omega\} \quad (8)$$

where, Δω is the frequency offset from the carrier frequency ω_0, P is the power consumed by the VCO core, and L{Δω} is the phase noise measured at an offset Δω from the carrier. Also, $\omega_{0,max}$ and $\omega_{0,min}$ denote the high-side and the low-side frequencies of the tuning range, respectively.

1.7 Layout of Active and Passive Components

In CMOS VCO circuits, finding the optimal layout for both the passive and active devices is critical to achieving the best possible performance. One reason is the increasing impact of the parasitics in the device layout with technology scaling. Therefore, a well-optimized layout, which minimizes the parasitics and the noise sources, is very important. This section is devoted to these issues, including the integration of spiral inductors with high quality factor, active inductors, capacitors, varactor, resistors, and transistors for realizing the ultimate goal of VCO design.

1.7.1 Resistors

Figures of merit for resistors are sheet resistance, tolerance, parasitic capacitance, and voltage and temperature coefficients. In CMOS technology, resistors can be formed from the implanted well, the gate polysilicon, the source/drain active areas, and metal.

Polysilicon resistors are often used in integrated circuits for their low dependence on voltage and temperature. A low-doped p-type polysilicon resistor is used for applications

requiring high resistance. Despite its good parasitic capacitance, this resistor exhibits a 25% tolerance [8]. On the other hand, highly doped p-type polysilicon resistors are preferred in most cases because of their good matching and low parasitic.
Non-salicide high resistance poly has a sheet resistance between 800 - 1200 ohm/square. Non- salicide P+ (N+) poly resistance has a sheet resistance of 280-455 (95-180) ohm/square. These non-salicide poly resistors can be used for high-frequency circuits. Salicide P+/N+ poly resistance has a sheet resistance of 2-15 ohm/square, with small parasitic capacitance.

Diffusion resistors are similar to poly in terms of parasitic capacitance and voltage coefficient. They are typically controlled to a 10% tolerance. Salicide P+/N+ diffusion resistance has a sheet resistance of 2-15 ohm/square, with large parasitic. Non- salicide P+ (N+) diffusion has a sheet resistance of 110 -190 (60 -100) ohm/square. Non-salicide diffusion resistors are only suitable for low-frequency circuits, e.g. they are often used for ESD protection.

Well resistors have a large sheet resistance of 300 to 500 ohm/square, with large parasitic capacitance. Because of their strong dependence on voltage, they are usually used to feed a DC bias voltage.

Another high-performance resistor is formed of a thin metal film, further above the substrate in the wiring levels [9]. It has a sheet resistance of 0.025 to 0.115 ohm/square, with several attractive features such as low tolerance, low variation with voltage, and low parasitic.

1.7.2 Capacitors

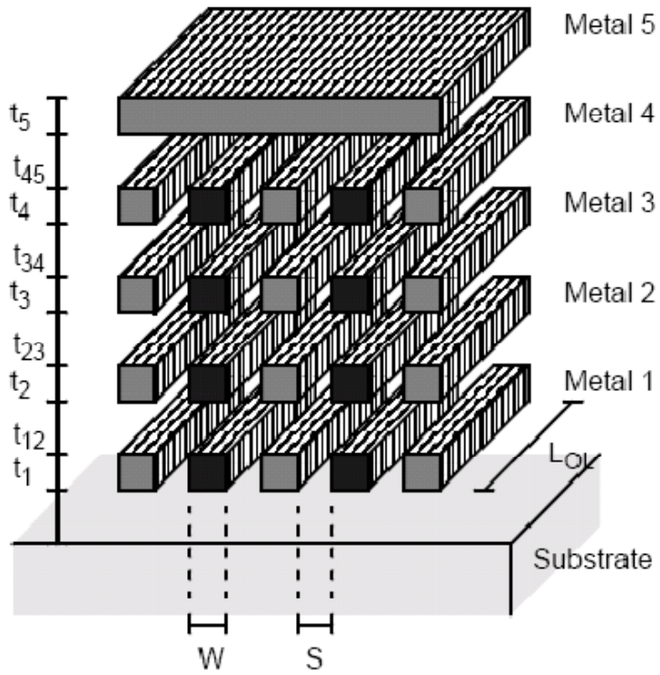


Fig. 10. Four Stacked Lateral Flux Capacitors. Fingers with dark cross-sections are connected to one port. The remaining fingers are connected to the other port [10].

Capacitors can be realized in any IC process using parallel plates from any two different layers (see Figure 10). Much larger capacitance per unit area can be obtained using the polysilicon layer as one or both of the capacitor plates. Nevertheless, a potential problem is that parasitic capacitance from the poly to the substrate may affect the circuit performance.
To achieve large capacitance per unit area, it is common to use several sandwiched-type capacitors and connect them in parallel (Figure 11). In order to obtain two capacitors with a good matching ratio, common-centroid and dummy devices are employed. Matched capacitors should have the same perimeter-area ratio.
Capacitors with relatively high-Q can also be implemented as interdigital, i.e. two conductors on the same plane are terminated in interdigitated fingers. These are used for low capacitance applications (0.05-0.5pF). With more metal layers available in a modern technology, the density of this capacitor tends to improve.

Since polysilicon-based capacitors are lossy, metal-insulator-metal (MIM) capacitors are preferred in RF design. MIM capacitors exhibit high density (e.g. 1-2fF/μm²) by using an ultra-thin layer of silicon nitride sandwiched along with an intermediate metal layer. Their typical Q exceeds 100 at 1GHz, with a relatively low parasitic capacitance (1% or less) [4].
MIM capacitors and Metal finger capacitors can be simply modeled by equivalent series RC networks, where R represents the series loss from the finite resistance of the metal plates.

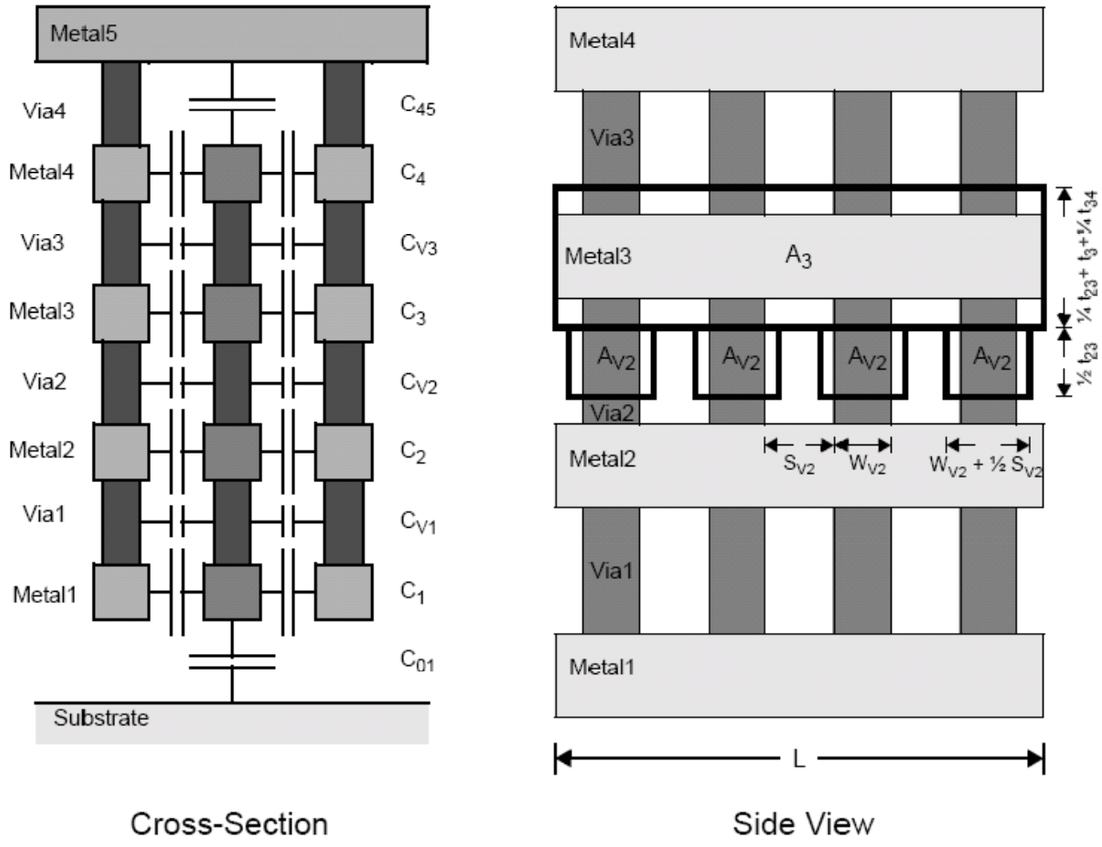


Fig. 11. Cross-Section of a Vertical Mesh Capacitor (left) and side view (right) [10].

1.7.3 Integrated Passive Inductors

On-chip inductor is by far the most critical component in an LC-tank oscillator, since its Q affects the phase noise performance and determines the power dissipation. As the process technology improves and the number of metal layers is increased, the quality (Q) of the passives is generally enhanced. Typical values of a standard on-chip inductor are in the range of a few nH with a Q ranging from 2-10 (for frequencies below 6GHz), depending on the technology and operating frequency [2].
On-chip inductors often need large loops and they have an area inefficient structure, compared to capacitors and resistors. However, planar inductors are widely implemented due to their flat Q and the ease of fabrication in standard processes. Typical on-chip spiral inductor structures are shown in Figure 12, which consist of multiple squares, octagonal, or circular spiraling turns forming its coils [4].

Making an inductor wider decreases the series resistance, and hence has a positive effect on Q at a particular frequency to a certain extent [12]. However, this would increase the coil capacitance and further reduce the resonant frequency. The maximal width of the metal (usually it is about 15-30 μm) is usually established using an optimization for resonance frequency or *Q*-factor.
The spiral is generally implemented in the topmost available metal layer because of its larger thickness than lower metal layers which helps reduce resistive losses. Also due to lower parasitic capacitance to the substrate, top metal layers give rise to higher self-resonance frequency. Note that the use of lower metal layers (closer to the substrate) brings down the self-resonance of the inductor. Sometimes two or more levels are connected in parallel to reduce resistance. Again, this technique effectively brings the coil closer to the substrate, which lowers its self-resonance.
The outer diameter of the inductor depends on how wide the inductor wire is, which in turn determines the area the inductor covers. For a given inductor area, one can fill in more turns until the entire space is occupied. Nevertheless, this is not recommended because of loss constraints and the fact that inner turns only slightly increase the overall inductance. Thus, spiral inductors are rarely filled to their maximum number of turns, and increasing the inductance is typically achieved by increasing the coil radius.

The inductance of a spiral is a complicated function of its geometry, and accurate computations require the use of field solvers. However, an approximate estimate, suitable for quick hand calculations as described in [12], gives the result which may deviate about 30% in comparison with field simulator results.

Square spirals offer the largest inductance per area compared to octagonal or circular spiral, whereas circular spirals is known to provide somewhat higher Q factor. The octagonal spirals are used as the next best alternative [4], since often circular geometries are not supported by many layout tools and not permitted in many technologies.

Another popular technique which provides a much more compact layout is to utilize a differential structure, as shown in Figure 13 [4], instead of using two single-ended inductors. In addition, the differential structure suppresses common- or even-mode capacitive parasitics and associated losses [14]. These benefits can also improve the self-resonance frequency and quality factor.

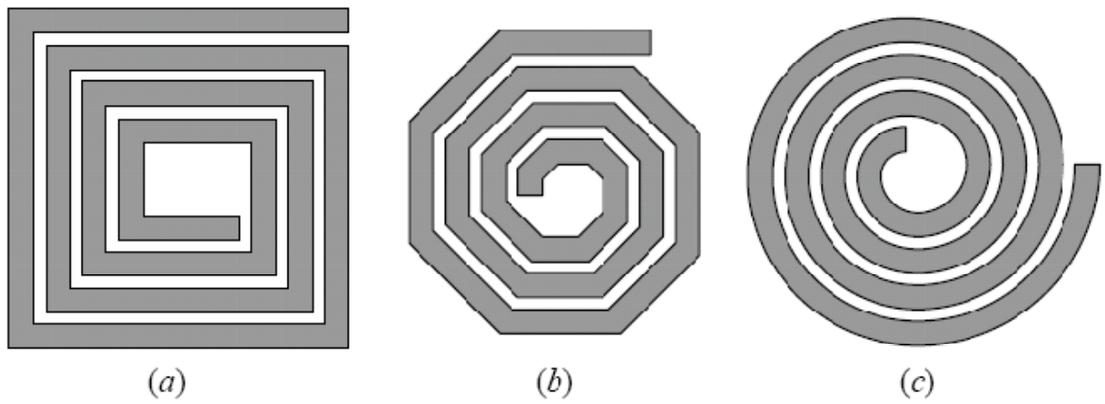


Fig. 12. Typical integrated inductors: (a) square, (b) octagonal, and (c) circular spirals [4].

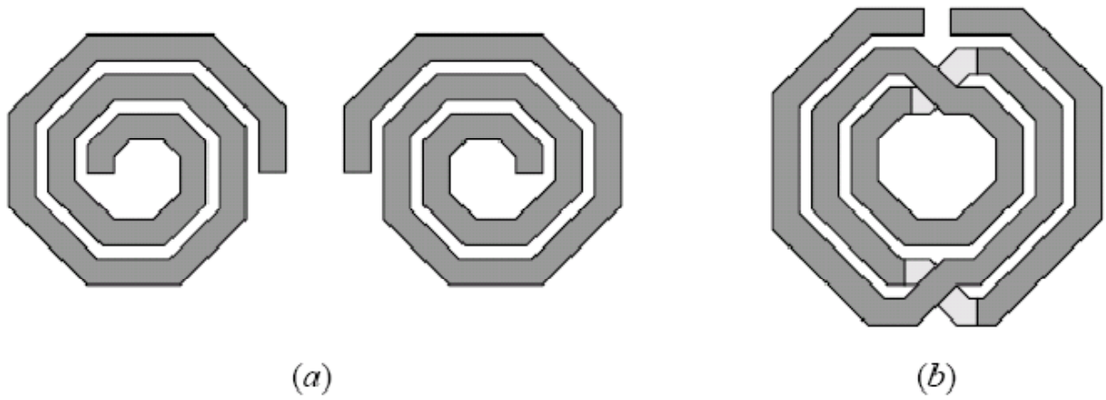


Fig. 13. A pair of single-ended inductors (a) and a differential inductor (b) with similar total inductance [4].

When two or more coils are used on the same chip, the distance between coil centers should be at least two times larger than the coil diameter for each couple of coils.

1.7.3.1 Measures for Q-enhancement

Three technological measures increasing Q are mentioned here. The first measure, which is anticipated to increase Q in two or three times, is using copper (Cu) alloys instead of aluminum (Al) alloys. The second measure is removal of the substrate under the coil (by etching or micromachining). It increases Q in addition by two or three times. The micromachined Cu inductors may have Q's as high as 50, and allow realization of bandpass filters with the insertion loss which is better than –5dB at the frequency about 6GHz.

Third measure is a pattern ground-shield, which has been shown to improve the Q of the inductor, since it reduces the capacitive coupling to the lossy substrate [13]. This technique also reduces the noise coupled from the substrate at the penalty of reduction of the self resonant frequency of the inductor.

Today, such inductors are common in standard available design kits provided by the manufacturers. However, despite these efforts, the inductor Q is still one of the main uncertain parameters in RF circuit design and in many cases the major bottleneck of entire systems.

1.7.3.2 Inductor Modeling

The area of an on-chip inductor can span up to hundreds of μm across and does not scale down with the technology [2]. Aside from their large physical dimensions, integrated inductors are usually described by simple lumped equivalent networks.

Figure 14 (a) shows a lumped π-model for an integrated inductor. L_s describes the series inductance and R_s represents the series resistance of the metal layer. C_p models the interwinding capacitance between the traces. In silicon technology the fairly conductive substrate is close to the spiral, which is essentially creating a parallel plate capacitor (C_{ox}) that resonates with the inductor. R_{sub} model the resistive path in the substrate which also reduces the Q of the inductor. C_{sub} models the capacitive coupling from metal to substrate which reduces the resonant frequency of the inductor.

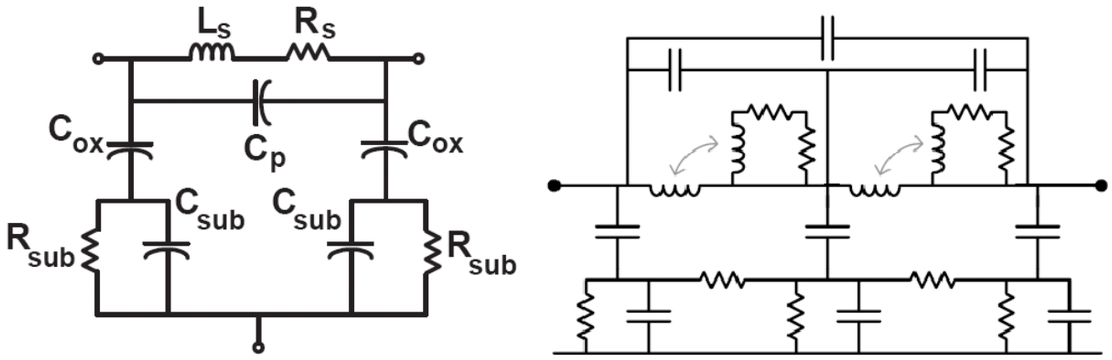


Fig. 14. (a) Basic π-model of an integrated inductor (b) wideband lumped equivalent.

The π-equivalent network is a narrowband model only valid in the close vicinity of that particular frequency and is not suitable in wideband designs [4].

The network shown in Figure 14 (b) approximates the frequency dependence of the most important characteristics of the coil using an expanded lumped equivalent network. As a result, its validity holds over a much wider frequency range and it is better suited for wideband design analysis [4].

1.7.3.3 Effect of frequency

The Q value of ideal inductors is improved with the increase in frequency. This is however not the case for on-chip inductors because the parasitic capacitance and substrate losses show their significance at higher frequencies [12].

The series dc resistance of the inductor is the dominant loss contributor at low frequencies (<1GHz). At higher frequencies, the series resistance rises considerably, due to skin and proximity effects. The skin effect forces the current in the inductor to flow on the outside of the spiral. This makes the inner turns of the spiral less effective than the outer turns and the effective series resistance is increased.

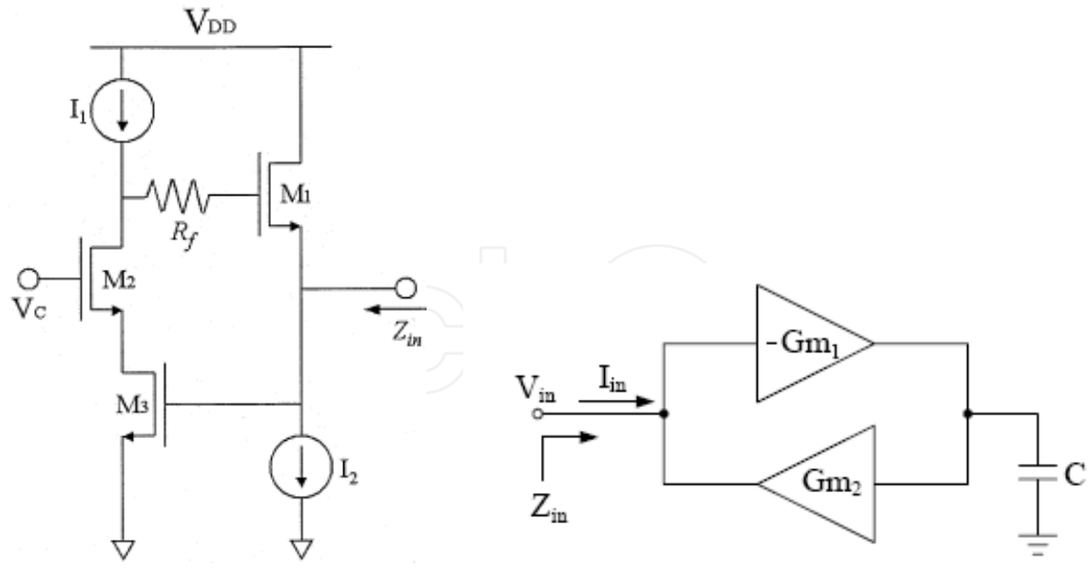
Proximity effects due to fields from adjacent turns result in a similar frequency-dependent non-uniform current distribution and corresponding loss increase. Also, the flow of currents in the substrate translates to additional losses which are a strong function of the substrate resistivity and become significant as frequency increases.

As a result, Q initially rises linearly with frequency since the loss is dominated by the coil's dc series resistance. Eventually, skin and proximity effects as well as substrate losses become dominant. Thus, Q gradually peaks to a maximal value, and beyond which it experiences a fast decline as frequency approaches the coil's self-resonance. Note that the impact of the above effects on the inductor performance is very complicated, and therefore, software tools must be used for its performance optimization.

1.7.4 Active Inductor Design

Active inductors may often be of interest in RF circuits, since passive inductors are not economical in terms of the fabrication technology and die area. An active inductor can be realized by connecting two transconductors with resistive feedback (R_f), as shown in Figure 15 (a) [15-18]. This realization is based on the gyrator-C topology (Figure 15(b)). In Figure 15(a), transistor M2 is employed to reduce the output conductance (g_{ds}), as a result of which the inductance, quality factor, and frequency tuning range are improved. Also, the feedback resistance R_f between M_1 and M_3 significantly increases the inductance [16]. The resistance (R_f) is usually implemented by a passive poly layer.

Due to low-inductance value and narrow frequency range of the above topology, improved cascode structure employing active resistors in the feedback line is also proposed [19]. The fully tunable active inductor (TAI) and its equivalent circuit model are shown in Figure 16(a) and Figure 16(b), respectively. This active inductor exploits a tunable feedback resistance, implemented by connecting the resistor (R_f) in parallel with a transistor. The gate-source voltage (V_{tune}) in this transistor controls the total effective resistance (R_{eff}). This reduces the output conductance and improves the quality factor.



(a) (b)

Fig. 15. (a) Schematic of cascode-grounded active inductor with a feedback resistance (b) Gyrator topology

The equivalent capacitance, inductance, and resistors are [19]:

$$C_{eq} = C_{gs3} \tag{9}$$

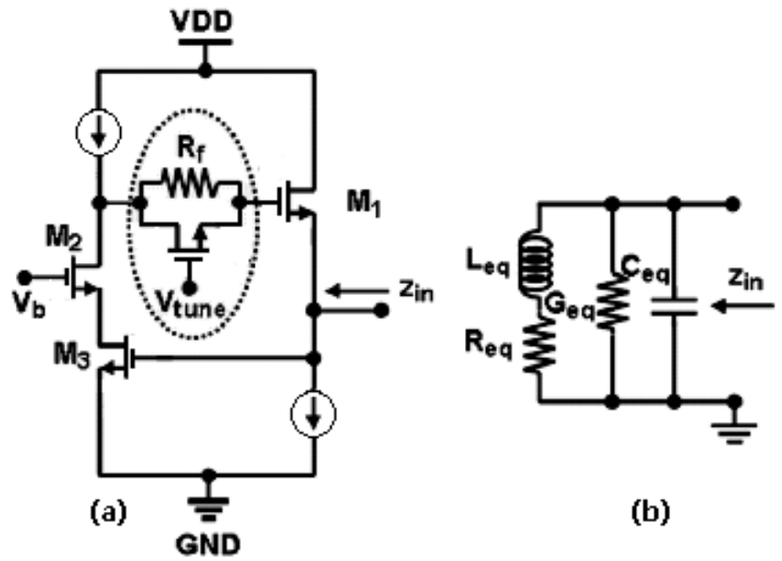


Fig. 16. (a) TAI topology (b) Equivalent circuit model of active inductor

$$L_{eq} = \frac{g_{m1}g_{m2}C_{gs1} + \omega^2 C_{gs1}^2 C_{gs2}(R_f g_{ds2} + 1)}{g_{m1}^2 g_{m3} g_{m3} + \omega^2 g_{m2} g_{m3} C_{gs1}^2} \tag{10}$$

$$R_{eq} = \frac{g_{m1}g_{ds2}g_{ds3} + \omega^2\left[g_{m2}C_{gs1}^2 - g_{m1}C_{gs1}C_{gs2}(R_f g_{ds2} + 1)\right]}{g_{m1}^2 g_{m2} g_{m3} + \omega^2 g_{m2} g_{m3} C_{gs1}^2} \tag{11}$$

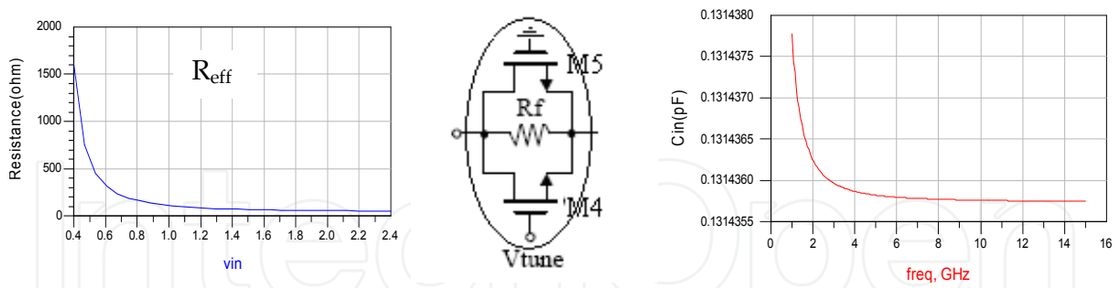
$$G_{eq} = \frac{2g_{ds2} + R_f g_{ds2}^2}{R_f g_{ds2} + 1} \tag{12}$$

In (12), the effect of feedback resistor is shown by $(R_f g_{ds2} + 1)$, which is designed for a value greater than unity. Decreasing R_{eq} by the help of R_f results in an increase in L_{eq}. The quality factor and the input impedance of TAI can be obtained from [15]:

$$Q = \left(\frac{\omega L_{eq}}{R_{eq}} \right) \left[\frac{1 - (R_{eq}^2 C_{eq}/L_{eq}) - \omega^2 L_{eq} C_{eq}}{1 + R_{eq} G_{eq} \{1 + (\omega L_{eq}/R_{eq})^2\}} \right] \quad (13)$$

$$z_{in} = \left[\frac{R_{eq} + j\omega L_{eq}}{(1 + R_{eq} G_{eq} - \omega^2 L_{eq} C_{eq}) + j\omega (R_{eq} C_{eq} + L_{eq} G_{eq})} \right] \quad (14)$$

Clearly, with decreasing R_{eq}, the quality factor is improved.
Note that in conventional TAI topology, V_b=constant (see Figure 16 (a)). As can be seen from equations (10), (11), and (13), active resistor has direct effect on increasing L_{eq} and R_{eq}. However, this increase in R_{eq} will degrade the quality factor. To overcome this problem, V_b can be utilized as the extra tuning voltage to control the g_{ds} of transistor M2. Thus, the required inductance and quality factor are achieved by controlling V_{tune} and V_b simultaneously.
For further enhancement of quality factor and inductance, one can utilize the transistor M5 in parallel with feedback resistance R_f, as shown in Figure 17(b) [18]. This transistor, which operates in the cut-off region, exhibits a frequency dependent capacitance as shown in Figure 17(c).
Using a 0.13μm CMOS technology, a tunable resistance from 100Ω to 1.6 kΩ may be achieved [18] for V_{tune}=1.2V to V_{tune}=0.4V, as illustrated in Figure 17(a).



(a) (b) (c)

Fig. 17. (a) Variation of effective resistance versus tuning voltages (b) Proposed active resistance with parallel MOSFET (c) Variation of capacitance in proposed active resistance versus frequency.

The values of each component of equivalent circuit model are expressed below (Cp is equivalent capacitance of M5):

$$C_{eq} = C_{gs3} - \frac{2\omega C_p R_{eff} g_{ds2} \left(R_{eff} g_{ds2} + 1\right) - R_{eff} \omega C_p \left(R_{eff} g_{ds2}^2 + 2 g_{ds2}\right)}{\left(R_{eff} g_{ds2} + 1\right)^2 + \omega^2 C_p^2 R_{eff}^2} \quad (15)$$

$$G_{eq} = \frac{2\omega^2 C_p{}^2 R_{eff}{}^2 g_{ds2} + \left(R_{eff} g_{ds2} + 1\right)\left(R_{eff} g_{ds2}{}^2 + 2g_{ds2}\right)}{\left(R_{eff} g_{ds2} + 1\right)^2 + \omega^2 C_p{}^2 R_{eff}{}^2} \tag{16}$$

$$R_{eq} = \frac{g_{m1}g_{ds2}g_{ds3} + \omega^2\left[g_{m2}C_{gs1}{}^2 + \left(C_{gs1}C_{gs2}\right)\left[\frac{g_{m1}C_pC_{gs1}R_{eff}{}^2 g_{ds2}}{1+\omega^2 C_p{}^2 R_{eff}{}^2} - g_{m1}\left(1+\frac{R_{eff}g_{ds2}}{1+\omega^2 C_p{}^2 R_{eff}{}^2}\right)\right]\right]}{g_{m1}{}^2 g_{m2}g_{m3} + \omega^2 g_{m2}g_{m3}C_{gs1}{}^2} \tag{17}$$

$$L_{eq} = \frac{g_{m1}g_{m2}C_{gs1} + \omega^2\left(C_{gs1}C_{gs2}\right)\left[\frac{g_{m1}C_pR_{eff}{}^2 g_{ds2}}{1+\omega^2 C_p{}^2 R_{eff}{}^2} + g_{m1}C_{gs1}\left(1+\frac{R_{eff}g_{ds2}}{1+\omega^2 C_p{}^2 R_{eff}{}^2}\right)\right]}{g_{m1}{}^2 g_{m2}g_{m3} + \omega^2 g_{m2}g_{m3}C_{gs1}{}^2} \tag{18}$$

In order to have L_{eq} greater and R_{eq} smaller than other conventional inductors, the following relations should be satisfied.

$$C_p > \frac{-g_{ds2}}{\omega^2 C_{gs1}} \tag{19}$$

$$C_p > \frac{C_{gs1}g_{ds2}}{\omega^2} \tag{20}$$

1.7.5 Varactors

Varactors are essential elements of voltage-controlled oscillators (VCOs). The key figures of merit for varactors are tunability (C_{max}/C_{min}), CV linearity for VCO gain variation, quality factor *Q*, tolerance, and capacitance density [8].

In general, two types of varactors have been developed for the RF CMOS processes, MOS accumulation mode capacitor (MOS varactor) and CMOS diode.

CMOS diode varactors are basically reverse-biased p-n junctions which can be implemented using the available p+/n-diffusions and n- or p-wells [4]. These varactors exhibit tunability of about 1.7:1 over a 3-V range, and can be used where fine tuning of capacitance is required. Also, they provide better linearity than MOS varactors.

The MOS varactor can be realized with an *n*-channel MOSFET fabricated in an n-well. Its main advantage is the high intrinsic C_{max}/C_{min} that is much higher than that of p-n junction varactors. This provides an excellent tunability over a wide frequency range and sufficiently high Q factor. The performance of this varactor improves with technology scaling.

Also, a hyper-abrupt (HA) junction varactor has been reported in the literature with a nearly linear *C*–*V* tuning ratio of 3.1 and a *Q* exceeding 100 at 2 GHz [8].

It should be mentioned that amplitude variations in wideband VCOs may reduce the varactor's capacitive range (C_{max}/C_{min}) and the associated reduction in the overall tuning sensitivity [7].

1.7.6 Transistors

The optimum layout design and biasing of transistors for a voltage-controlled oscillator (VCO) is very essential, since the purity of its output spectral signal is extremely sensitive to device noise. With the reduction in supply voltage, which scales with the transistor features in CMOS technologies, this becomes challenging because of the inherent device noise increase. The appropriate condition for oscillation, for the minimum expected bias current with a reasonable safety margin under worst-case conditions, is set by proper transistor sizing. Moreover, biasing of the transistors, which is anticipated to put an oscillator on the verge of the current-limited and voltage-limited regimes, is critical to achieving the best possible performance.

1.7.6.1 Biasing

Once a MOSFET is biased near characteristic current density [20], e.g. around 0.15mA/μm for n-type transistor, the transistor exhibits a minimum noise figure NF_{MIN}. Interestingly, this property remains invariant over technology nodes, foundries, MOSFET cascodes, as well as the type of transistor. Therefore, it is reasonably expected that circuit topologies realized with combinations of n-type and p-type MOSFETs will behave similarly.

In low noise amplifier (LNA) design, it is often attractive to bias the transistor below the characteristic current density (e.g. about 50% [21]) due to negligible influence on its noise performance and in favorite of reducing the power consumption. It should be noted that in general, the circuit topology in LNA majorly impacts its total noise performance. In other words, when the device NF is minimized, the total noise of the amplifier may not be at the lowest level since the NF concept of device is not necessarily the appropriate indicator for optimizing LNA noise performance. In particular, when NF <3dB, the noise in the circuit is dominated by the thermal noise of the driving source, and reducing the noise of the device cannot have a significant impact on NF. In fact, for optimizing the noise performance in this case, the total noise level and/or signal-noise ratio are more useful.

In VCO, the mechanism of noise to phase noise conversion is very complicated. Since the phase noise is inversely proportional to the power dissipated in the resistive part of the resonant LC tank, the (tail) current through the VCO is set large enough to maximize the voltage swing at the tank. As long as the tail current is below this current level, VCO operates in the current-limited regime. Raising the tail current will cause the VCO to enter in the voltage-limited regime. In this case, further increase of the tail current will increase the phase noise. Based on the author's experience, in the current-limited regime the best phase noise performance is achieved by biasing far below the characteristic current density (e.g., 30% to 50% of this current).

1.7.6.2 Finger Layout

Given the geometry of CMOS devices in oscillator, a multifinger gate structure is the most popular approach to adopt in the layout design. The different gate layout splits induce

different parasitic resistance, and the lower noise characteristics result in a lower VCO phase noise performance. When two devices share the same gate length, total gate width, and process, the flicker noise should be similar based on the intrinsic device operation. However, as shown in [22] the parasitic resistances will also contribute to flicker noise.

Thus, reducing the gate width and increasing the finger number in the design of gate configuration can enhance the device noise performance, as long as the gate resistance is decreased [22]. Once the layout structure is determined, the number of contact on the gate is also important. Beside, the design of double-sided gate contacts (two contact holes in both ends of the gate finger) can be utilized to further decrease the resistance.

1.7.6.3 Number of Contacts

Generally speaking, at the expense of increased parasitic capacitance, the more the gate contacts are added, the lower will be the gate resistance. The gate resistances for single-sided and double-sided contacts are given by Equations 21 and 22, respectively [9].

$$R_G = \frac{\frac{R_{CON}}{N_{CON}} + \frac{R_{sq}}{L} / \left[W_{ext} + \frac{W_f}{3} \right]}{N_f} \tag{21}$$

$$R_G = \frac{\frac{R_{CON}}{N_{CON}} + \frac{R_{sq}}{L} \left[W_{ext} + \frac{W_f}{6} \right]}{2N_f} \tag{22}$$

where, R_{CON} is the contact resistance, N_{CON} the number of contacts per gate finger, R_{sq} the gate poly sheet resistance per square, W_{ext} the gate extension beyond the active region, W_f the finger width, N_f the number of gate fingers connected in parallel, and l_{phys} the physical gate length. As a rule of thumb, for the technologies between 180 to 90nm, the optimum finger width appears to be from 1-2μm.

1.7.6.4 Experimental Tests

The 2μm × 36 fingers and 8μm × 9 fingers transistors have been used as a MOS varactor individually in the design of a VCO circuit [22] in a 0.13μm CMOS technology. In both VCO circuits, the rest of the MOS transistors use the same 2μm × 36 fingers gate layout, in order to provide the best noise performance.

The VCO phase noise at 100 kHz offset is as low as -97 and -91 dBc/Hz of 2μm ×36 fingers and 8μm ×9 fingers varactors at 5.2 GHz, respectively, where the dc current is 5 mA at a 1.5-V supply. At 1MHz offset, the respective phase noise is -115 dBc/Hz and -111 dBc//Hz. Thus, the VCO performance is extremely sensitive to device layout. That is because the contribution to the overall noise of the resistance of the gate in an MOSFET is highly layout dependent.
Note that the current density is 0.069mA/μm which is used for the best performance of the VCO [22]. This once again indicates that the transistor biasing in VCO is significantly below characteristic current density.

1.8 Design Considerations for Wideband LC-VCOs

In narrow-band applications, the resonator of the VCO is usually optimized to achieve a maximum Q at the desired operation frequency. This is possible within a limited tuning range, since the transconductance cell can be optimized for a given oscillation amplitude and power dissipation.

In a wide-band design, however, this is not straightforward due to performance variations over the frequency range, e.g. the VCO loop gain, the oscillation amplitude, and the phase noise vary considerably from the low-side to the high-side of the tuning range. In this section, the main design challenges and differences between wide-band and narrow-band VCOs are discussed.

1.8.1 Fundamental Start-Up Constraint

In an LC-VCO, the equivalent parallel tank impedance at resonance R_T is a strong function of the oscillation frequency ω_0 and inductance L, and is given by [4]:

$$R_T(\omega_o) = Q_T.\omega_o.L = \frac{(\omega_o L)^2}{r_s} \tag{23}$$

where, the overall tank quality factor Q_T is assumed to be dominated by inductor losses characterized here by the physical series resistance r_s of the coil, which eventually becomes a function of frequency due to skin/proximity effects and substrate eddy current induced losses. The above equation is valid as long as the capacitive elements of the tank have a significantly higher Q than the inductor, which may not hold true at very high frequencies.

In any oscillator, the most fundamental design criterion consists of satisfying start-up conditions. In tunable *LC* oscillators, these conditions are themselves a function of frequency [5]. For the generic *LC* oscillator shown in Figure 18, such conditions are satisfied if the pair of complex conjugate poles of the small-signal (initial) loop-gain transfer function lie in the RHP, which occurs when the magnitude of the loop-gain is greater than unity

$$g_m \geq \frac{1}{R_T} = \frac{r_s}{(\omega_o L)^2} \tag{24}$$

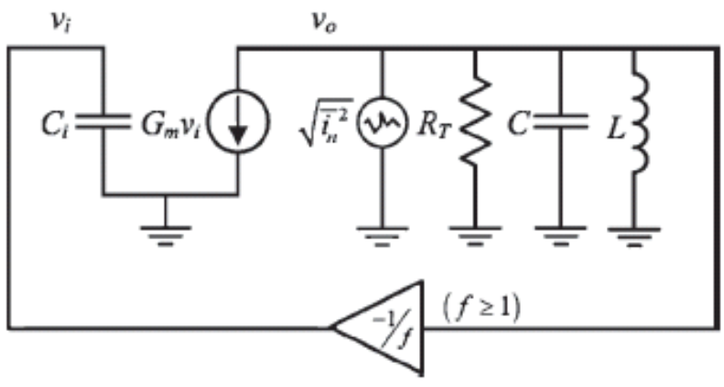


Fig. 18. Generic *LC* oscillator.

Equation (24) indicates a fundamental lower limit on the current consumption for a given transconductor and *LC* tank configuration. In practice, the small-signal transconductance g_m is set to a value that guarantees startup with a reasonable safety margin under worst-case conditions, i.e. at the low-end of the desired frequency range. Thus, wideband VCOs using transconductors fixed at a predetermined critical value feature significant excess of g_m in the upper portion of their frequency range. Raising g_m above this level generally contributes more noise.

1.8.2 Impact of Oscillation Amplitude Variations

As bias current is increased, the VCO's output voltage amplitude also keeps rising. However, the drain cannot exceed the power supply voltage by more than about 0.6 volts before the drain-well diode is turned on, resulting in clipping of the output voltage. As a result, bias current is usually limited by the process.

For the widely used differential cross-coupled *LC* oscillator shown in Figure 19, two such regimes can be identified [6]. In the current-limited regime, the current I_B from the tail current source is periodically commutated between the left and right sides of the tank.

Thus, the resulting fundamental amplitude is directly proportional to I_B and R_T, whereas higher harmonics of the commutated current are attenuated by the bandpass profile of the *LC* tank.

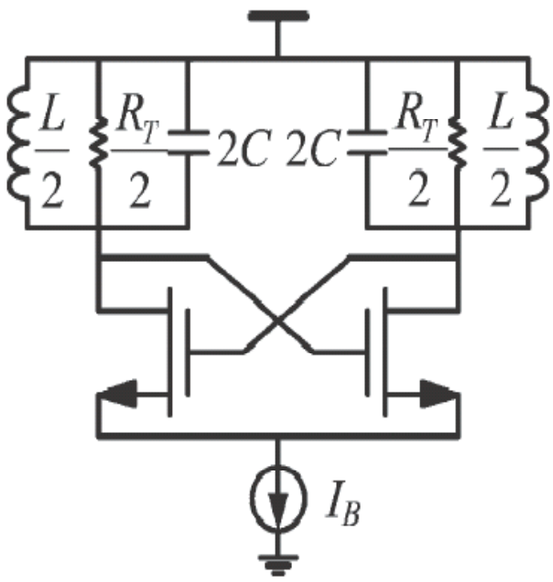


Fig. 19. Differential cross-coupled *LC* oscillator.

As I_B is increased from its minimum value, satisfying start-up conditions, the tank amplitude increases linearly. Eventually, the amplitude saturates by the available headroom from the supply voltage. These two regimes are illustrated in Figure 20(a) [7]. Operating an oscillator in the voltage limited regime is generally undesirable because raising the current will not cause the swing to grow any more, increasing the phase noise [6].

In wideband VCOs, large changes in R_T with frequency can also cause a transition from the current-limited to the voltage-limited regime as frequency increases. Thus, I_B should be reduced as frequency increases in order to prevent such a transition from occurring, otherwise power is wasted.

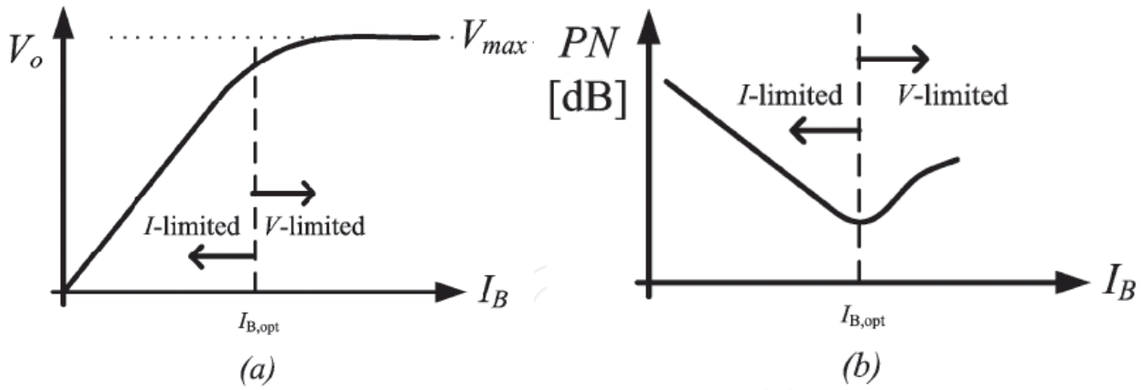


Fig. 20. (a) Steady-state oscillator amplitude versus I_B trend and (b) phase noise versus I_B trend, indicating current- and voltage-limited regimes [7].

1.9 Phase Noise in Wideband Oscillators

To illustrate the impact of oscillation amplitude variations on phase noise, we consider the simplified case of a generic linear time-invariant *LC* oscillator with an equivalent noise generator i_n across its tank, as shown in Figure 18. Solving for the noise to signal power ratio gives [7]:

$$PN \approx \frac{\bar{\imath}_n^2}{V_o^2} \cdot \frac{R_T^2}{4Q_T^2} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \propto \frac{(\eta . g_m + 1/R_T)}{V_o^2} \cdot \frac{R_T^2}{Q_T^2} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \tag{25}$$

where, $(\eta.g_m+1/R_T)$ has been substituted, implying that noise generators from the energy-restoring transconductor and from the tank loss dominate, as is often the case. V_o is the tank amplitude and $\Delta\omega$ is the frequency offset from the carrier. η is an excess noise factor, which appears to be 2/3 for long-channel devices.
In the current limited regime, (25) can be rewritten as follows [7]:

$$PN \propto \frac{(\eta . g_m + 1/R_T)}{I_B^2} \cdot \frac{1}{Q_T^2} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \tag{26}$$

For narrowband designs, R_T does not vary appreciably over the tuning range and the phase noise shows a $1/(Q_T^3 L)$ dependence. Clearly, there is a direct relationship between bias current and phase noise, which provides the designer with a convenient way to trade power for noise performance.

In the voltage-limited regime, (25) can be rewritten as follows:

$$PN \propto \frac{(\eta . g_m + 1/R_T')}{V_{max}^2} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \tag{27}$$

where $R'_T<R_T$ due to the excessive signal amplitude bringing the transconductor into its resistive region, which degrades the overall tank quality factor Q_T. In a narrowband design where the voltage-limited regime is reached by increasing I_B, (27) indicates that the phase noise must degrade since the amplitude saturates to V_{max} while the transconductor noise keeps rising.
Figure 20(b) shows a typical scenario of PN versus I_B. The boundary between the two regimes of operation represents the optimum point for achieving lowest phase noise. Increasing I_B beyond this point degrades the performance in terms of both phase noise and power.
While the above observations yield important insights for narrowband designs, frequency dependences must be taken into account in order to assess similar characteristics for wideband VCOs. Here, we restrict the analysis to the current-limited regime since it is the preferred region of operation. Again starting from (25), a phase noise expression highlighting its frequency dependence is derived assuming a fixed current I_B and $V_o \propto I_B \,.\, R_T$.

$$PN(\omega_o) \propto \left[\eta.\, g_m + \frac{r_s}{(\omega_o L)^2}\right].\left(\frac{r_s}{L.\, I_B}\right)^2 \tag{28}$$

Equation (28) reveals that the phase noise tends to improve as frequency increases. Even in cases where r_s grows linearly with frequency, Eq. (28) shows that phase noise is relatively constant with frequency. The reason why phase noise does not degrade with its classical ω_o^2 dependence is that the tank amplitude in this particular topology basically grows with ω_o^2.

However, (28) only applies in the current-limited regime. Wideband designs operated with fixed I_B experience significant amplitude growth as frequency increases, which eventually brings the VCO into the voltage-limited regime where phase noise will degrade. Furthermore, the optimal point for lowest phase noise indicated in Figure 20(b) cannot be held across frequency.

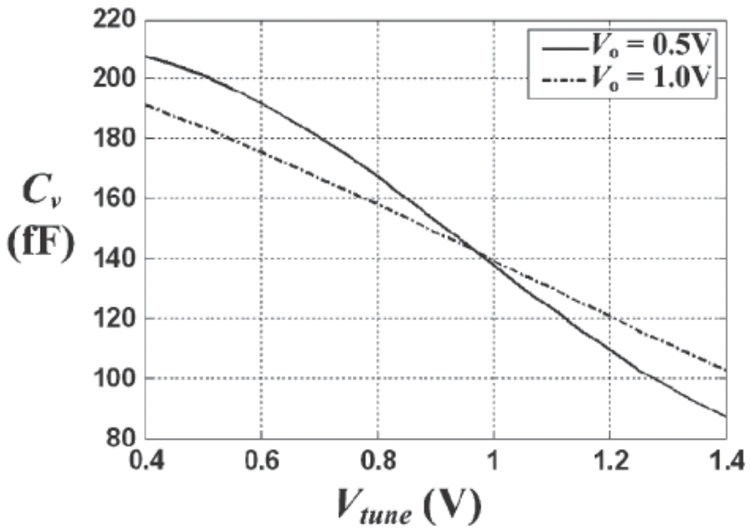


Fig. 21. Periodic-steady state simulation of varactor capacitance versus V_{tune} for two different tank amplitudes [7].

Amplitude variations in wideband VCOs cause several additional second order effects. One such effect is the reduction of the varactor's capacitive range and the associated reduction in the overall tuning sensitivity. Figure 21 shows a typical MOS varactor - curve for different values of oscillation amplitude.
Amplitude variations in wideband VCOs cause variations in the phase noise performance over frequency. Thus, providing a way to control the dependence of oscillation amplitude on frequency is highly desirable.

1.10 Wideband Oscillators

Wide tuning range in the VCO can be obtained by employing a parallel combination of switched binary weighted capacitors and a MOS varactor. However, the VCO loop gain varies considerably over the wide tuning range. Also, the sensitivity of the Q of inductors to operation frequency and varactor nonlinearities and its Q variations cause significant deterioration in phase noise and amplitude variations. These issues complicates the design of wideband (or ultra wideband) VCOs. The objectives of the following sections are to address these issues and provide some guidelines for (ultra) wideband VCO design.

1.10.1 Wideband Tuning

Narrow band *LC*-VCOs have been implemented with optimized performance in the past, since the negative transconductor (g_m) cell can be well designed for a given Q, phase noise, and power consumption. This is due to the fact that in narrow-band VCO the tank Q remains approximately constant over the tuning range. However, the design of (Ultra) Wideband VCOs, e.g. operating between 3–6GHz, is complicated as the equivalent tank impedance at resonance changes considerably along the tuning range. The variations in Q change the output amplitude, as well as the g_m of the transconductor cell, and hence the startup safety margin may not be sufficient over the entire frequency range. Additionally, due to the absence of high and flat Q inductors, the phase noise increases with frequency.

This section gives an overview of various tuning techniques along with the implemented tuning range reported in the literature. Then, it discusses the techniques and issues associated with the design of Ultra Wideband VCOs. Finally, the techniques for phase noise reduction are presented.

1.10.1.1 Tuning with Wieghted Array capacitors

Because the oscillation frequency in an LC-VCO is determined by the tank's resonant frequency, $\omega_0 = 1/\sqrt{LC}$, the tank capacitance may be tuned to adjust the frequency of oscillation. This may be achieved by connecting some combination of MOS capacitors, selected by RF-switches from a weighted array, across a fixed inductor. Each capacitor may be tuned continuously with an analog voltage, and together the array defines the desired piecewise voltage-to-frequency characteristic [23]. In order not to degrade the capacitor Q, the switch must be designed large enough. Consequently, the parasitics associated with the switch may now load the capacitor array when the switch is OFF. This limits the possible tuning frequency.

To alleviate the above problem, the RF switch may be designed using an array of doughnut-shaped sub-FETs, whose gate encloses the drain junction [23]. With this layout, the drain junction capacitance is 20% lower than in a conventional interdigitated FET. The measured tuning range with this array of switched capacitors [23] appears to be 1.34 GHz ±6%. Also, the phase noise remains almost invariant when the RF switch is fully ON or OFF, indicating that the switch resistance does not degrade resonator Q. However, during the switch transition time, the capacitor Q is severely reduced and the phase noise is degraded by 12 dB.

1.10.1.2 Tuning with Inversion mode MOS Varactor

Accumulation MOS (AMOS) varactors cannot achieve their physical maximum and minimum capacitance when the tuning voltage is lower than 1V. For this reason, inversion mode MOS (IMOS) varactors, which provide abrupt gradient of capacitance-voltage curve, can be used for VCO tuning with a low supply voltage [24]. In order to improve the tuning capability further, each IMOS varactor may employ a large resistance in its bulk, isolating the gate to bulk parasitic capacitance of IMOS from the VCO output port. This varactor provides approximately 25% improvement in C_{max}/C_{min} ratio.

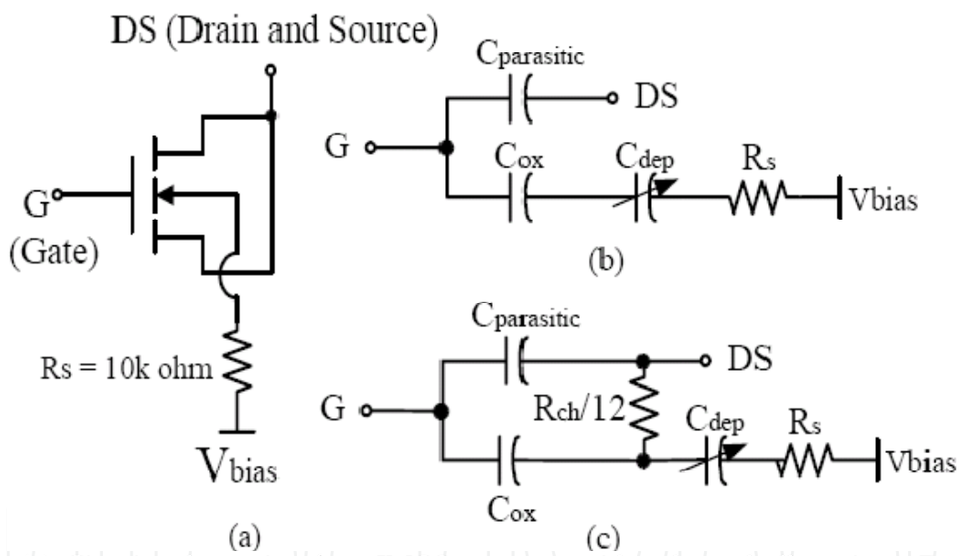


Fig. 22. (a) Circuit schematic of an IMOS varactor with a large bulk resistor Rs (b) The equivalent model in depletion mode (c) The equivalent model in inversion mode [24].

Figure 22 shows the circuit schematic and equivalent models of the IMOS varactors used in the VCO design [24]. In this figure, a large poly resistance Rs (e.g.10kΩ) connects the bulk of the NMOS and the ac ground terminal V_{bias}. When the terminal DS in Figure 22(a) is biased at the positive end voltage, the IMOS is operated in the depletion mode and Figure 22(b) shows the equivalent model. The value of $C_{parasitic}$ is dominated by the gate-source and gate-drain overlap capacitance; C_{ox} is the gate-oxide capacitance and C_{dep} is the depletion capacitance.

However, if the bulk is connected directly to the ac ground, C_{min} will become ($C_{parasitic} + C_{ox} \| C_{dep}$). Thus, C_{min} can be decreased by ($C_{ox} \| C_{dep}$) by using a large resistance R_s in

Figure 22(a). When DS is biased at the negative end, a sheet of electrons accumulates at the surface of the channel and the IMOS is operated in the inversion mode. Figure 22(c) shows the equivalent model. R_{ch} is the channel resistance.

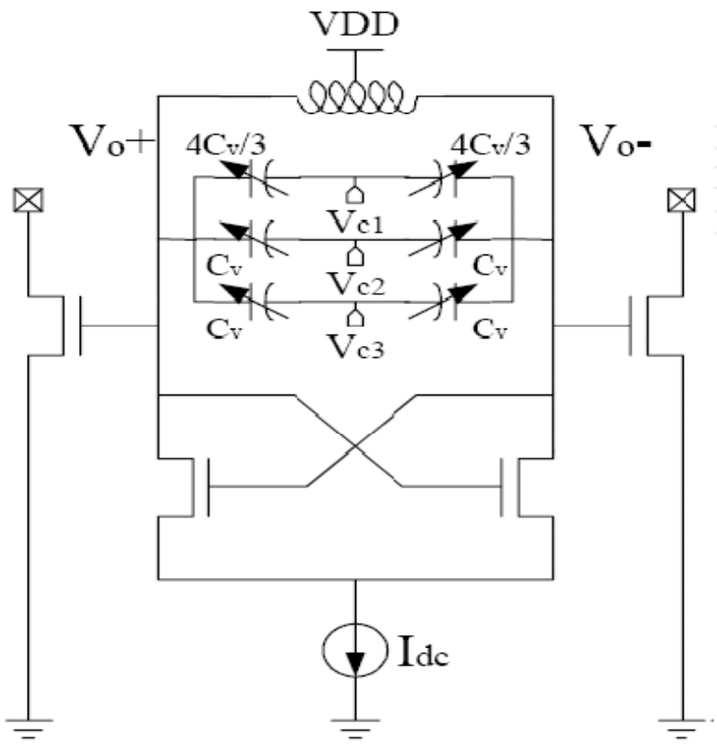


Fig. 23. VCO schematic [24]

The new modified IMOS varactor is utilized in the differential VCO architecture, shown in Figure 23. The simulation results [24] using a 0.18um CMOS technology show that the effective minimal capacitance (C_{min}) is reduced from 775 to 590 fF and the frequency tuning range increases by 500MHz. When the supply voltage is 0.8V, the tuning range of the VCO is from 4.4 to 5.9GHz and the phase noise is -109.65dBc/Hz at 1MHz offset from the carrier at 5.52GHz. The VCO core dissipates 1.2mW of power.
When the supply voltage is reduced to 0.6V, the VCO core consumes only 0.9mW. The tuning range is from 4.7 to 5.9GHz and the phase noise is -105.24dBc/Hz at at the same offset from the carrier.

1.10.1.3 Tuning with Weighted Binary Array

Tuning can be achieved by employing AMOS varactors and a high-Q inductor with a perfectly symmetrical single copper loop [25]. Using an LC cross-coupled differential topology with both PMOS and NMOS latches, fabricated in a 0.13 μm SOI CMOS process, this provides a multi-GHz (3.0-5.6 GHz) wideband VCO. The schematic of the VCO is shown in Figure 24. At a 1 V supply and 1MHz offset, the phase noise is close to -120 dBc/Hz at 3.0 GHz, and -114.5 dBc/Hz at 5.6GHz. The results illustrates that the up-converted flicker noise is reduced in this VCO structure.

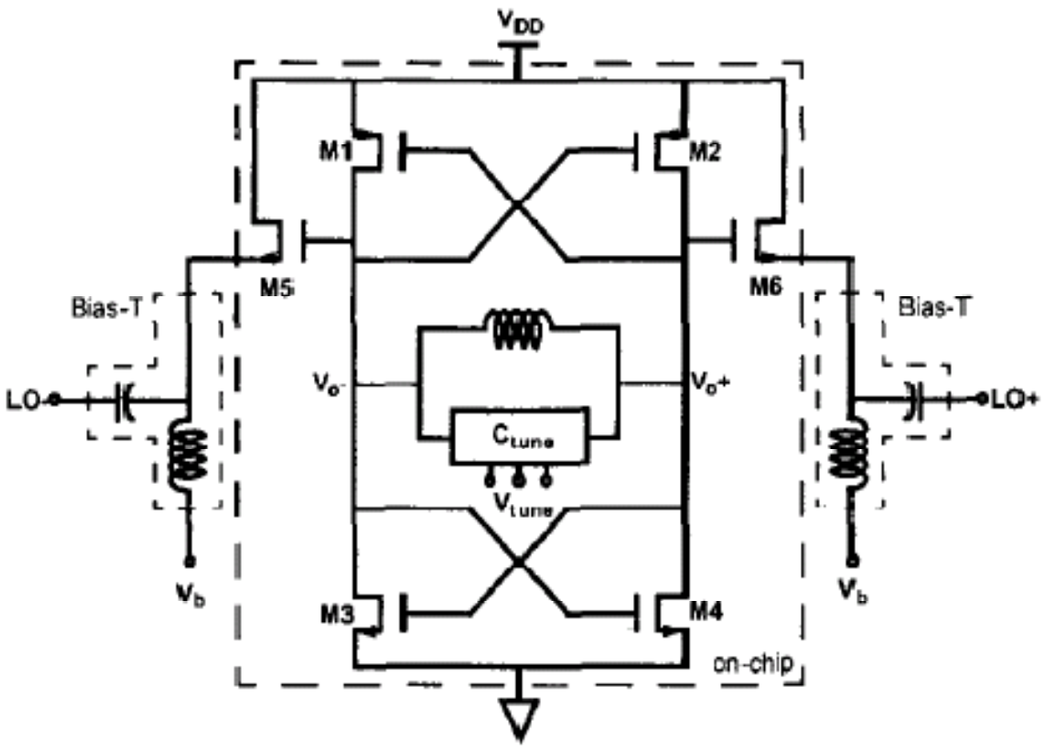


Fig. 24. Schematic of the Band-Switching L-C VCO [25]

1.10.1.4 Tuning with Accumulation-mode MOS Varactors

A very wideband *LC*-VCO in [7], implemented in 0.18μm bulk CMOS, has been described that simultaneously achieves low phase noise and 1.3GHz tuning range around 1.8GHz center frequency. To provide robust operation and stabilize performance over the entire frequency range, the VCO amplitude is controlled using a digital amplitude calibration scheme that does not degrade phase noise and consumes negligible area and power. The proposed calibration-based amplitude control scheme is illustrated in Figure 25.

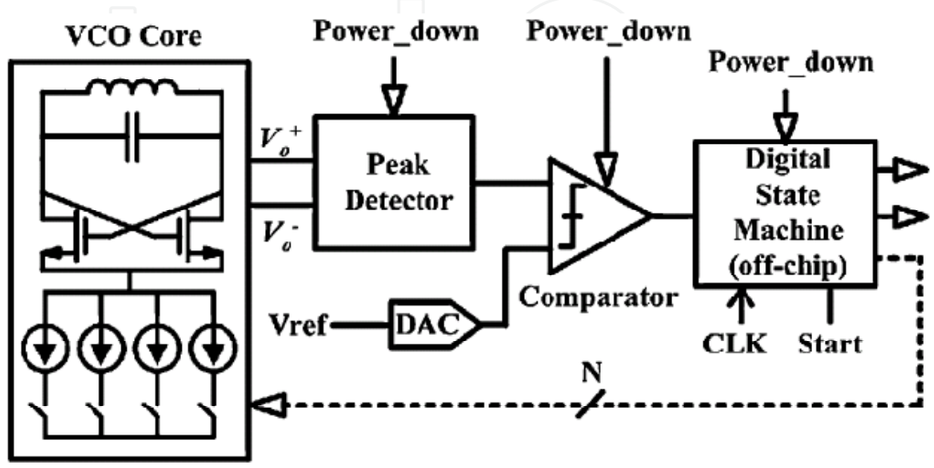


Fig. 25. Proposed calibration-based amplitude control scheme [7].

The VCO core is based on a standard *LC*-tuned cross-coupled NMOS topology. The *LC* tank consists of a single integrated differential spiral inductor, accumulation-mode MOS varactors allowing continuous frequency tuning, and a switched capacitor array providing coarse tuning steps. Figure 26 shows a simplified schematic of the VCO core.
The W/L of the cross-coupled NMOS devices is chosen based on oscillation startup requirements at the low-end (worst-case) of the tuning range.

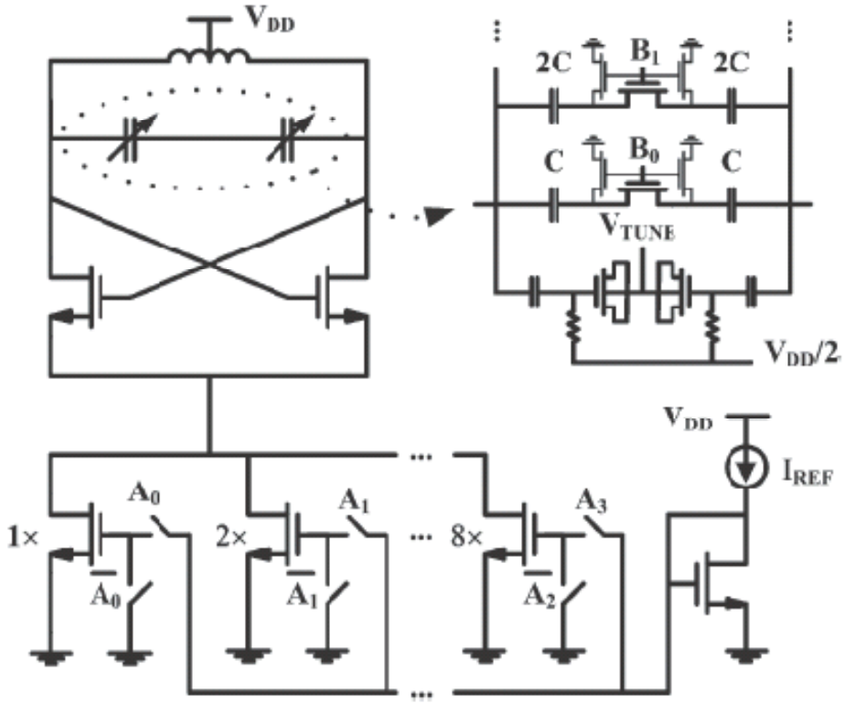


Fig. 26. Simplified VCO core schematic [7].

In order to achieve a large frequency range, the *LC* tank combines a switched capacitor array with a small varactor. The targeted frequency range is split into 16 sub-bands by means of a 4-bit binary-weighted array of switched MIM capacitors. The capacitors are switched in and out of the tank by differential switches.

Suppose a generic binary-weighted band-switching *LC* tank configuration of size n, as shown in Figure 27. Assume that:

$$\beta_v = \frac{C_v}{C_{v,min}} \tag{29a}$$

$$\beta_a = \frac{C_a}{C_{a,off}} \tag{29b}$$

$$\beta_v = \frac{C_{total}}{C_p} \tag{29c}$$

where, $C_{v,min}$ is the minimum varactor capacitance for the available tuning voltage range and is reached as the device enters its depletion mode. $C_{a,off}$ represents the effective capacitance of a unit branch of the array in the off state. The MOS switch in a unit branch of the array contributes a parasitic capacitance C_d that is mainly composed of its drain-to-bulk junction and drain-to-gate overlap capacitors, giving $\beta_a=1+C_a/C_d$.
C_p is the total lumped parasitic capacitance and C_{total} equals the total tank capacitance. Hence, (29c) may be equivalently expressed as $\beta_p=1/(\omega_{o,min}{}^2.L.C_p)$. Furthermore, note that according to equations (29a–c), increasing any one of the defined terms increases the achievable tuning range.

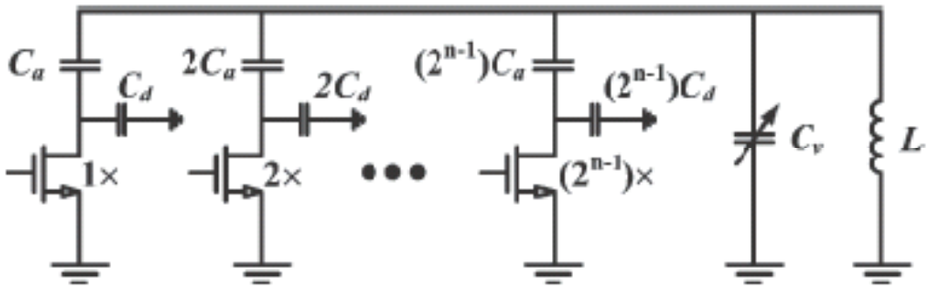


Fig. 27. Generic binary-weighted band-switching LC tank configuration [7].

For a given set of specifications, the tuning range extremities are defined as follows [21]:

$$\omega_{o,min} = [L.(C_v + (2^n - 1).C_a + C_P]^{-1/2} \quad (30a)$$

$$\omega_{o,max} = \left[L.(\frac{C_v}{\beta_v} + (2^n - 1).\frac{C_a}{\beta_a} + C_P\right]^{-1/2} \quad (30b)$$

To guarantee that any two adjacent sub-bands overlap, the following condition must be satisfied:

$$\Delta C_v \geq \Delta C_a \quad (31)$$

where $\Delta C_v = C_v - C_{v,min}$ and $\Delta C_a = C_a - C_{a,off}$. Using (29a) and (29b), (31) can be written as

$$C_v = k.C_a.\frac{\beta_v}{\beta_a}.\frac{(\beta_a - 1)}{(\beta_v - 1)} \quad (32)$$

where k is a chosen overlap safety margin factor and is greater than unity. Equation (32) can be substituted in (30a) to solve for C_a independently of C_v, giving

$$C_a = \frac{\left(L.\omega_{o,min}^2\right)^{-1} - C_p}{k.\frac{\beta_v}{\beta_a}.\frac{(\beta_a - 1)}{(\beta_v - 1)} + 2^n - 1} \tag{33}$$

Thus, having chosen parameters β_a, n, and L, and given design constants $\omega_{o,min}$, k, and β_v, one can solve for C_a and C_v [using (32)]. Taking the ratio of (30b) and (30a) yields the tuning range

$$TR = \frac{\omega_{o,max}}{\omega_{o,min}} \tag{34}$$

To account for the impact of lossy switches, we note that the quality factor of the capacitor array is well approximated as $Q_a=(\omega_o.R_{on}.C_a)^{-1}$, where R_{on} is the resistance of the unit MOS switch. Given that $\beta_a=1+C_d/C_d$, the resulting quality factor of the capacitor array is given by

$$Q_a = \frac{1}{\omega_o.R_{on}.C_d.(\beta_a - 1)} \tag{35}$$

Note that since the MOS switch would generally use the minimum available gate length and $C_d \propto W$, the product is approximately constant for a given technology. Figure 28(a) shows values of TR and Q_a from (34) and (35) plotted versus β_a for a typical scenario, and clearly illustrates the direct trade-off between tuning range and Q_a.

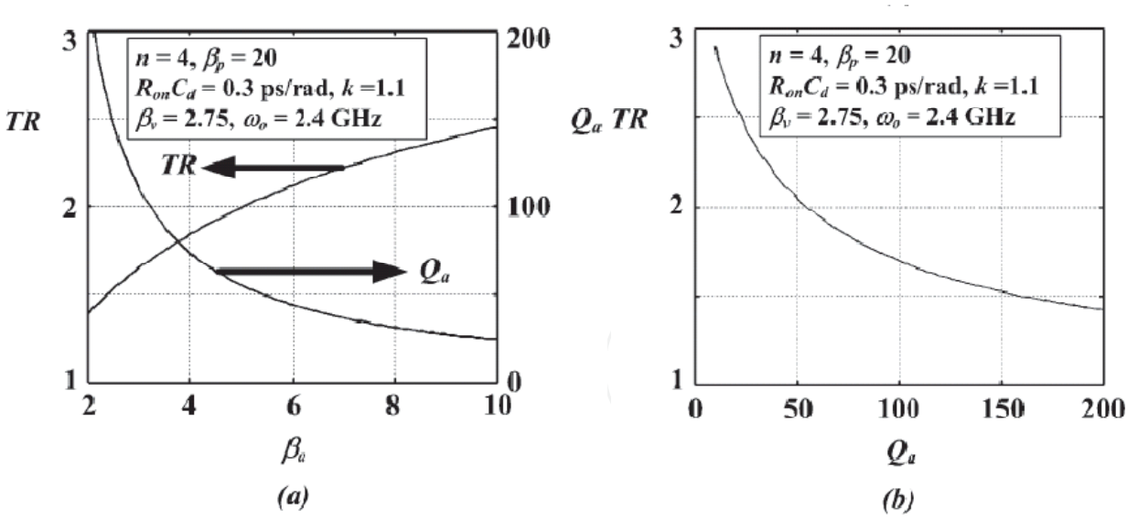
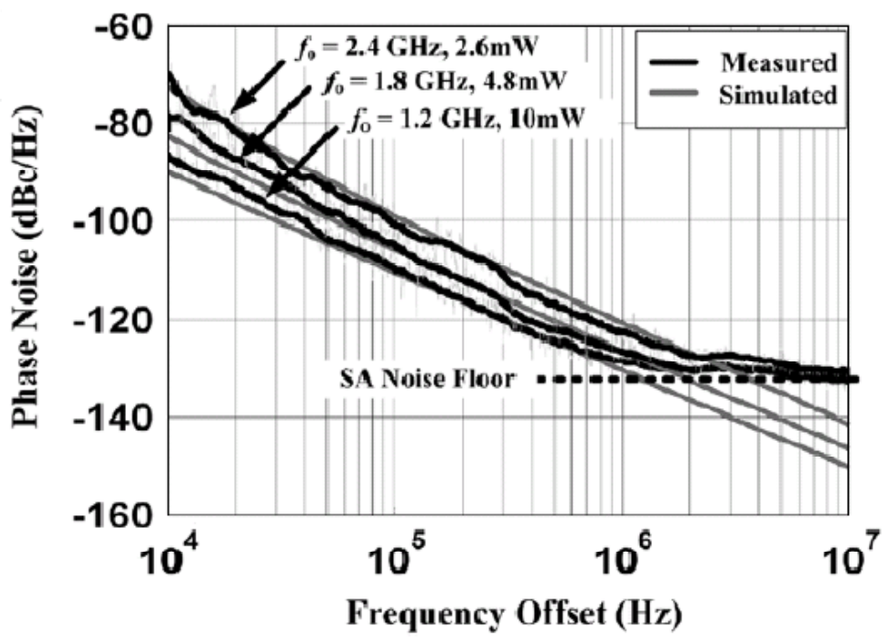


Fig. 28. (a) Tuning range and capacitor array quality factor versus β_a (b) Tuning range versus Q_a [7].

Each switch contributes additional loss to the tank due to its finite resistance, R_{on}. Thus, minimum-length NMOS devices are utilized and made as wide as possible before the resulting parasitic drain-to-bulk capacitance limits the achievable tuning range.
Because the desired tuning range has been divided into several sections, a small accumulation-mode NMOS varactor is sufficient to cover each frequency sub- band.

The tank inductor was realized as a 5.6-nH differential spiral on a 2- μm-thick top metal layer achieving a measured (single-ended) *Q* ranging from about 7.5 to 9 over the VCO frequency range [7].
Figure 29 shows the measured and simulated phase noise at the lower, middle, and upper ends of the tuning range running at a core power consumption of 10, 4.8, and 2.6 mW, respectively. The measured frequency range is 1.14–2.46 GHz.



Figu. 29. Phase noise at 1.2, 1.8, and 2.4 GHz for a core power consumption of 10, 4.8, and 2.6 mW, respectively [7].

1.10.1.5 Tuning with Switched-Capacitor Array and Varactors

Weighted array capcitors may also be used for wideband frequency tuning [3]. Although PMOS transistor requires higher current to provide the same transconductance (g_m) as NMOS transistor, PMOS differential pair is used to achive a better phase noise (see Figure 30).
This design uses a switched-capacitor array and varactor together to form the capacitive portion of the tank. As illustrated in Figure 31, the tank capacitance is formed by a varactor diode capacitance that varies from $C_{v,\,min}$ to $C_{v,max}$, a capacitor array that varies from $C_{a,\,min}$ to $C_{a,max}$, and a parasitic capacitance C_p. In essence, this structure provides coarse tuning via the capacitor array and fine tuning via the varactor.

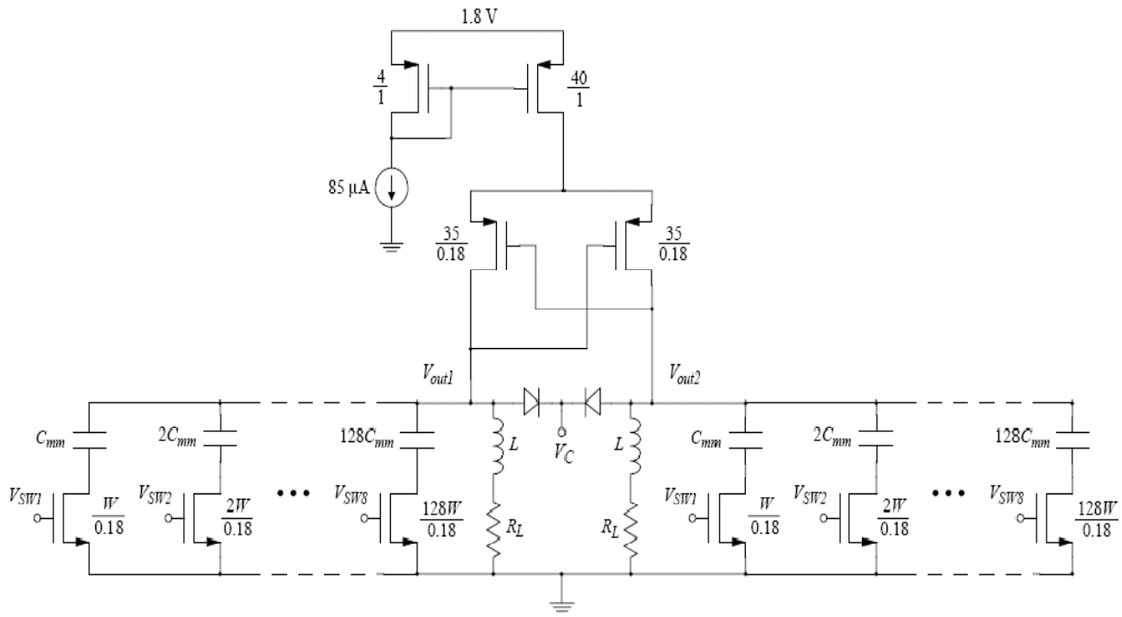


Fig. 30. Complete VCO schematic [3]

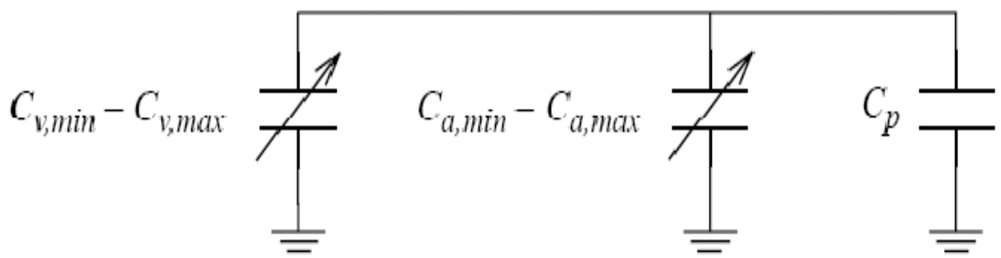


Fig. 31. Tank capacitances [3].

To determine how to size the capacitors, switches, and varactor, one can start with the desired continuous tuning range, f_{min} to f_{max} and inductance range, L_{min} to L_{max}. The widest range of total tank capacitance needed to tune from f_{min} to f_{max} corresponds to the lowest inductance value L_{min}. The minimum and maximum capacitance values that define this range are given by:

$$\boldsymbol{C_{t,min}^{Lmin} = [(2\pi . f_{max})^2 . L_{min}]^{-1}} \tag{36}$$

$$\boldsymbol{C_{t,max}^{Lmin} = [(2\pi . f_{min})^2 . L_{min}]^{-1}} \tag{37}$$

The general binary weighted capacitor array is shown in Figure 32, where C_{mm} represents the capacitance of a metal-metal capacitor and C_{dd} represents parasitic drain capacitance. To maintain a constant Q for each switch/capacitor pair when the switches are on, as each capacitor size doubles, the channel on-resistance must halve. Therefore, the NMOS switch widths are also binary-weighted (since channel resistance is inversely proportional to channel width), and consequentially, the parasitic drain capacitances associated with each switch are binary-weighted too.

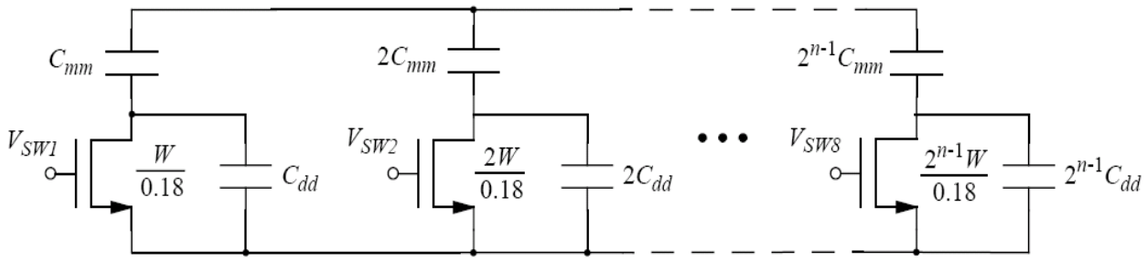


Fig. 32. General binary-weighted capacitor array [3].

Using the above topology, a 2-GHz VCO has been implemented and simulated in a 0.18-µm CMOS process with 1.8V power supply. The resulting tuning range is 1.848 to 2.044 GHz.

1.10.1.6 Tuning with Switched oscillators

In this technique, one of an array of independent oscillators may be selected with a MOSFET switch connected to a common-mode point outside the oscillator loop [23] (Figure 33**).** The inductors which tune each oscillator are sized differently. The outputs combine in buffer FETs with a common drain, one of which is turned **ON** by the selected oscillator. These FETs are of small size so as not to excessively load the resonant circuit in the oscillator core. A larger buffer follows to provide adequate drive to the subsequent circuits. Each oscillator is continuously tuned by a MOS varactor.

With this method, either an array of weighted capacitors may be switched in parallel with a single oscillator core, or one of an array of multiple oscillator cores may be selected, each tuned by inductors of various sizes.

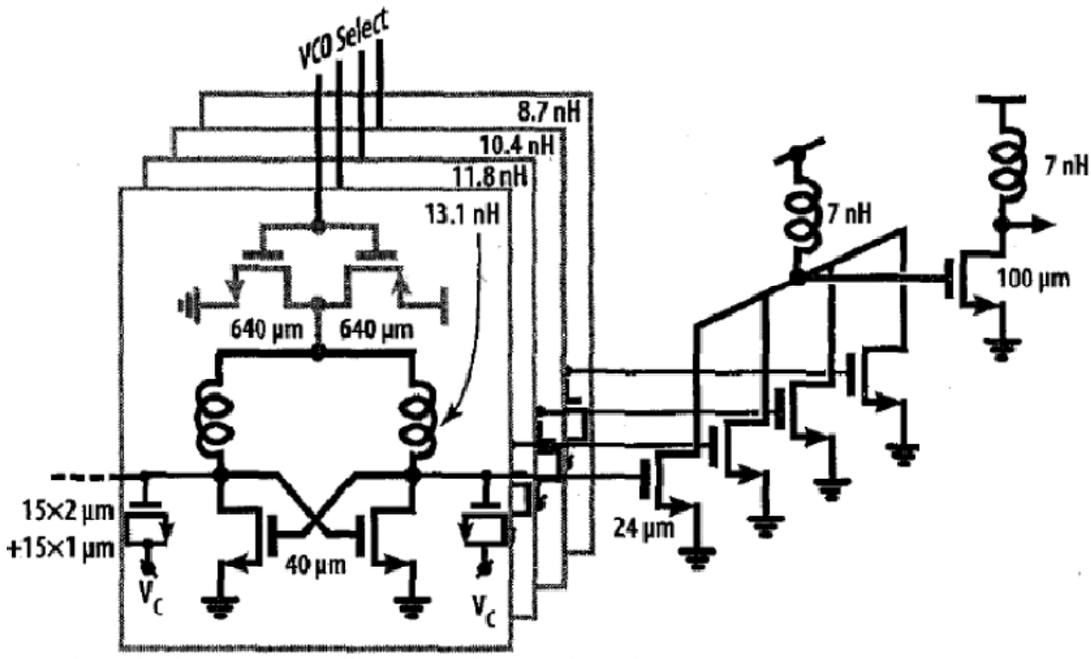


Fig. 33. Switched array of oscillators, with a combined output [23]

Using the above switched tuning methods, RF CMOS oscillators are shown to obtain a wide tuning characteristic, e.g. a frequency range from 1.4 to 1.85GHz with the required overlaps between the switched segments [23].

1.10.1.7 Tuning with Switched Resonator

The switched resonator concept, illustrated in Figure 34, can be utilized to increase the tuning range and to achieve low phase noise over the tuning range at reasonable power consumption [26]. The LC tanks include MOS varactors, inductors, and variable resonator transistors M3 and M4.

In this figure, the inductance seen between ports 1 and 2 is changed by turning M3 on and off. When the transistor is off, the inductance is approximately the sum of L1 and L2. The actual combined inductance is somehow lower due to the effects of C_{GD} in series with C_{GS}, and C_{DB} of M1. These capacitances also affect the capacitance seen from L_1 side (C_{p1}).

When M3 is on, L_2 is shunted out and the inductance is decreased. Furthermore, when M3 is on, C_{p1} is reduced because the transistor capacitances and the capacitances associated with L_1 (partially) and L_2 are shunted to ground by the low on-resistance of M3, thus, leading to simultaneous decreases of inductance and capacitance.

This ability to simultaneously tune L and C provides greater flexibility to trade-off phase noise and power consumption, as well as to achieve given phase noise performance over a larger frequency range compared to using only switched capacitors. In fact the resonators are used for band selection, while varctors provide the tuning within bands. This concept has been implemented for frequencies from 667 to 1156 MHz. The phase noise at a 600 kHz offset versus oscillation frequency is about -123 dBc/Hz.

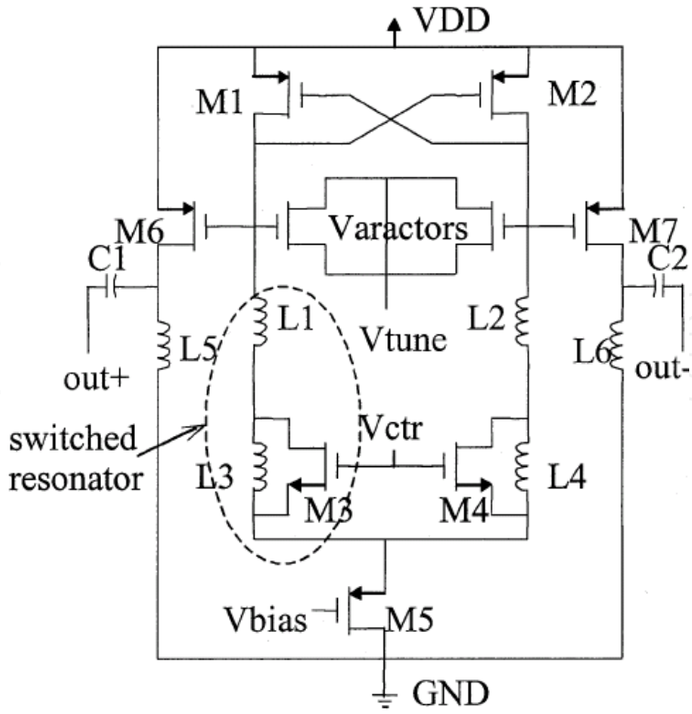


Fig. 34. VCO schematic including switchable L–C resonators [26].

1.10.1.8 Tuning with Variable Inductor

The variable inductor consists of a conventional planar spiral inductor, above which a metal plate is placed such that it can be moved vertically using a MEMS parallel-plate actuator [27]. By generating DC bias between the stationary electrode and the movable electrode (the metal Plate), the metal plate is moved vertically, resulting in the variation of inductance. The bias voltage can control the inductance continuously.

Using the above variable inductor in a LC-VCO (see Fig. 34), fabricated using a 0.35μm CMOS technology, it can be tuned for different frequency ranges [27], e.g. entire tuning is from 2.14GHz to 3.13GHz. The inductance is changed from 3.87nH to 5.98nH, while the respective quality factor changes from 2.98 to 3.87. The typical phase noise at 1MHz offset is -112dBc/Hz, which remains almost constant for the entire tuning range.

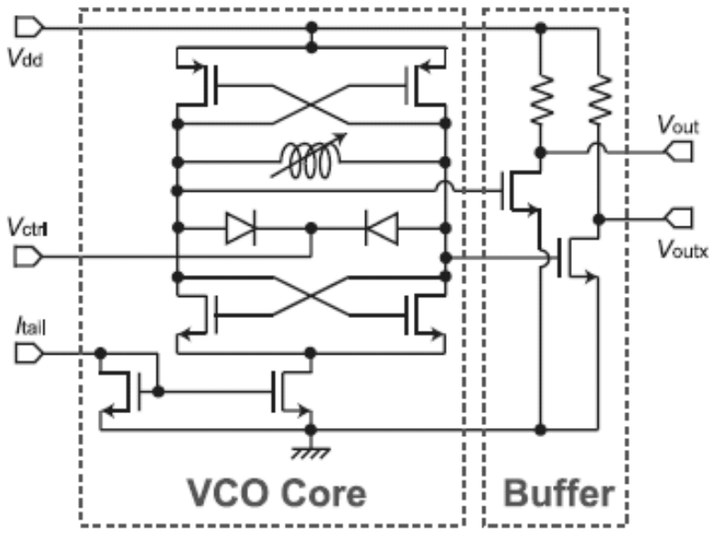


Fig. 35. Schematic of LCVCO [27]

1.11 Phase Noise Improvement Techniques

As explained above, LC-VCO are often designed with sufficiently high phase noise performance. To achieve this, utilizing low-flicker-noise active devices and high-Q resonators are the most commonly techniques. However, with increasing frequnecy tuning range, due to variation in quality factor and ampltitude of oscillation the perfomance may not maintain. In Section 1.7.6 we discussed the techniques of transistor layout design and its biasing to minimize the device noises,which can lead to the design of a high perfomrnace wide tunig VCO. This section presents two simple methods [28, 29] for phase noise reduction which can be incorporated in UWB VCO design.

1.11.1 Harmonic Tuning

Harmonic tuning technique can reduce the phase noise in LC-VCOs [28]. In this technique the output waveform zero crossing points become steeper. As a result, the phase noise is reduced due to increase of the voltage on the resonator.

This is explained using leeson equation for phase noise as follows [28].

$$F = 2 + \frac{8\gamma R I_T}{\pi V_o} + \gamma \frac{8}{9} g_{mbias} R \tag{38}$$

where, I_T is bias current, γ denotes the channel noise coefficient of the FET, and V_0 is the resonator voltage. Clearly, with increasing V_0 due to harmonic tuning, F is reduced. In addition, in this technique the S_{11} parameter is shorted at second harmonic, which improves the phase noise further. Figure 36 illustrates the schematic of the VCO before and after phase noise improvement.

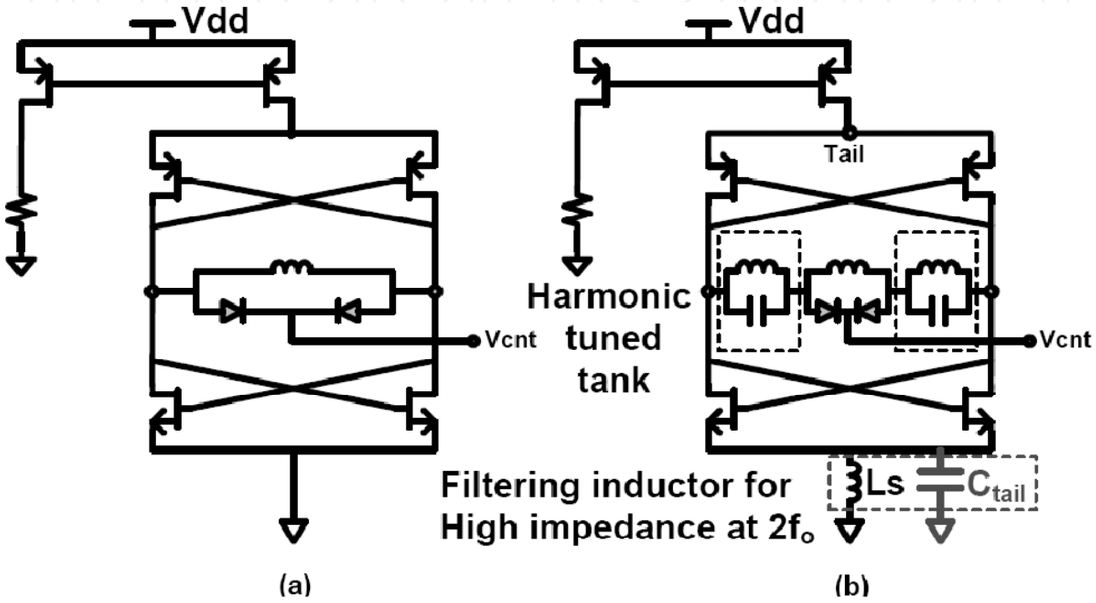


Fig. 36. Schematic of VCO (a) before (b) after phase noise reduction

As can be seen in Figure 36 (b), two series resonators are utilized in addition to main resonator.These resonators are designed such that they are open in fundamental and third harmoics frequencies, while they are shorted at second harmonics. Thus, the output signal attains a rectangle shape instead of a sine wave.This in turn reduces the phase noise due to abrupt switching.

Noise fitering is also exploited in [28]. In top-biased differential oscilators, direct connection of NMOS pair to ground forces one of them to enter the triode region when they turn off. This reduces the quality factor in general . Using LC pair with oscilation frquency at second harmonic gives a high impedance at this harmoic and removes the loading effect of oscillator in triode. This technique may improve the phase noise by 10dB [28].

1.11.2 Feedback method

An alternative technique for noise suppression is given in [29], in which a frequency to current converter (FCC) extracts the noise properties of VCO output signal. This extracted current then passes through an integrator, which converts it to a voltage carrying important noise and frequency properties. This voltage will enter a low pass filter and fed back as an input voltage to the oscillator.

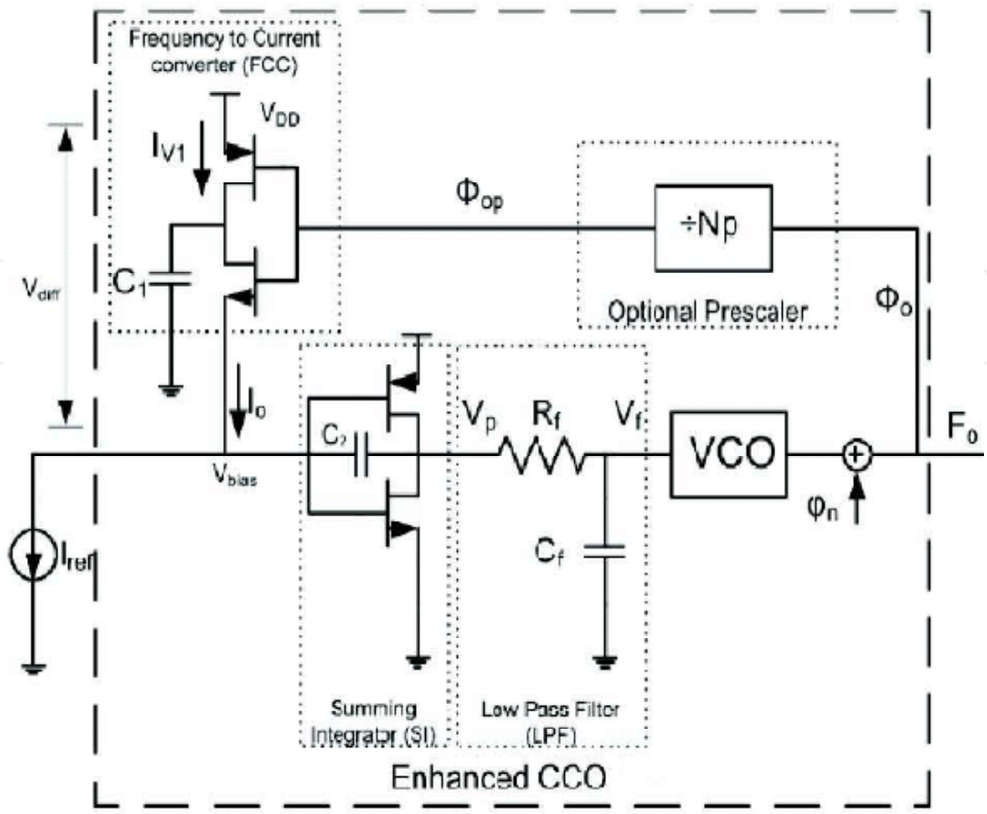


Fig. 37. Schematic of phase noise reduction with feedback [29]

The system in Figure 37 can be interpreted as current controlled oscillator (CCO), which exhibits better noise compared to its initial state. The output capacitance of FCC is charged to VCC in each period and then discharged to V_{bias}. Therefore, the current source in FCC represents the phase noise characteristics of VCO output signal. The difference between this current with I_{ref} is integrated. The output voltage is proportional to signal phase noise. The filter suppresses the high frequency component. This technique can give rise to 10dB phase noise improvement [29].

1.12 Design of Ultra Wideband Oscillators

Design of Ultra wideband (UWB) VCOs demands extending the tunability bandwidth to multi-gigahertz range (i.e. in the range of 3 to 10GHz). A method to achieve this is based on tunable active inductors (TAI) despite their noise and nonlinearity, since they have major advantages over passive inductors in terms of area, tunability, and higher Q factors.

This section describes the design of UWB CMOS VCO, using the tunable active inductor (TAI) presented in section 1.7.4. The transistor sizing, layout issues, and the trade-off between power and bandwidth are discussed. Also, the robustness of the oscillator performance under reduced bias voltage, temperature change, and process variations are examined. Finally, the effect of packaging is investigated.

1.12.1 TAI-Based VCO

In order to incorporate the one-port TAI, the conventional single-ended Colpitts or Hartley topology can be chosen (see Figure 1). The former incorporates a single inductance, and hence replacing it with TAI provides a limited improvement of its tuning range. On the other hand, Hartley topology can incorporate two TAIs, and therefore it provides a wider tuning range [19, 33]. However, the phase noise degradation due to these TAIs is a concern, which demands a technique of phase noise reduction for this structure. These are discussed in the following.

1.12.2 TAI-based Colpitts VCO

A TAI-based VCO may be implemented using the Colpitts topology shown in Figure 1(a). In this implementation, the output has been derived from the drain using a load inductor (L_{load}). This isolates the output port from the resonator and also provides a higher output power. Note that, higher value of the load inductor also helps in harmonic suppression.

The proposed TAI is illustrated in Figure 38(a), and the TAI-based Colpitts oscillator [30] is shown in Figure 38(b). The expressions for the undamped oscillation frequency, as well as the start-up condition for oscillation in terms of the resonator elements and the intrinsic parameters of the transistor M_1 are:

$$\omega_n \approx \sqrt{\frac{(C_1C_2 + C_2C_3 + C_3C_1) + \left(\frac{R_l C_1 C_3}{R_{ds}}\right)}{C_1C_2C_3L + \left(\frac{R_l C_1 C_2 C_3 L_{load}}{R_{ds}}\right)}} \tag{39}$$

$$\boldsymbol{g_m \gg \left[\frac{\omega_n^2 LC_1C_3 - (C_1 + C_3) + A}{C_3 R_{ds}}\right]}$$

$$\boldsymbol{A = \omega_n^2[L_{load}(C_1C_2 + C_2C_3 + C_3C_1) + RR_{ds}C_1C_2C_3 - \omega_n^2 LL_{load}C_1C_2C_3] > 0} \tag{40}$$

C_3 has to be chosen large as compared to C_1 and C_2 such that it has negligible effect on the oscillation frequency. From the denominator in (39), it can be observed that $R_l << R_{ds}$ and L_{load} (denoted by Z_{load} in Figure 38(b)) is of the same order as L_1. Thus, L_{load} has a negligible effect on ω_n. However, the use of L_{load} demands a higher g_m for the start -up condition due to the additional positive term A in (40).

Equation (41) gives the dependence of the phase noise on the loaded Q, noise generated, and the signal power on the resonator node.

$$L\{\Delta\omega\} \propto \frac{NKT}{PQ^2}\left(\frac{\omega_o}{\Delta\omega}\right)^2 \tag{41}$$

where, N is the noise factor, P is the signal power at the resonator, Q is the loaded quality factor of the resonator, and $\Delta\omega$ is the deviation from the carrier frequency.
From (39), it is evident that $R_l << R_{ds}$, and hence, has a negligible effect on the oscillation frequency. However, it has a significant effect on the Q of the inductor, as well as the loaded Q of the resonator, which directly affects the phase-noise performance of the oscillator (see (41)).
Although the high Q of the active inductor has a positive effect on the phase-noise performance, the active devices in the inductor generate additional noise that results in a higher noise factor, which degrades the phase noise.

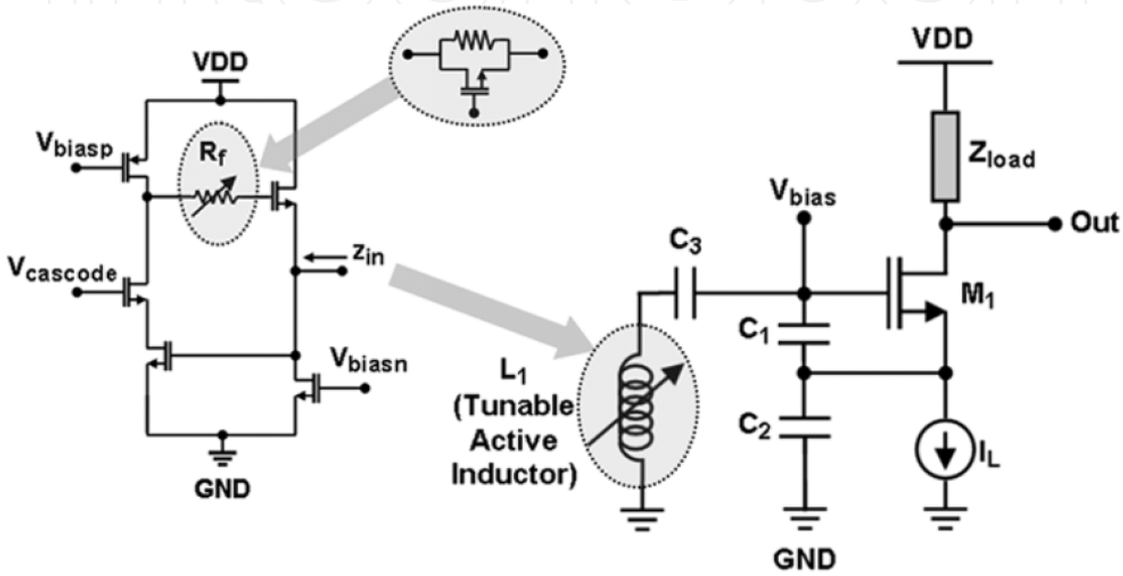


Fig. 38. Circuit schematic of the TAI-based Colpitts VCO [30]

With the above TAI-based VCO implemented in a 0.18μm standard CMOS technology, a frequency range of 500 MHz – 2.0 GHz is achieved [30].The total circuit consumes 13.8 mW of power from a 1.8-V supply. The phase noise varies from -78 to -90 dBc/Hz at 1-MHz offset from the carrier over the tuning range.
In general, phase noise decreases with oscillation frequency. One possible reason for this might be that a lower resistance is required in the active inductor to generate lower inductance, resulting in higher oscillation frequencies.
Moreover, from the trend of the phase-noise variation, it can be found that the noise floor is reached very early, which results in the flat characteristics of the phase noise at offsets higher than 1 MHz. Also, for high output power, the phase noise decreases. However, the variations of the output power and phase noise with the oscillation frequency are not monotonous.

1.12.3 TAI-based Hartley UWB-VCO

The basic structure for Hartley oscillator with a common source amplifier and passive inductors is shown in Figure 39(a). Also, Figure 39(b) illustrates this oscillator using two grounded active inductors in parallel.

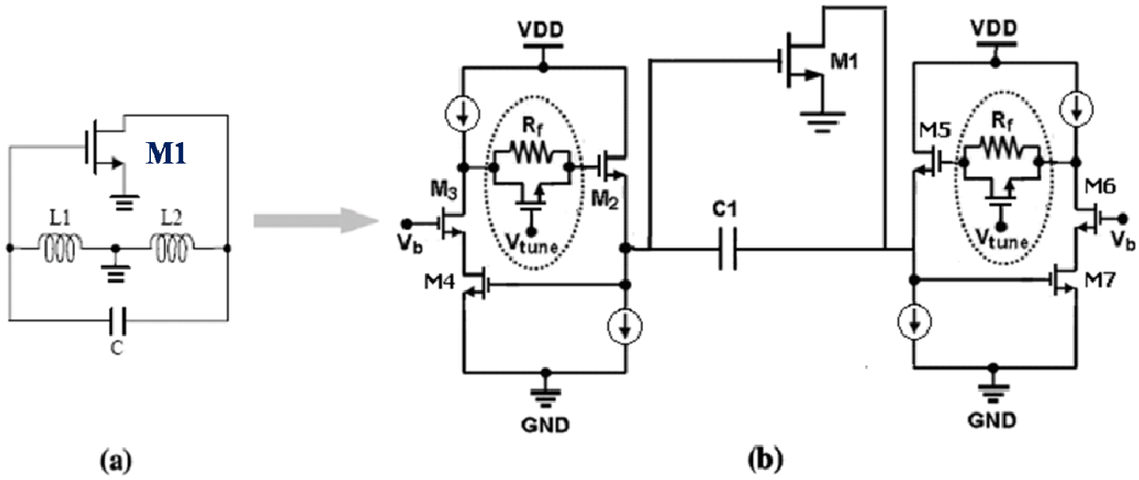


Fig. 39. a) Schematic of Harley Oscillator b) Harley oscillator with active inductors

To prevent the drain of the transistor from any external loading effects and also to suppress the harmonics, the transistor drain can be connected to feedback loop and the supply voltage through a series capacitance and a passive RF choke (see Fig. 40), respectively. Note that, the value of L larger than 5nH will sufficiently suppress the harmonics.

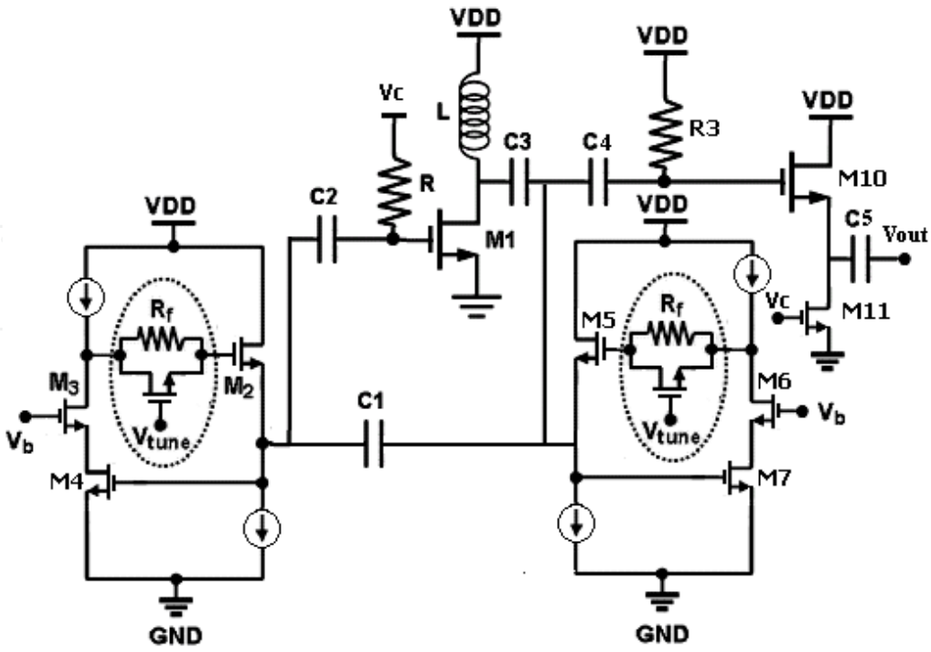


Fig. 40. Proposed schematic of UWB VCO

Assume the inductances associated with the two TAIs are L_1 and L_2. For starting the oscillation, the gain of the feedback system must equal to unity and the phase shift around the loop should be zero. Basically, the frequency of operation is $1/\sqrt{(L_1+L_2)C_1}$. However, in high frequency, the inductance L and the parasitic capacitances of the transistor M1 should also be counted for.

Thus, the size of M1 has an important role in frequency of oscillation, as well as in phase noise and power dissipation. The optimum size of the transistor is obtained when its gate-to-source capacitance (Cgs) is nearly equal to the feedback capacitance [19, 33]. In Fig. 41, the effect of width (W) of M1 on the phase noise and frequency of oscillation is illustrated, using a 0.18μm CMOS technology.

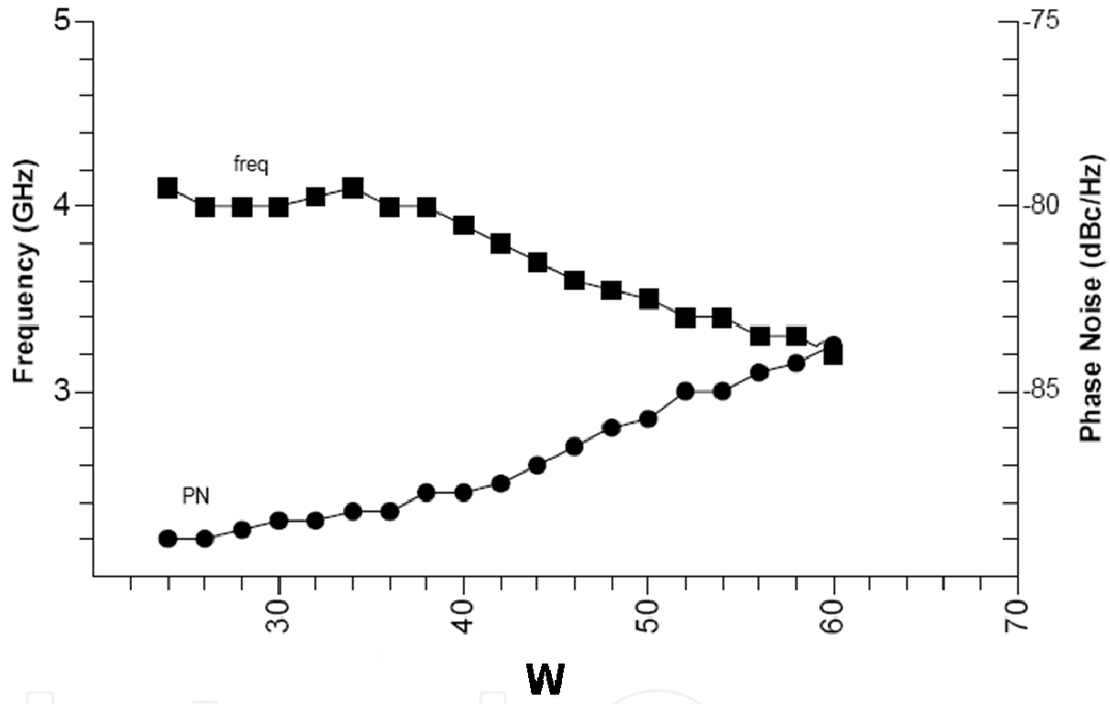


Fig. 41. Frequency and phase noise variation versus width (**W**) of M1

Obviously, when W increases, the frequency reduction is due to increasing parasitic capacitance and hence the total capacitance in the LC tank. The optimum W for 4GHz is achieved for W=38μm which gives rise to -88dBc/Hz of phase noise at 1MHz offset from the carrier.

The value of L also impacts the frequency and phase noise. The reduction of L for increasing the frequency is reasonable as long as it sufficiently suppresses the harmonics. Figure 42 shows the effect of using a relatively small **L** on output harmonics. Note that with decreasing the size of M1, the minimum requirement for **L** is increased because of smaller capacitance associated with M1.

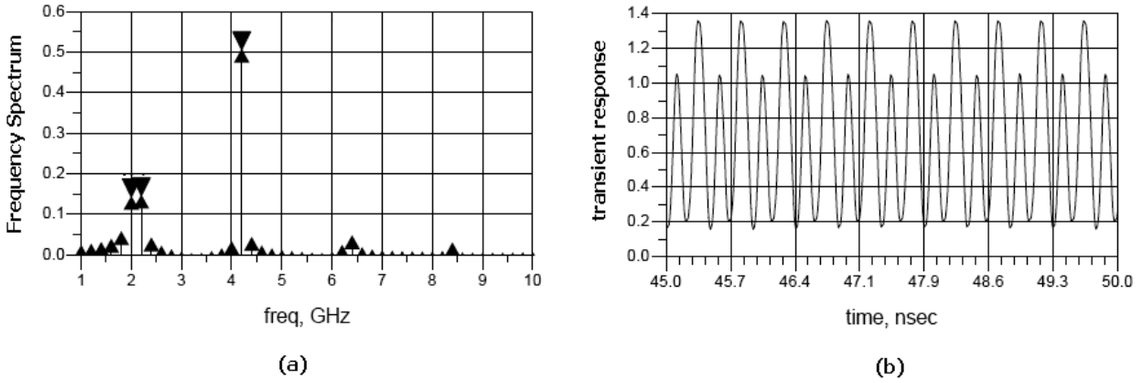


Fig. 42. a) spectrum of output signal b) time domain output signal with harmonics

Also, the value of resistance (R) in the gate of M1 affects the amplitude and bandwidth of oscillation. A typical value of 0.5KΩ can provide 1.3V of amplitude.
The capacitances in the feedback loop determine the phase noise and the frequency. Figure 43 shows the effects of C2, C3, and C4 on frequency. Small variations of the capacitors give rise to limited change in frequency, while the change in phase noise is large.

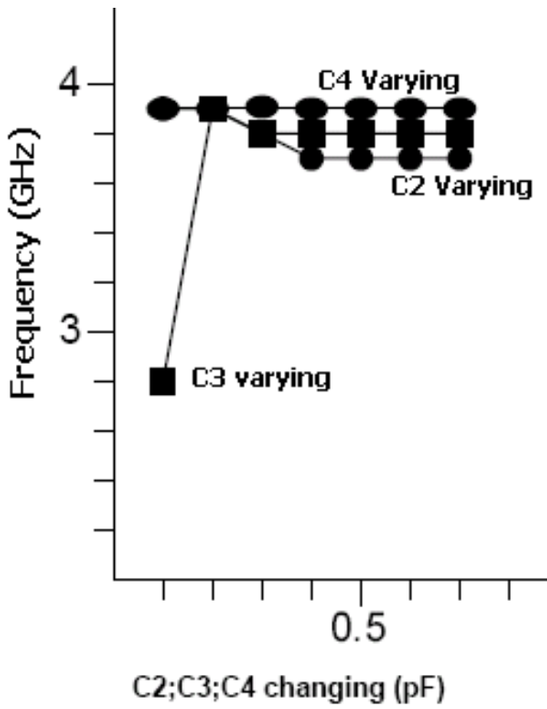


Fig. 43. The effect of capacitors on frequency

The lowest phase noise is achieved when the capacitors are equal. In this case, the optimum noise at 3.8GHz is -92dBc/Hz at 1MHz offset. Based on the results in Figure 41 for transistor sizing, the feedback capacitance C1 is approximately 10fF, i.e. the same size as C_{gs} in M1. The effect of C_1 as the main capacitor in the feedback has a significant impact on oscillation frequency and bandwidth. With decreasing C_1 higher frequency and better phase noise are

achieved at the cost of decreasing the tuning bandwidth. Figure 44 shows the frequency as a function of C1.

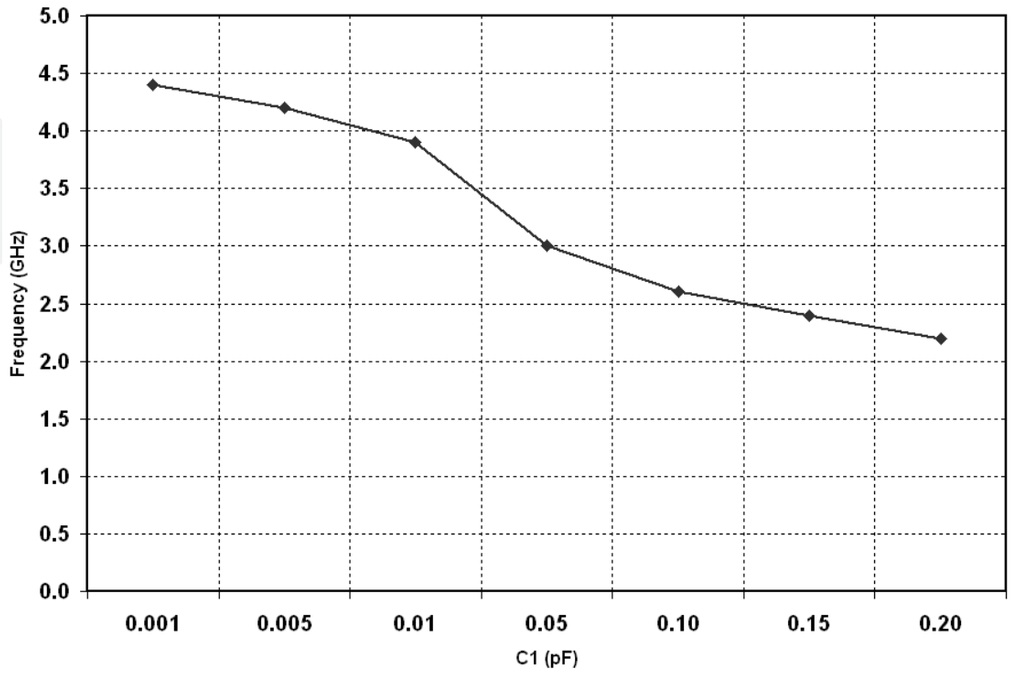


Fig. 44. Frequency as a function of C1.

The tuning of TAI is accomplished by the voltage V_{tune} of the transistor in feedback path (see Fig. 39), as long as its Vgs<Vt. Thus, the sizing of M1 is an important factor for tuning range.

By increasing the aspect ratio (W/L) of M1, it needs a smaller gate voltage. As a result, the tuning transistor turns on with smaller voltage values, which in turn reduces the tuning range. By reducing the aspect ratio of M2, the equivalent capacitance of the active inductance is reduced, resulting in a better phase noise. Decreasing g_{ds} of M2 decreases the low-end frequency of the active inductance, and hence provides a wider tuning range.
The g_{ds} of M2 also affects the Q factor, and provides a way of preventing Q degradation. Thus, the active inductance is tuned using both V_{tune} and V_b.
Taking into account the feedback loop, the gain expression for VCO results in the following equation:

$$\left(CC_3LL_1\right)\omega^4-\left(CL_1+C_3L_2+C_3L\right)\omega^2+1=0 \tag{42}$$

Solving (42) for ω, we have:

$$\omega=\frac{\left(CL_1+C_3L_2+C_3L\right)-\sqrt{\left(\left(CL_1+C_2L_2\right)^2+C_2^2L^2+2C_2^2LL_1-2CC_2LL_1\right)}}{2CC_3LL_1} \tag{43}$$

The accuracy of operating frequency obtained from (43) will be compared to that obtained from simulation in the following.
Simulation illustrates that the phase noise is minimized when the sizing of transistor M1 is such that its C_{gs} is the same as C_1. Also, M1 plays a major role in designing the centre frequency of operation. As the aspect ratio (W/L) of M1 is increased, the central frequency will decrease, at the cost of higher total power dissipation. The variation of operating frequency versus Width (W1) of M1 is depicted in Figure 45.

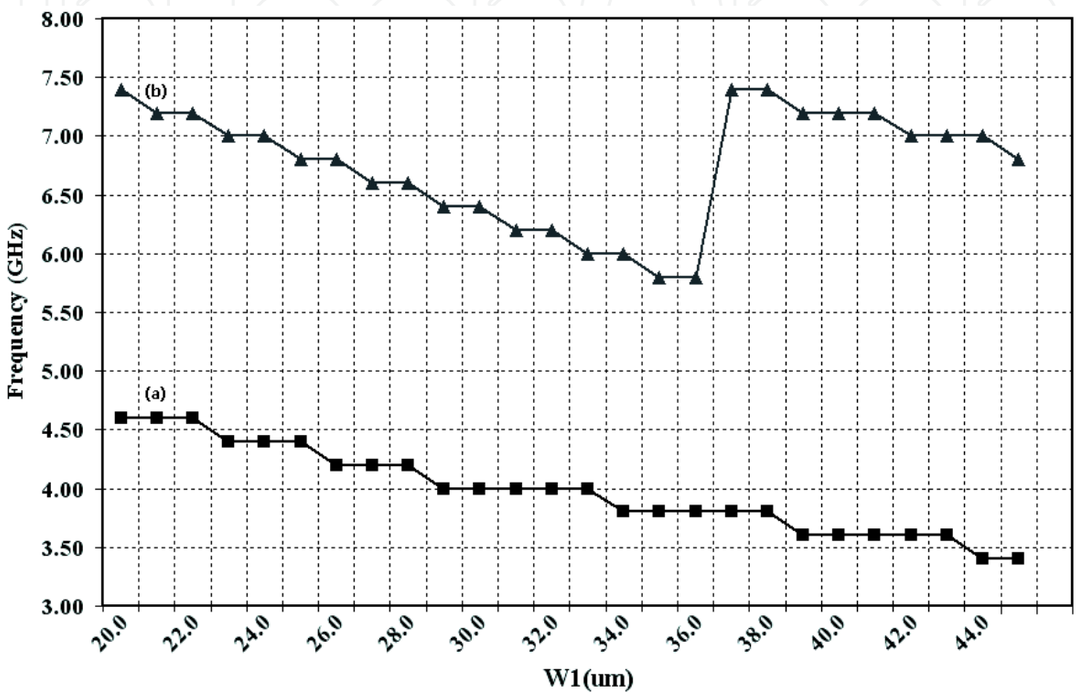


Fig. 45. a) lower frequency variation (b) upper frequency variation

As this figure shows, with decreasing the width of M1 and using the highest V_{tune}, output amplitude tends to reduce while frequency is increased. When the width is 37μm, the oscillator enters non-oscillation mode, forcing to decrease V_{tune} by 0.1V. Consequently, the high-side frequency range is lowered. This will also occur for 20μm width.
On the other hand, enlarging M1 increases the power. Figure 46 illustrates the trade-off between the power and bandwidth.

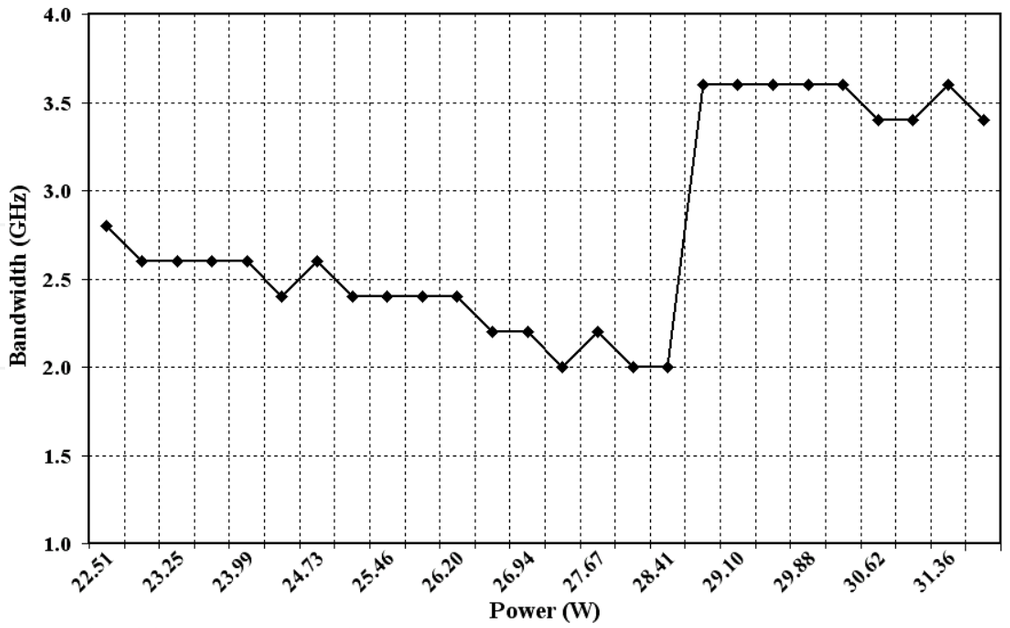


Fig. 46. Bandwidth variations with power

Thus, given the bandwidth and power, Figure 45 and Figure 46 can be used for proper sizing of M1.

Output stage in Figure 40 consists of a source follower amplifier (M10-M11), which in addition to DC cancellation handles the effects of the next stage. In contrast to M1 sizing, W/L ratio of the output stage less likely affects the frequency of oscillation. However, enlarging the size of the output stage improves the phase noise, as shown in Figure 47.

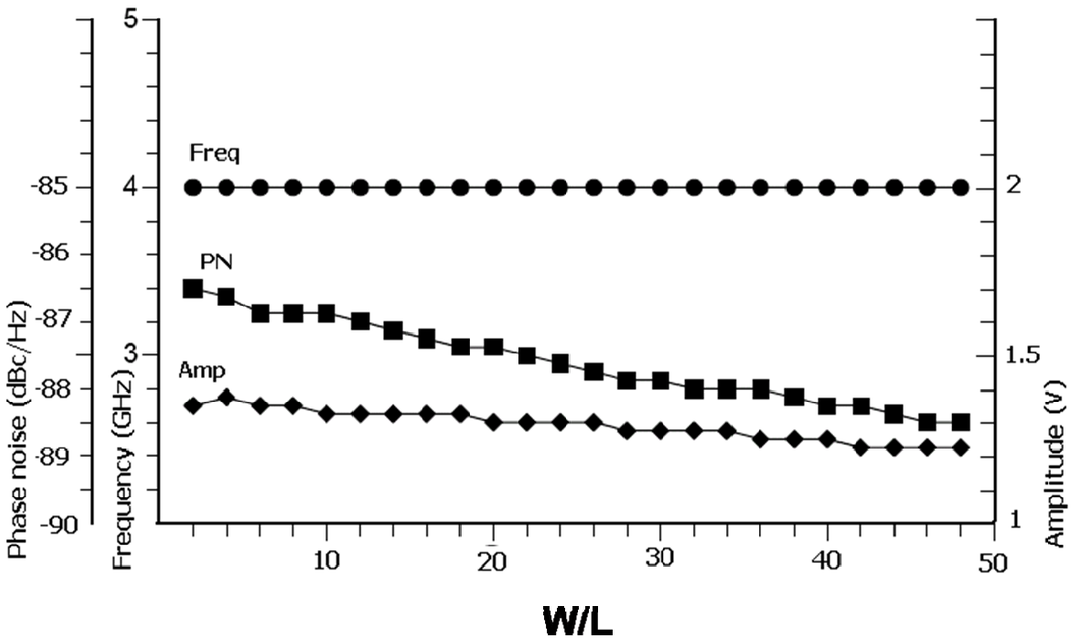


Fig. 47. Phase noise, amplitude, and Frequency versus (W/L) of output stage

1.12.3.1 Comparisons

The circuit in Figure 40 is simulated in a 0.18μm CMOS technology with a power supply of 1.8V. The complete VCO with the values of its elements is shown in Figure 48. The total power is 29.1mW, with dc current of 2mA in active inductor and 17mA in the main core of oscillator. Tuning range of 3.8GHz- 7.4GHz is achieved by varying V_{tune} from 1V to 2.5V, as shown in Figure 49. Maximum quality factor of active inductor is acquired at 3.8GHz with 0.55nH inductance. At 1MHz frequency offset, phase noise varies from -92.05dBc/Hz to -70dBc/Hz.

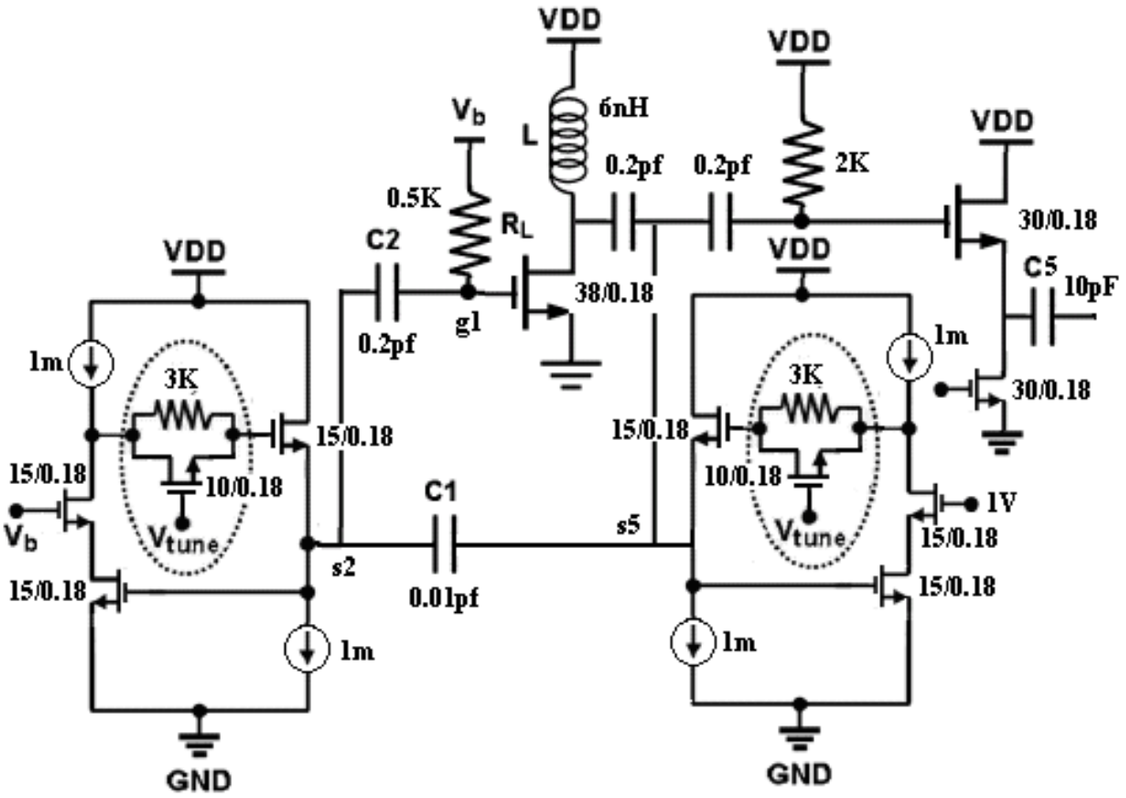


Fig. 48. The final circuit used for simulation

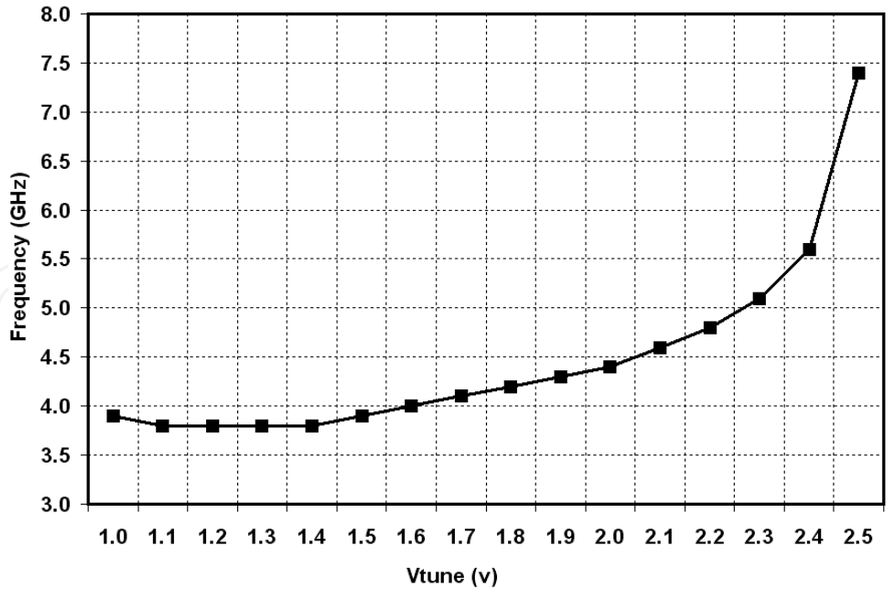


Fig. 49. Frequency variation with V_{tune}

Comparison of the accuracy between frequencies computed from (43) and those obtained from simulation are shown in Figure 50. V_{tune} can be increased until the parallel NMOS in active resistor switches on. As a result, the active inductor can be tuned from 0.34nH to 0.61nH, as depicted in Figure 51.

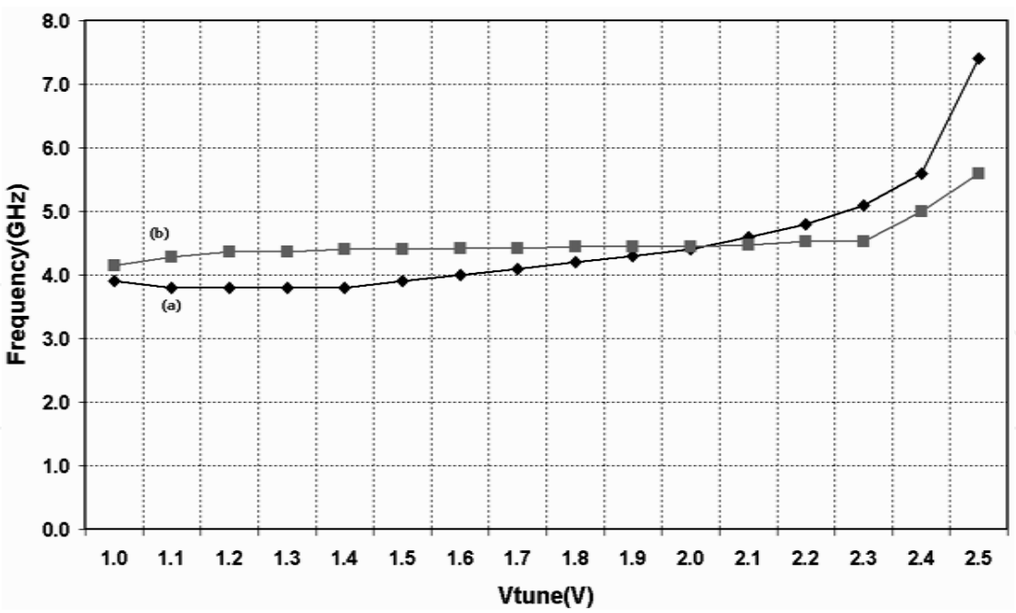


Fig. 50. (a) simulation results (b) frequencies derived from equation (43)

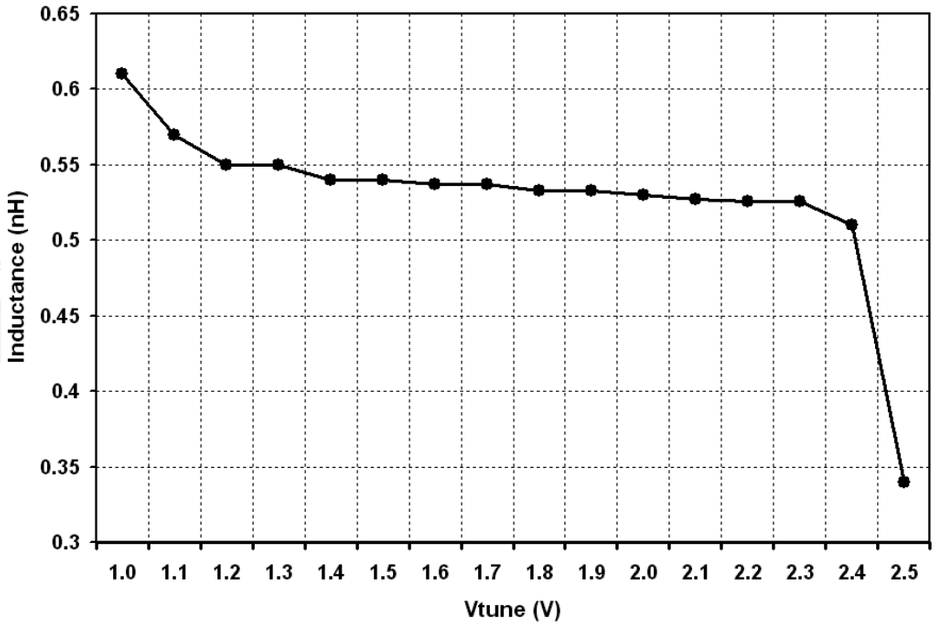


Fig. 51. Inductance variation with Vtune

1.12.3.2 Phase Noise Results

For phase noise simulation, different trade-offs between circuit elements may be examined to estimate the best performance. Simulations show that, when C2, C3 and C4 are equal, the best phase noise performance is achieved. Despite [30], which employs only a single biasing voltage for active load, separate bias voltage, Vc, can be utilized for active load M11 (see Figure 40). This will prevent quality factor degradation due to increasing V_{tune}, and improves the phase noise about 4dBc/Hz, as shown in Figure 52.

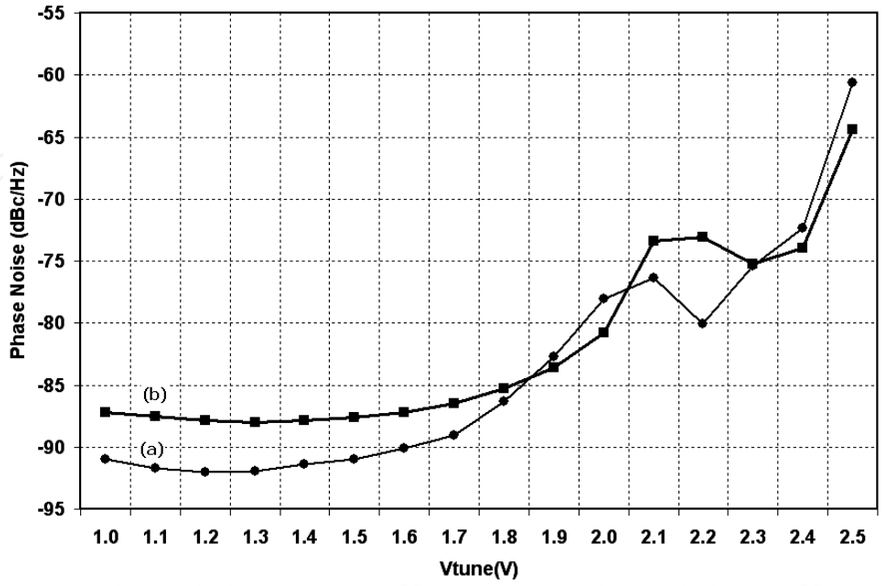


Fig. 52. (a) phase noise variation by tuning V_C (b) phase noise variation for V_C=constant

1.12.3.3 Effect of Bias Voltage Decreasing

The oscillator performance may also be examined by decreasing the supply voltage. Obviously, this will reduce the amplitude of oscillation. In this case, the phase noise quickly wraps up to worse quantity. The results of simulation at 4GHz show that reducing V_{DD} to 1.4V will have negligible effect on phase noise. Nevertheless, further reduction of the supply voltage will significantly degrade the phase noise, such that for V_{DD} =1V phase noise is -82dBc/Hz. Despite this, the frequency range of operation tends to maintain. These are shown in Figure 53 and Figure 54.

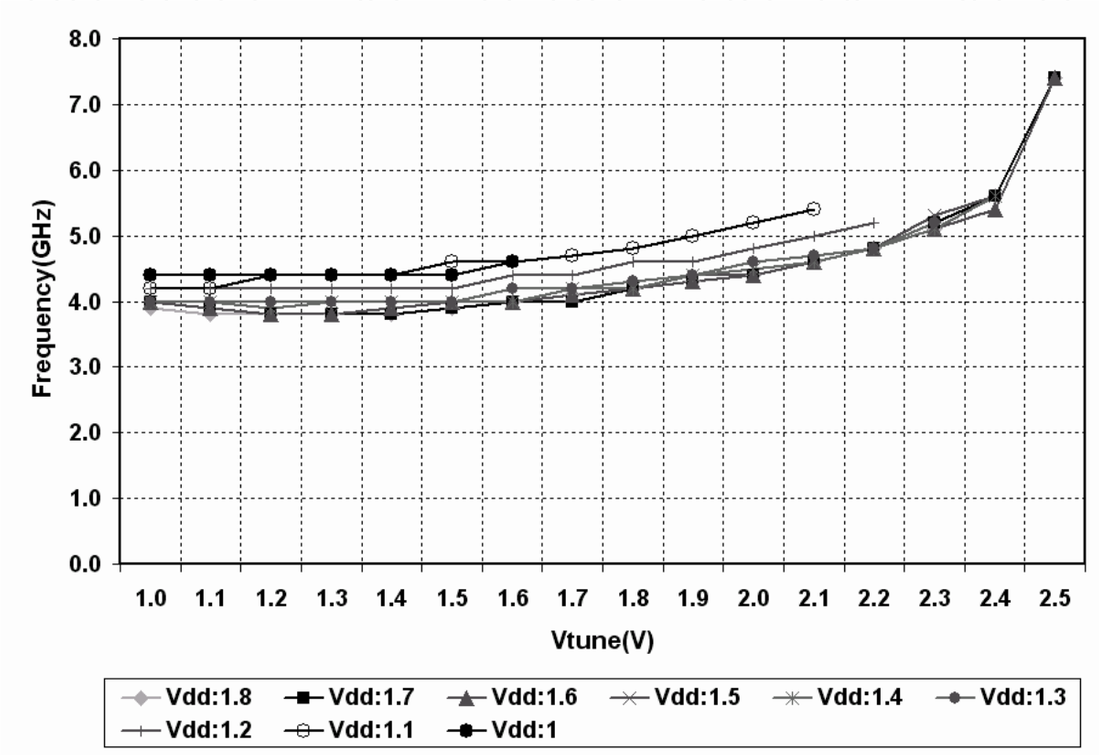


Fig. 53. Bandwidth with Vdd reduction

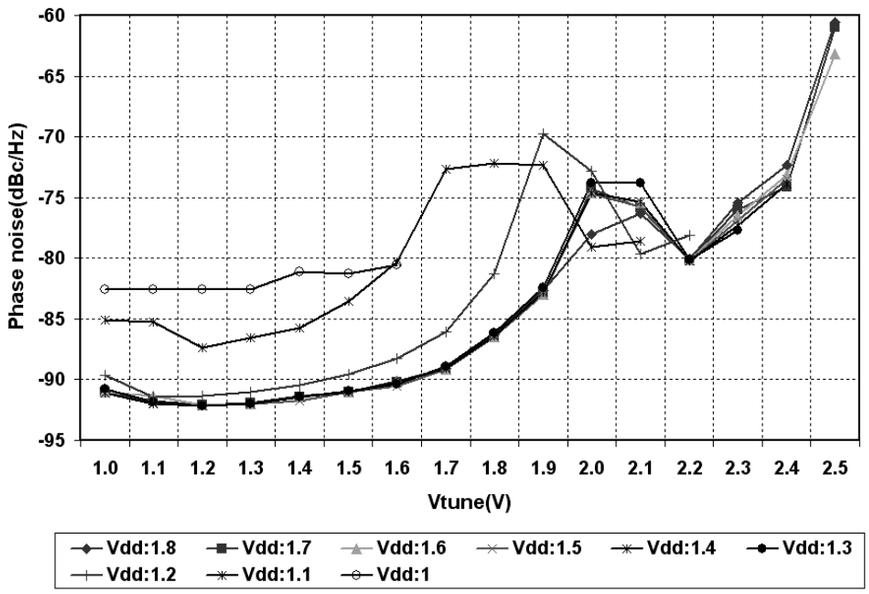


Fig. 54. Phase noise versus Vdd reduction

1.12.3.4 Effect of Process Variations

Simulation results show 2% and 0.1% change in frequency and phase noise, respectively, for 5% variation in bias voltage. For 10% change in temperature, the phase noise is only changed by 0.1% while the frequency is approximately constant.
In addition, mobility variation of NMOS model around 5% shows 0.5% and 1% variations in phase noise and frequency of operation, respectively.

1.12.3.5 Package and Wirebond Modeling

For accurate simulation of the RF circuit, an equivalent model of pad including the bonding wires is required to be tested [11]. Suppose the QFN package with equivalent model of Figure 55 is employed [31].

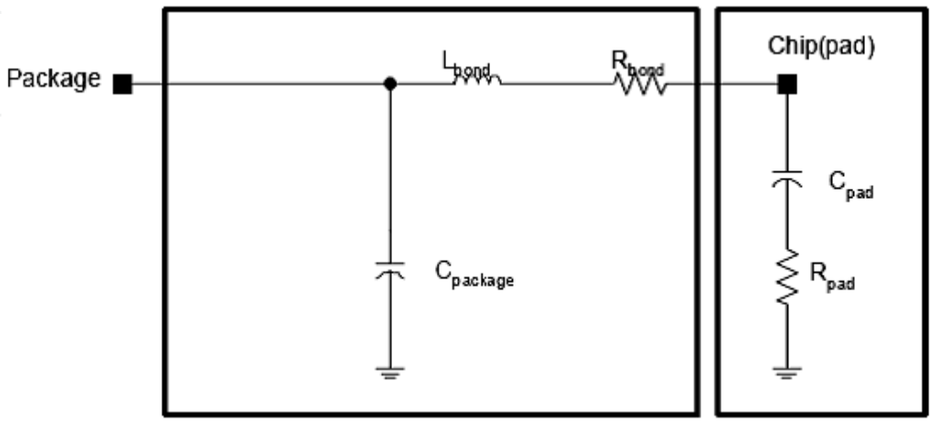


Fig. 55. Wirebonding and pad model [31]

Simulations show that adding the model elements to the circuit reduces the high-end frequency of the tuning range from 7.4GHz to 7.0GHz, while the phase noise will experience slight improvement. Other package models [32] were also tested for 3.8GHz. The results are compared in Table 1.

Package model	Frequency (GHz)	Phase Noise (dBc/Hz)	Equivalent circuit		
			L(nH)	C(pF)	R(Ω)
SOIC-20	3.8	-91.84	5.01	0.71	0.03
SSOP-20	3.8	-92.21	3.49	0.42	0.04
TSSOP-20	3.8	-92.18	2.80	0.31	0.05
TVSOP-20	3.8	-92.11	2.56	0.34	0.04
QFN-20	3.8	-92.25	1.10	0.35	0.05

Table 1. comparison between different package models

1.12.3.6 Oscillator Layout

Layout design can be divided into two parts as of passive and active devices. Capacitors and passive inductor may be designed using different layers of metals [19, 26]. For instance, passive inductor (L in Figure 48) can be implemented with 4 metal layers, which exhibits a very low serial resistor. Nevertheless, it introduces a very large parasitic capacitor, forcing the layout to be changed to one-layer design [19]. Here "L" is designed as square spiral inductor with layer one metal. Total area occupied for the lumped inductor is 157 μm *157 μm. Capacitors of C1 to C4 have been designed using metal layers of one to four, using finger-based architecture [26]. Total area occupied for each capacitor is 20 μm *21 μm. Poly silicon resistors are also utilized with narrow layers of poly silicon shaped in a way to form the desired resistance.

For phase noise reduction and chip size minimization, finger-based layout has been utilized for transistors. Each gate is divided into number of fingers, which are utilized symmetrically between cascade transistors. Using this method with poly silicon resistors, the active inductor layout is designed as shown in Figure 56.

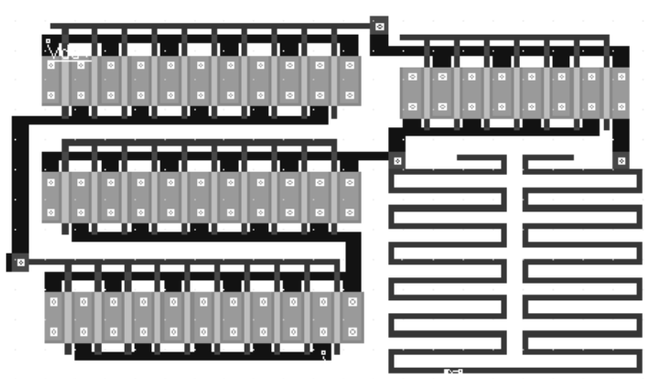


Fig. 56. Active inductor layout

Symmetric finger-based design typically helps in 10% chip size reduction. Total occupied die area is 0.22mm² as shown in Figure 57.

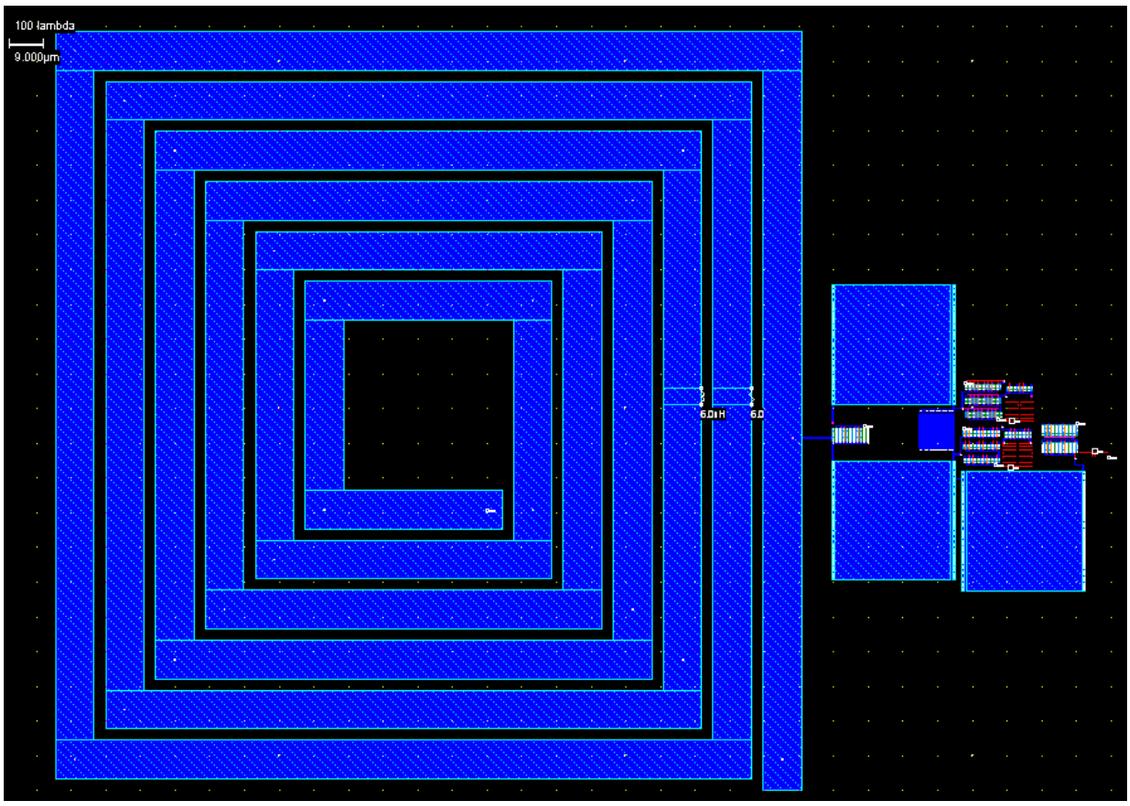


Fig. 57. VCO Circuit layout

1.12.3.7 Phase Noise Reduction

The noise reduction techniques were described in Section 1.11. First, the Noise filtering technique [28] is employed here. This implies LC resonating networks in the sources of M1 and M11, instead of directly connecting them to ground, as shown in Figure 58.

The frequency of oscillation for LC networks is 2GHz. This helps in turning the NMOS off rapidly and having a positive impact on the phase noise. Simulation in this case shows 3dBc/Hz improvement in the phase noise, reducing it to -93.7dBc/Hz from -91.01dBc/Hz at the frequency of 4GHz and the offset of 1-MHz. Although this limits the frequency tuning range, it can be used as a good technique for noise reduction when narrower frequency range is required.

As explained above, another technique for noise suppression is given in [29], in which a frequency to current converter extracts the noise properties of VCO output signal. This extracted current then passes through an integrator, which will converts it to a voltage carrying important noise and frequency properties. This voltage will enter a low pass filter and fed back as an input voltage to the oscillator.

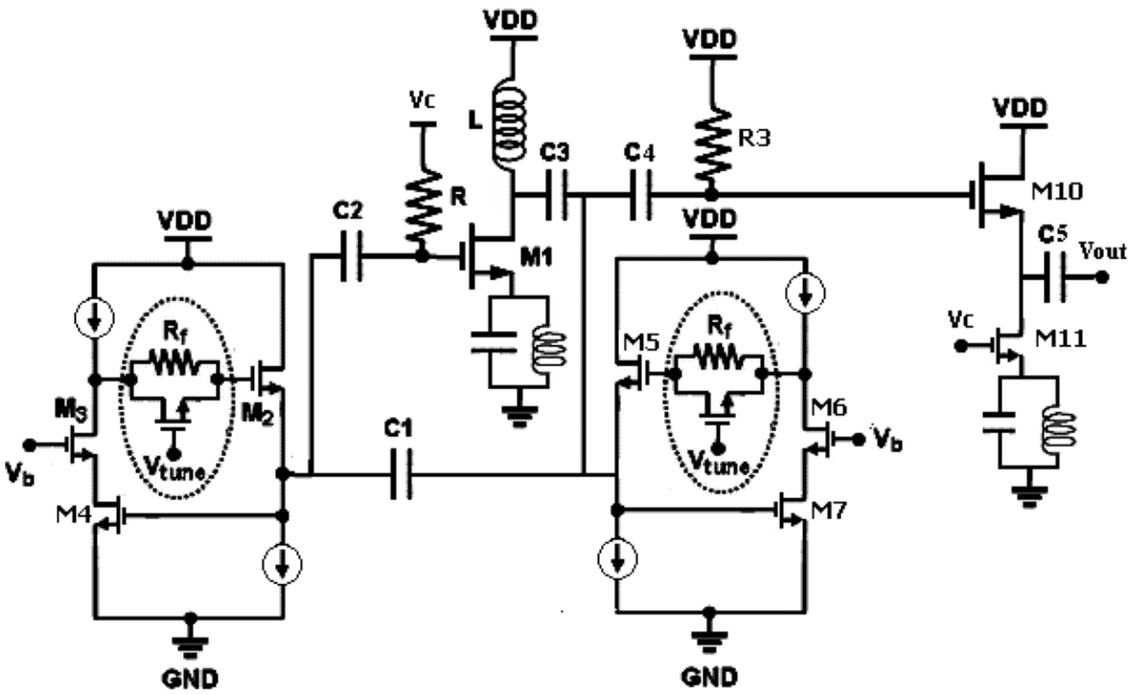


Fig. 58. Noise filtering technique

Although this method has been tested for ring oscillators [34] and shows a significant decrease in phase noise, here we obtain only 1dBC/Hz improvement for UWB oscillator. Characteristics of the proposed VCO and also a number of previously simulated oscillators are shown in Table 2 and Table 3, respectively. Comparison with similar designs illustrates a wider tuning range with better noise performance and gain factor for the UWB oscillator presented in this section.

Technology	0.18 μ m CMOS Technology
Power supply	1.8V
Bias current	17.21mA
Power Dissipation	29.1mW
Frequency Range	3.8GHz ~ 7.4GHz
Phase noise	-92.05 ~ -75.42 dBc/Hz @1MHz

Table 2. brief characteristics of proposed VCO

Year	Freq. range GHz	K_{VCO} (MHz/V)	Process	Ref.
2001	4.20 ~ 5.05	340	0.25um	[35]
2005	2.70 ~ 5.40	1687	0.18um	[30]
2005	0.50 ~ 2.0	500	0.18um	[27]
2005	1.14 ~ 2.46	270	0.18um	[7]
2005	1.90 ~ 2.19	116	0.18um	[34]
2007	3.80 ~ 7.40	2400	0.18um	[19]

Table 3. comparison with Previously simulated VCOs

1.13 Summary

This chapter has explored the techniques for VCO design with wide tuning range. An overview of various wideband tuning solutions proposed in the literature and the associated design challenges have been discussed. Wideband (Ultra Wideband) oscillators can be realized by carefully designing passive and active devices. The techniques for sizing and layout design of active and passive elements are discussed to optimize the phase noise performance of oscillators. The feasibility of CMOS VCO capable of multi-GHz operation has been demonstrated. The performance of the VCOs highlight the higher tuning ranges achieved in the case of inductive tuning. The VCO based on inductive tuning, realized by the tunable active inductor (TAI) using a 0.18μm CMOS technology, can provide a tuning range between 0.5–2.0 GHz and 3.8-7.4GHz using Colpitts and Hartley structures, respectively. Also, it is shown that with phase noise reduction techniques such as PLL-based feedback and harmonic tuning, the phase noise can be improved for 1-3dB.

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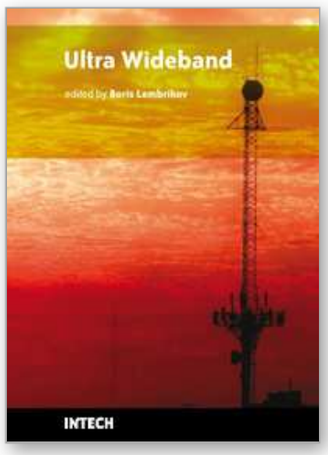

Ultra Wideband

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Ultra wideband technology is one of the most promising directions in the rapidly developing modern communications. Ultra wideband communication system applications include radars, wireless personal area networks, sensor networks, imaging systems and high precision positioning systems. Ultra wideband transmission is characterized by high data rate, availability of low-cost transceivers, low transmit power and low interference. The proposed book consisting of 19 chapters presents both the state-of-the-art and the latest achievements in ultra wideband communication system performance, design and components. The book is addressed to engineers and researchers who are interested in the wide range of topics related to ultra wideband communications.

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