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Progress Toward Nanowire Device Assembly Technology

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1. Introduction

The advancement of integrated circuits (ICs) has been following Moore's Law well since 1960s. For the sustaining of Moore's Law, technologists in the microelectronics industry are, on one hand, trying to push lithography technology to the limit for making devices with smaller length scales. Extreme ultraviolet, e-beam, nanoimprint or other lithography technologies have been developed as candidate replacement technologies for the conventional optical lithography (Gwyn et al., 1998; Vieu et al., 2000; Chou et al., 1996). On the other hand, technologists are also exploring the third dimension for the 3D integration of chips (Baliga, 2004). Although the advancement of lithography technologies and 3D integration technology can keep the IC industry abreast of Moore's Law for the next decade, the problems we will face at the end of that period are becoming visible. The emerging of nanowires/nanotubes as building blocks of ICs will bring fundamental changes to the future IC industry and offer continuance of Moore's Law. Besides the applications in logic circuits, nanowires have very promising applications as sensing elements in highly sensitive bio/chemical/photon sensors and detectors.

Nanowires are commonly grown by vapor-liquid-solid (VLS) process (Wagner & Ellis, 1964), vapor-solid (VS) process (Zhang et al., 1999), electrochemical deposition into nanoporous templates (Sander et al., 2002), and solution growth (Govender et al., 2002). In the past 20 years, nanowires of a diverse range of compositions have been produced at a relatively low cost with precisely controlled parameters including structure, size, defect, and doping. Nanowire devices such as field effect transistors (FETs) (Ju et al., 2007), single virus detector (Patolsky et al., 2004), pH sensor (Cui et al., 2001), gas sensors (Zhang et al., 2004), and photodetectors (Soci et al., 2007) have been demonstrated to show superior performance than their thin-film counterparts or even exhibit novel properties that have never been achieved by thin-film technology. However, most of the nanowire devices are limited to the demonstration of single device, not adequate for production on a large scale at low cost. Ultimately, cost and yield will decide whether nanowire devices find their way into market. Developing cost-effective means to integrate nanowires into working devices on large scales is essential for the prosperity of nanotechnology. In this chapter, we focus on progress toward nanowire device assembly technologies, which may benefit for the mass production of nanowire devices in the future. Generally, two strategies exist for the fabrication of devices from nanowires, namely, transfer pre-grown nanowires onto a surface with

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alignment and direct growth of nanowires onto a substrate at desired locations. Examples of nanowire devices demonstrated by these two strategies are given. It should be noted that although the assembly techniques described here are for nanowires, in most of the cases, they can also be applied to other 1D nanostructures, such as nanorods, nanotubes, and nanobelts.

2. Transfer with alignment

While manipulating atoms is still a dream to be realized in future nanotechnology, manipulating an assembly of them, such as nanowires, is a tough but possible task at current stage. At the early stage of nanowire research, nanowire devices are commonly made by "pick and place" method (Cui & Lieber, 2001). Nanowires grown by bottom-up process are removed from their substrates and suspended into a solution. Then, nanowires are dispersed randomly onto another substrate. Before nanowire dispersion, markers are made on the substrate, so that the position and angle of the nanowires can be noted under SEM observation. Next, a lift-off process is applied to pattern metallic contacts to the nanowires. This method is suitable for studying fundamental properties of the nanowires because the structure is well defined (Keem et al., 2006). However, it is complicated and costly and, therefore, not suitable for production. In some other cases, the metal electrodes are made before nanowire dispersion (Kind et al., 2002). Successful placement of nanowires between the pre-fabricated electrodes requires luck and the contact barriers between the electrodes and the nanowires are usually very high, which make the technique non-reproducible and not suitable for many device applications. The assembly of many individual nanowires over large areas with controlled directions and interspacing is desired for the fabrication of complex circuits of nanowires with logic functions. In this section, we concentrate on techniques that have been developed to transfer pre-fabricated nanowires and align them parallel with each other on substrates where standard lithographic processes can be applied to fabricate devices.

2.1 Alignment with fluid flow in microchannels

The shear force created by the motion of a fluid against a solid boundary can be used to align nanowires that are suspended in a solution. The nanowires will reorient to the direction of the fluid flow to minimize the fluid drag forces. The shear forces from the evaporation of a droplet can align nanowires, but the resulting pattern is a ring because the nanowires dispersed in the drop are advected to the contact line (Deegan, 2000). By flowing a stream of fluid across a substrate surface, nanowires can be reoriented towards the flow direction and become quasi-aligned (Wang et al., 2005a). A better technique to align nanowires with fluid flow is to confine the fluid flow to a microfluidic channel (Huang et al., 2001a). The microchannel can establish a shear force that is more uniform than the previous techniques. In this flow assembly technique, a poly(dimethylsiloxane) (PDMS) mold with a microchannel with width ranging from 50 to 500 μm and length from 6 to 20 mm is brought into contact with a flat substrate. Parallel nanowire arrays are achieved by flowing a nanowire suspension inside the microchannel with a controlled flow rate for a set duration. The degree of the alignment can be controlled by the flow rate: the angular distribution of the nanowires narrows substantially with increasing flow rates. The nanowire density increases systematically with the flow duration. High-performance p-Si nanowire transistors have been demonstrated using this fluid flow alignment technique (Duan et al., 2003).

The ability to assemble nanowires into complex crossed structures makes this technique more interesting for building dense nanodevice arrays. Crossed nanowire arrays can be obtained by alternating the flow in orthogonal directions in a two-step flow assembly process. An equilateral triangle of nanowires can be obtained in a three-step assembly process, with 60^o angles between flow directions. The important feature of this layer-by-layer assembly scheme is that each layer is independent of the others and, therefore, a variety of homo- and hetero-junctions can be obtained at the crossed points. By using nanowires with different conduction types (e.g., p-Si and n-GaN nanowires) in each step, the authors have demonstrated logic gates with computational functions from the assembled crossbar nanowire structures (Huang et al., 2001b). The weakness of this technique is that the area for nanowire alignment is limited by the size of the fluidic microchannels. It will be more difficult to establish a uniform shear force in a large channel.

2.2 Alignment by interactions with chemically patterned surfaces

Nanowires deposited on a substrate from a suspension have random orientations. The deposition site of the nanowires strongly depends on the surface chemical functionality. The deposition sites can be controlled through van der Waals and hydrogen bonding interactions between the nanowires and the chemically functionalized substrate. Selective deposition of nanowires onto the chemically patterned area can be achieved under proper deposition conditions. One common technique to achieve such interactions is through the hybridization of complementary DNAs (Mbindyo et al., 2001; Lee et al., 2007b), which is well established in biology. A suspension of nanowires whose surface is modified with single-stranded DNA (ssDNA) is cast onto a substrate patterned with the complementary DNA (cDNA) strands and polyethylene glycol (PEG) (Wang & Gates, 2009). Nanowires deposit on the areas that are patterned with cDNA through hybridization of ssDNA with cDNA, but not on the surfaces that are passivated by PEG. This assembly technique has also been exploited for bridging nanowires across two electrodes by selective DNA hybridization (Lee et al., 2007b). The assembled nanowires show ohmic contact with minimum contact resistance, which proves this is an effective way for nanowire assembly. Similar approaches to enhance the interaction between the nanowires and the substrate include using biotin-avidin linkages (Chen et al., 2006), block-copolymer modifications (Nie et al., 2007), and hydrophobic/hydrophilic surface modifications (Ou et al., 2008). Future works should focus on improving the efficiency of the nanowire-substrate interaction and on using this technique to make ordered and patterned nanowire arrays.

Although selective deposition of nanowires can be achieved by this surface modification technique, the nanowires are not aligned after the assembly process. The alignment is driven largely by the shear force during solvent evaporation. To solve this problem, Huang et al. have combined the surface modification technique with the flow assembly technique introduced above to obtain periodic aligned nanowire arrays (Huang et al., 2001a). The SiO_2/Si substrate is patterned with NH_2-terminated monolayers in the shape of parallel stripes with a separation of a few micrometers. During the flow assembly process, the nanowires are preferentially attracted to the NH_2-terminated regions of the surface. The orientation of the nanowires is controlled by the shear force generated from the fluidic flow in the microchannels. Controlling both the location and orientation of the nanowires is therefore realized.

2.3 Alignment by Langmuir-Blodgett technique

When a solid surface is vertically dipped into a liquid containing a Langmuir monolayer and then pull out properly, the monolayer will deposit homogeneously onto the surface. This process creates Langmuir-Blodgett (LB) films. The LB technique is usually used to transfer organic monolayer from water onto a solid substrate to form extremely thin films with high degree of structure order. This technique can also be applied to prepare LB films of nanowires if the materials for assembly meet the following requirements: 1) soluble in water-immiscible solvents; 2) formation of stable floating monolayers at the surface of the subphase with internally oriented, cohesive, and compact structure that are sheer resistant. To meet these requirements, the nanowires used to form LB films are usually functionalized by surfactants. Without functionalization, the nanowires do not form stable suspensions in the organic solvents and sink into water. The process of the LB technique is illustrated in Fig. 1a. A nanowire-surfactant monolayer is initially formed on a liquid (usually water) surface in an LB trough. The monolayer is then compressed using the barrier under an appropriate level of compression. The nanowires are close-packed as parallel arrays with their longitudinal axes aligned perpendicular to the compression direction to minimize the surface energy of the liquid. The formed nanowire monolayers resemble a microscopic version of "logs-on-a-river". The monolayer of the aligned nanowires is then transferred onto a substrate through vertical-dipping (i.e., LB) or horizontal-lifting (i.e., Langmuir-Schaefer (LS)) techniques. The spacing between the parallel nanowires can be adjusted by the lifting speed and by the pressure of the compression.

The LB technique has so far been adopted by many researchers to assemble various nanowires in large scales. Tao and coworkers used the LB technique to assemble aligned monolayers of silver nanowires that are ~50 nm in diameter and 2-3 μm in length over areas as large as 20 cm^2 (Tao et al., 2003). The SEM images of the resulting Ag nanowire arrays on a Si wafer are shown in Fig. 1b-c. The Ag nanowire monolayers serve as excellent substrates for surface-enhanced Raman spectroscopy with large electromagnetic field enhancement factors.

Other aligned nanowire monolayers are also realized using the LB technique, including Ge nanowires (Wang et al., 2005b), ultrathin (~1.3 nm in diameter) ZnSe nanowires (Acharya et al., 2006), V_2O_5 nanowires (Park et al., 2008), and VO_2 nanowires (Mai et al., 2009). Whang et al. used the LS technique to transfer Si nanowire monolayers on a 1 cm × 3 cm substrate (Whang et al., 2003). The spacing of the transferred nanowires is controlled from micrometer scale to well-ordered and close-packed structures by the compression process, as shown in Fig. 1d-f. Using the LS assembly of Si nanowire arrays, they have also fabricated FET arrays over large areas without the need to register individual nanowire-electrode interconnects (Jin et al., 2004). The non-registration integration method is very useful because it can also be applied to nanowire arrays assembled by other methods. The ability to assemble hierarchical nanowire structures makes the LB and LS techniques more interesting. Hierarchical structures are produced by repeating the assembly process after changing the orientation of the substrate (Whang et al. 2003; Acharya et al., 2006). The challenges of the LB and LS techniques are the aggregation of nanowires in the Langmuir monolayer and the reorientation of nanowires during the post processes. The applications of LB techniques for the assembly of nanomaterials including nanoparticles, nanorods, nanowires, nanotubes, and nanosheets have been well summarized in a recent review (Acharya et al., 2009).

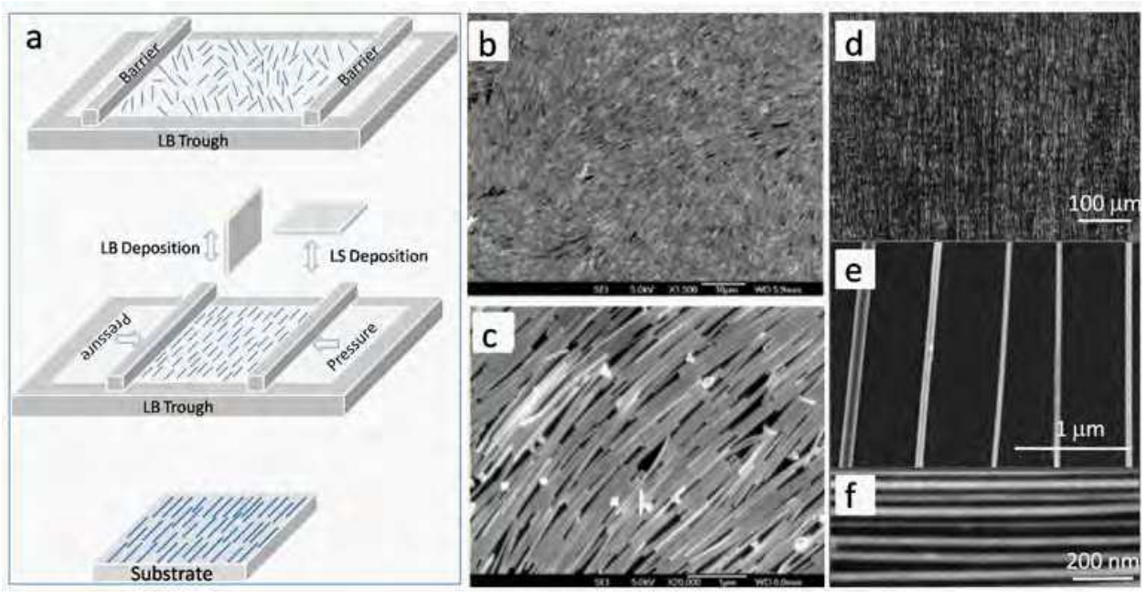

Fig. 1. Alignment of nanowires by LB and LS techniques. (a) Schematic processes of the LB and LS techniques. (b & c) SEM images of an LB assembly of Ag nanowires. Reprinted with permission from (Tao et al., 2003), © 2003 American Chemical Society. (d-f) SEM images of an LS assembly of Si nanowires. Reprinted with permission from (Whang et al., 2003), © 2003 American Chemical Society.

2.4 Electric and magnetic fields assisted orientation

For nanowires with an inherent charge or modified to adopt a specific charge, electrostatic interactions between the nanowires and patterned substrates can be used for nanowire assembly (Myung et al., 2005). The process is similar to the nanowire assembly using chemically patterned surfaces. Nanowires can also be aligned with the assistance of external electric and magnetic fields. The process for the alignment of nanowires in a fluid under electric field is called dielectrophoresis (DEP) assembly of nanowires. The dielectrophoretic forces which arise from induced dipole moments embedded in nonuniform electric fields are widely used to manipulate micro and nanoscale particles. The structures align with a minimum energy configuration within the applied field, such as along the field lines. In practice, electrodes with proper gap distances are fabricated by lithography on the substrate for DEP. Nanowire dispersion is dropped onto the substrate and a direct current (dc) or an alternating current (ac) electric field is applied to the electrodes. The density of the assembled nanowires can be controlled from a dense array of nanowires (Zhou et al., 2007) to a single nanowire (Duan et al., 2001). The density of the nanowires is generally increased with the increase in the applied voltage or with the decrease in the gap distance, that is, with the increase in the applied electric field. In the cases of ac electric field, the nanowire assembly becomes tighter, straighter, and more uniformly aligned as the frequency increases (Wang et al., 2007). A gate voltage is also used to control the deposition position of the nanowires (Wang et al., 2007). Due to the large geometric aspect ratio of nanowires, the induced dipole of the nanowires is proportional to their conductivity. Therefore, the DEP assembly works well with metallic nanowires (Smith et al., 2000). For semiconducting nanowires, super-band-gap illumination has been used to increase their conductivity, which

results in an increase in the wire DEP mobility (Zhou et al., 2007). Theoretical understanding of the DEP assembly has also been done for further improving this technique (Liu et al., 2006). The weakness of the technique is the need of prefabricated electrodes for nanowire assembly and the reorientation and aggregation of the nanowires upon evaporation of the solvent.

For magnetic nanowires (e.g., Fe, Co, and Ni), a magnetic field can be applied to align them in a liquid. The nanowires align along the magnetic field lines. Pre-fabricated ferromagnetic microelectrodes on substrates provide an additional degree of control, dominating dipole interactions among nanowires, for site-specific assembly (Hangarter et al., 2007; Yoo et al., 2006). Magnetic nanowires can be effectively trapped on templates with nanomagnet arrays under a low external magnetic field if magnetic charge and dimension are matched between the magnetic nanowires to be assembled and the gaps between the two nanomagnets (Liu et al., 2007). Nonmagnetic nanowires can be capped with magnetic ends and assembled using magnetic field (Hangarter & Myung, 2005). The field gradients can also control the alignment of nonmagnetic nanowires immersed inside magnetic fluids (Ooi & Yellen, 2008). Due to the competition between a preference to align with the external field and a preference to move into regions of minimum magnetic field, the nanowires align perpendicular to the external field at low field strengths, but parallel to the external field at high field strengths. Magnetic nanowires assembled in conjunction with micropatterned magnet arrays have been demonstrated to be a flexible tool for manipulation and positioning of mammalian cells (Tanase et al., 2005). One major problem for the magnetic assembly is the lateral aggregation and edge accumulation of the nanowires. The concentration of nanowires in the solution and the applied magnetic field are very important parameters in reducing these problems (Hangarter et al., 2007).

2.5 Alignment in blown bubble films

Another technique for large-scale assembly of nanowires is using shear force created by the expansion of a blown-bubble film (Yu et al., 2007). Blown film extrusion is a well-developed process for the manufacture of plastic films in large quantities. Yu et al. applied this technique to the formation of nanocomposite films where the density and orientation of the nanowires were controlled within the films. The basic steps in their approach consist of (1) preparation of a homogenous, stable, and controlled concentration polymer suspension of nanowires; (2) expansion of the polymer suspension using a circular die to form a bubble at controlled pressure and expansion rate; (3) transfer of the bubble film to substrates or open frame structures. The nanowires within the film align along the shear force created by the expansion of the film. More than 85% of the nanowires are aligned within ±6° of the upward expansion direction. Si nanowires are transferred conformally to single-crystal wafers up to 200 mm in diameter, flexible plastic sheets up to 225 mm × 300 mm, highly curved surfaces, and also suspended across open frames. The nanowire density within the film can be controlled by the concentration of the nanowire in the polymer suspension. Large nanowire FET arrays were also fabricated using transferred Si nanowire blown-bubble films. The limitation of this method lies in the necessity to embed nanowires in the bubble films which result in contamination of the nanowires and degradation of their performance. Also, excess epoxy matrix should be removed using processes such as reactive ion etching before the fabrication of nanodevices.

3. Integration by direct growth

Even though the transfer techniques allow one to align nanowires and control the position to a certain degree, their need for transfer media in most cases liquid, poses potential harm to the unique properties of the nanowires. Especially when the surface cleanness of the nanowires are critical to the performance of devices (such as detectors and sensors), reducing or eliminating post-processing of the nanowires is necessary. In this respect, integration of nanowires into devices on desired locations by direct growth possesses apparent advantage over the transfer methods. The synthesis methods can be modified to achieve selective growth of nanowires on desired locations by patterning of catalysts/seeds. Both vertical and planar integration of nanowires with respect to the substrate are possible. In this section, examples are given on the direct growth strategy for nanowire device integration.

3.1 Direct growth of vertical nanowire arrays

The simplest example of this strategy that can be given is the growth of vertically aligned nanowire arrays for application in devices such as nanolasers (Huang et al., 2001), light-emitting diodes (LEDs) (Könenkamp et al., 2004; Lai et al., 2008), and solar cells (Law et al., 2005). Starting with a substrate covered by nanosized catalysts or seeds, vertically aligned nanowires are grown on top of it by either vapor phase or solution growth methods. The substrate is chosen to have a good lattice match with the nanowires so that the nanowires can be epitaxially grown from the substrate to achieve better alignment. Depending on the purpose, post-treatments of the nanowire array may be necessary for the final device.

For laser applications, the nanowires are optically pumped and laser emission is observed when the excitation intensity exceeds a threshold. The lasing threshold is much lower than those for random lasing obtained in disordered particles or thin films. The vertically aligned nanowires serve as natural resonance cavities, so that lasing action is observed in the nanowire array without any fabricated mirrors.

For LED applications, the nanowires should be grown from a thin film with different conduction type to form p-n junction. To protect the nanowires and to form a buffer layer between the thin film, the nanowire array is buried in spin-on glass (Luo et al., 2006) or in high-molecular-weight polymers such as polystyrene (PS) and poly(methyl methacrylate) (PMMA). After etching the insulating layer on top of the nanowire array, ohmic contacts are formed on the thin film and on the exposed nanowire tips. Similar process has been proposed recently as a generic approach for vertical integration of nanowires (Latu-Romain et al., 2008). Electroluminescence is observed under a forward bias, which originates from the recombination of minority carriers that are injected across the junction between the thin film and the nanowire array. The vertical nanowire architecture of the device leads to waveguided emission, which is one of the advantages of using a vertical nanowire array over a thin film. Similar device architecture has been realized recently using InAs vertical nanowires on Si substrate for photovoltaic and photodetection applications (Wei et al., 2009).

Vertical nanowire arrays are also used to construct the anodes of dye-sensitized solar cells (DSCs) to replace anodes made by thick films and nanoparticles. Vertical nanowire arrays are grown on a transparent conductive substrate, dye-coated, sandwiched together and then bonded. The internal space of the cell is filled with a liquid electrolyte by capillary action. The nanowire anode features a large surface area as well as direct electrical pathways which

ensure rapid collection of carriers generated throughout the device, which promotes high device efficiency. Although nanoparticle DSCs offer larger surface area, they rely on trap-limited diffusion for electron transport, a slow mechanism that can limit the device efficiency.

3.2 Patterned growth of vertical nanowires

Above devices are made using dense nanowire arrays without precisely controlling the locations of the nanowires. Although this technique offers the advantage of simplicity and low cost in the fabrication process, the alignment of the nanowires, far from ideal, presents a certain degree of randomness. Controlling the density, position, and arrangement of the nanowires is of great interest for most applications in nanoelectronics, nanophotonics, and optoelectronics. The patterned growth of nanowires in a periodic fashion over a large scale (square-centimeter and above) by inexpensive methods is highly desired. This is realized using patterned arrays of metal nanodots as catalysts made by nanopatterning techniques. The nanowires would copy the pattern of the metal nanodots due to the selective growth of nanowires via the VLS process. Existing nanopatterning techniques include photolithography (Greyson et al., 2004), e-beam lithography (Ng et al., 2004), nanosphere lithography (Fuhrmann et al., 2005; Zhou et al., 2008), nanoimprint lithography (Martensson et al., 2004), and nanoporous mask patterning (Fan et al., 2005). The nanowires are usually grown by CVD, MOVPE, MOCVD, and MBE. The patterned growth of vertical nanowires has been realized with various semiconductors, such as Si, InP, InAs, ZnO, and GaN. The key advantages of this technique are that the diameter, height, orientation, and location of the nanowires can all be controlled. For more details about the patterned growth of semiconductor nanowires, readers can refer to an extensive review given by (Fan et al., 2006) and the references therein. Here, we will focus on the applications of these patterned nanowires for device assembly.

One demonstrative device using highly ordered vertical nanowires is the nanowire vertical surround-gate field-effect transistor (VSG-FET). This device was first realized by (Ng et al., 2004) using an array of individual ZnO nanowires. By patterning Au catalyst pads with diameter of ~180 nm and thickness of ~1.5 nm using e-beam lithography, a single ZnO nanowire with an average diameter of ~35 nm was grown at each catalyst spot in the CVD process. A heavily doped SiC was used as the device substrate because the SiC (0001) plane has very small lattice mismatch (~5.5%) between the ZnO (0001) which facilitates epitaxial growth of vertically aligned ZnO nanowires and its high conductivity offers bottom electrical contacts to the nanowires. Fig. 2a-f show a generic process flow for the fabrication of a functional VSG-FET. A 3D schematic cartoon and a FE-SEM cross-sectional image are shown in Fig. 2g-h. In principle, similar fabrication schemes can be used with other nanowire/substrate combinations. Similar strategy has been employed for the realization of a VSG-FET using Si nanowire grown epitaxially by CVD on a (111)-oriented p-type Si substrate (Schmidt et al., 2006). The surround gate allows better electrostatic gate control of the conducting channel and offers the potential to drive more current per device area than is possible in a conventional planar architecture (Wang et al., 2004). 1D nanowires obtained using the bottom-up approach completely eliminate the lithography and etching processes typically employed in the top-down approach to obtain nanopillars (Endoh et al., 2003). Direct integration of the vertically aligned nanowires using current semiconductor processing technology bridges the gap between microtechnology and nanotechnology.

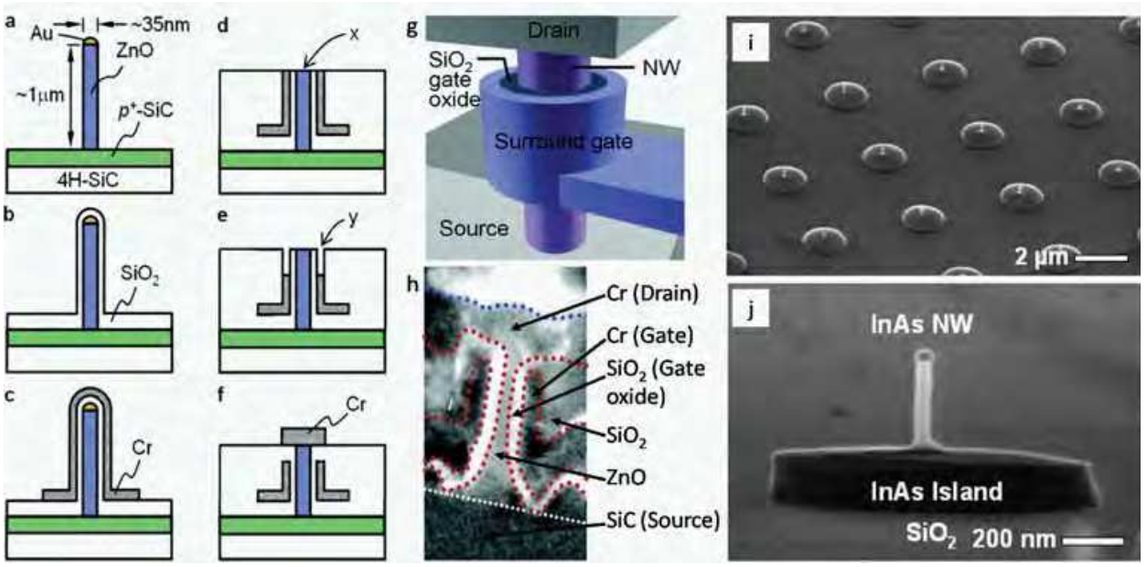

Fig. 2. (a-f) Schematics of a process flow showing the major steps to fabricate a ZnO nanowire VSG-FET. (g) A 3D schematic illustrating the critical components of the device. (h) SEM cross-sectional image of the vertical surround-gate FET. Reprinted with permission from (Ng et al., 2004), © 2004 American Chemical Society. (i-j) SEM images of vertical and electrically isolated InAs nanowires on SiO_2/Si. Reprinted with permission from (Dayeh et al., 2008), © 2008 American Institute of Physics.

The processes in the two examples given above are designed only for single device demonstration. The presence of the underlying semiconducting substrate precludes electrical isolation and individual addressability of single nanowire. For practical applications, addressable patterned underlying electrical contacts are needed. Dayeh and co-workers (Dayeh et al., 2008) tried to address this problem by a layer transfer technique that combines hydrogen ion implantation and wafer bonding, known as ion-cut or Smart-cut® process (Bruel, 1995). A thin InAs layer is transferred onto SiO_2/Si by Smart-cut® technique and ordered InAs nanowires are epitaxially grown on the layer by MOVPE. After nanowire growth, the InAs layer in the regions between the nanowires is etched resulting in an ordered, vertical, and electrically isolated InAs nanowire array as shown in Fig. 2i-j. Combining this technique with the VSG-FET technique would result in the realization of individually addressable, high density VSG-FET arrays suitable for 3D circuit applications.

Nanowires and nanotubes have been proved to exhibit excellent field emission properties due to their high aspect ratio and tip-like shape which maximize the geometrical field enhancement (Au et al., 1999; Wong et al., 1999; Nilsson et al., 2000). Another important device demonstrated using site-determined vertical nanowires is the self-aligned, gated arrays of individual nanotubes/nanowire emitters (Gangloff et al., 2004). The fabrication process of the device is shown in Fig. 3a-d. A resist hole is first patterned on a gate electrode/insulator/emitter electrode sandwich. The gate and insulator are then isotropically etched. A thin film of catalyst and a barrier layer are deposited on the structure. A lift-off process is performed to remove the unwanted catalyst on top of the gate followed by the growth of nanowire/nanowire inside the cavity. The gated nanotube cathode array has a low turn-on voltage of 25 V and a peak current of 5 μA at 46 V, with a

gate current of 10 nA, which corresponds to a gate transparency of ~99%. These low operating voltage cathodes are potentially useful as electron sources for field emission displays or miniaturizing electron-based instrument.

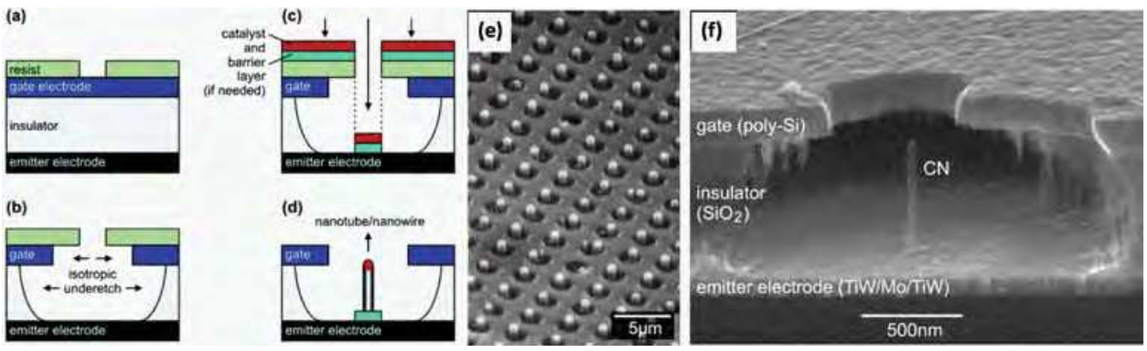

Fig. 3. (a-d) Schematics of the self-aligned process for fabricating individual nanowire/nanotubes emitters with integrated gates. (e) An array of integrated gate Si nanowire cathodes. (f) Cross-sectional view of an integrated gate carbon nanotube cathode. Reprinted with permission from (Gangloff et al., 2004), © 2004 American Chemical Society.

3.3 Direct growth of horizontally aligned nanowires

The growth of vertically aligned nanowires can be easily achieved if the substrate is terminated with a surface which allows epitaxial growth of the material and the crystal orientation of the surface matches the fast growth direction of the nanowires. The growth of horizontally aligned nanowires is, however, not easily achieved and less studied. Horizontally aligned nanowires offer a benefit of fabricating integrated nanodevices. As we discussed before, most of the works focus on the transfer of nanowires with alignment to a different substrate. It would be better if nanowires could be grown horizontally on desired locations of the substrates.

Nikoobakht has proposed a method to grow horizontally aligned nanowires on desired locations and directions (Nikoobakht, 2007). In this architecture, nanowires are grown where the nanodevices will later be fabricated on. Gold nanodroplets are first patterned on an α-plane ($11\bar{2}0$) sapphire substrate. ZnO nanowires with diameter of ~10 nm are then grown selectively on the predefined gold sites. The growth direction of the nanowires is controlled using the anisotropic crystal match between ZnO and the underlying substrate. Subsequently, metal electrodes are deposited on nanowires at once and in a parallel fashion. Large numbers of top-gated ZnO nanowire field-effect transistors are fabricated using only three photolithographic steps. The advantages of this technique are: 1) the starting coordinates of the horizontally grown nanowires are defined; 2) the number of nanowires in each device is controlled; and 3) the technique is scalable and therefore capable of industrial production. The horizontally grown nanowires have also been utilized to integrate horizontal nanochannels with known registries to microchannels (Nikoobakht, 2009).

Horizontally aligned GaAs nanowires have also been realized on GaAs (100) substrates using atmospheric pressure MOCVD with Au as catalyst (Fortuna et al., 2008). GaAs nanowires with diameter of ~30 nm and length of several microns are grown in plane in either the $[1\bar{1}0]$ or $[\bar{1}10]$ direction axially at 460-475 °C. The spacing between the adjacent planar nanowires can be controlled by the density of the gold catalysts. The drawback of

this method is that the nanowires are grown on conducting substrates. Therefore they cannot be directly integrated into nanodevices. To solve this problem, the authors have applied a direct transfer process to the nanowires. The position and alignment of the nanowires are maintained after the transfer process, which makes possible the nanowire integration afterwards.

A general method for growing laterally aligned and patterned ZnO nanowire arrays on any flat substrate is also proposed (Qin et al., 2008). The nanowires are grown by a solution based growth process, in which the orientation control is achieved using the combined effects from a ZnO seed layer and a catalytically inactive Cr (or Sn) layer for nanowire growth. Because the growth temperature is low (<100 °C), the method can be applied to any substrate. However, the alignment of the nanowires should be improved for device applications such as FETs. Xu et al. recently achieved highly ordered horizontal ZnO nanowire arrays using a hydrothermal decomposition method onto the $[2\bar{1}\bar{1}0]$ surface of a single crystal ZnO substrate (Xu et al., 2009). However, the diameter of the nanowires is quite large (> 400 nm) and increases with the length of the nanowire. It is apparent that there is much work to do in this area before the techniques can benefit to practical applications.

3.4 Nanowire integration by bridging method

For horizontally aligned nanowires obtained either by a transferring method or by a direct growth method, electrodes are made on top of the nanowires afterwards. The post processing usually introduces contamination to the nanowires, which may deteriorate the performance of the nanodevices. Especially, keeping the nanowire surface clean is of significant importance for nanowire sensors and detectors. A solution for this would be to grow nanowires from one desired location directly to another desired location, such as between two electrodes. Nanowires bridge two desired locations in the "bottom-up" process, therefore this technique is called "bridging method". In this method, a substrate is etched to form two electrode posts using microfabrication process. Catalysts or seed layers are then deposited on the side walls of the posts. Nanowires are grown across the trench between the electrode posts and form bridges in a VLS process. Since the electrode posts are fabricated prior to the growth of nanowires, surface contamination is minimized. The nanowire integration process is also more efficient than the former methods. The bridging method was first demonstrated by Haraguchi and coworkers by growing GaAs nanowhiskers across a trench between GaAs posts (Haraguchi et al., 1996; Haraguchi et al., 1997). Although the bridging nanowhiskers in this architecture cannot be used for electrical characterization because the substrate between the two posts is conductive, it shows the potential to directly integrate an ensemble of nanowires on-chip. In recent years, this technique has been used to fabricate bridging nanowire devices such as gas sensors, photodetectors, and transistors with Si, GaN, and ZnO. Some representative works are given below.

Because of silicon's compatibility with existing IC process, Si nanowires are especially attractive. Using the vast knowledge of Si technology, the Hewlett-Packard (HP) group first demonstrated ultrahigh-density Si bridging nanowires across a trench etched into a (110)-oriented Si wafer (Islam et al., 2004). The sidewalls of the trench are (111) planes, on which Si nanowires grow vertically to the surface. The bottom of the trench is still conductive in this case. However, this problem can be easily solved by using a silicon-on-insulator (SOI)

wafer. The trench is etched into the SOI until reaching the buried insulator layer. By using Si bridging nanowires grown on an SOI wafer, the HP group has realized a gas sensor and proposed a concept for using bridging nanowires to build a sensor system (Kamins et al., 2006).

A typical process for the fabrication of Si bridging nanowires on an SOI is as follows. SOI wafers consisting of a 20-80 μm thick Si(110) layer, a 0.5-2 μm thick thermally grown SiO_2 layer, and a ~400 μm thick Si(100) handle layer are used as the substrates. A 0.5-1 μm-thick thermal SiO_2 layer is first grown on the Si(110) surface and patterns designed for trenches are made by photolithography and transferred onto the SiO_2 layer by plasma etching. The trenches are made by DRIE process using the patterned SiO_2 layer as a mask. The SiO_2 mask is removed by wet etching afterwards. Gold colloids are dispersed on the substrate at catalysts for VLS growth of nanowires. Si bridging nanowires are then grown by CVD. In this process, the lengths, diameters, and densities of the bridging nanowires can be controlled. The lengths of the nanowires can be tailored to fit in trenches of varying widths by controlling the growth time. The diameters of the nanowires can be defined by the sizes of the Au colloids. The density of the nanowires in the trenches can be controlled by the surface density of the Au colloids. Using a single Si bridging nanowire fabricated by this process, giant piezoresistance effect was demonstrated (He & Yang, 2006).

Apart from Si bridging nanowires, other compound semiconductors can also be fabricated into a bridging architecture. GaN bridging nanowires are fabricated using a similar process (Chen et al., 2008). A wafer with a ~2-μm-thick layer of highly n^+-doped c-plane GaN on sapphire is used as the substrate for fabrication of the bridging nanowire device. Ni electrodes with thickness of 0.2-0.4 μm are patterned on the substrate by photolithography and lift-off. The trenches are then made by RIE using the patterned Ni electrodes as a mask. To ensure the electrical isolation between two electrodes, the n^+- GaN layer is over-etched down to the sapphire surface. After sputtering a thin (< 10 nm) layer of Au catalyst, GaN nanowires are grown by CVD to bridge the electrodes. The formed nanobridge device shows a linear *I-V* characteristic in dark, which suggests that there is no contact barrier between the electrodes and the bridging nanowires. The device shows ultrahigh (~10^5 A W^{-1}) photocurrent responsivity to UV light, which could be used as a visible-blind photodetector. The problem with this device is that the dark current is too large compared to the photocurrent, which should be addressed before using as a photodetector. One possible solution is to improve the crystal quality and lower the defect density of the GaN nanowires. The horizontally aligned GaN bridging nanowires can also be used as nanoelectromechanical resonators (Henry et al., 2007).

The formation of bridging nanowires with other material is also possible using Si trenches on a SOI wafer as substrate. This allows the integration of other functional elements into Si microelectronics. Conley et al. have demonstrated a gas and UV sensor using ZnO nanowires bridging between n^+-Si electrodes (Conley et al., 2005). Lee et al. also have successfully achieved ZnO bridging nanowires between Si electrode posts by a single-step thermal evaporation method (Lee et al., 2006). The fabricated ZnO nanobridge device shows very fast response upon turning on/off UV (Lee et al., 2007a). This kind of heterostructures have contact barrier between the electrode posts and the bridging nanowires, which may not be favored by some devices. On the other hand, the heterojunction can be beneficial for some devices if it is properly designed.

Recently, the HP group has advanced this technique to realize a top-gated MOSFET (Quitoriano & Kamins, 2008). Fig. 4a-f shows the schematic process flow for fabricating such a Si bridging nanowire MOSFET. An SOI wafer consisting of a 100 nm thick, (100)-oriented, n^+-Si layer on a 200 nm thick buried SiO_2 layer on a p-Si handle layer is used as the starting substrate. A 70 nm Si_3N_4 layer is deposited on the n^+-Si, patterned, and used as hard mask to etch the exposed Si to form electrically isolated electrodes. The SiO_2 layer is then etched to undercut the top n^+-Si layer. Colloidal Au nanoparticles are deposited only on the exposed Si surfaces by a selective placement technique, as schematically shown in Figure 4c. Si bridging nanowires are grown across the gap between the source and drain in a CVD process. The growth direction of the Si nanowires is guided by using the SiO_2 surfaces. The mechanism of the guided VLS nanowire growth using SiO_2 is also studied by the same group (Quitoriano et al., 2009). The nanowires are thermally oxidized to form a 13-21 nm oxide. Al (200 nm in thickness) is deposited to make contacts to the source and drain and Ti (170 nm in thickness) is deposited as the top gate. The SEM and TEM images of the fabricated MOSFET are shown in Fig. 4g-i. The measured drain characteristics with gate voltages from 0 to -1.35 V show good saturation. The gate characteristics measured at a drain voltage of 0.1 V show high I_{on}/I_{off} ratio of ~10^4 and inverse sub-threshold slope of ~155 mV/decade. The integration of nanowires into MOSFETs by bridging method can help realize the full promise of semiconducting nanowires since practical applications of nanowires are likely to use a combination of top-down patterning with self-assembly to integrate nanowires with conventionally formed microstructures.

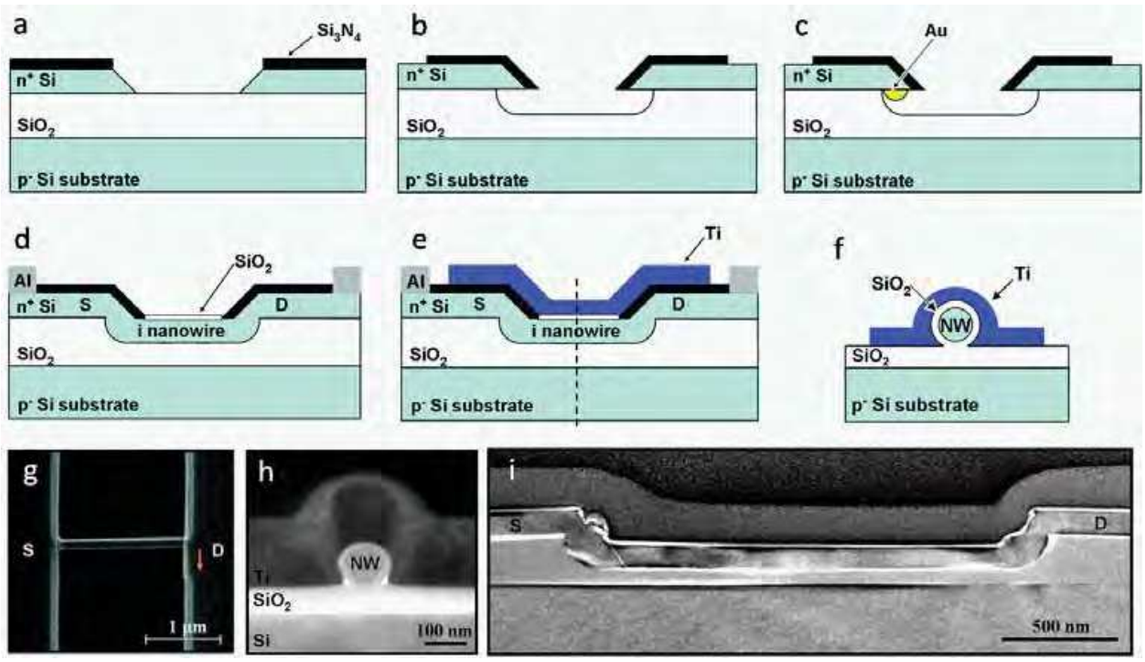

Fig. 4. (a-f) Process flow and schematic architecture of the Si bridging nanowire MOSFET. (g) Top-view SEM image of a Si bridging nanowire grown between source (S) and drain (D). (h) Perpendicular and (i) longitudinal, cross-sectional TEM images of a nanowire bridging source and drain. Reprinted with permission from (Quitoriano & Kamins, 2008), © 2008 American Chemical Society.

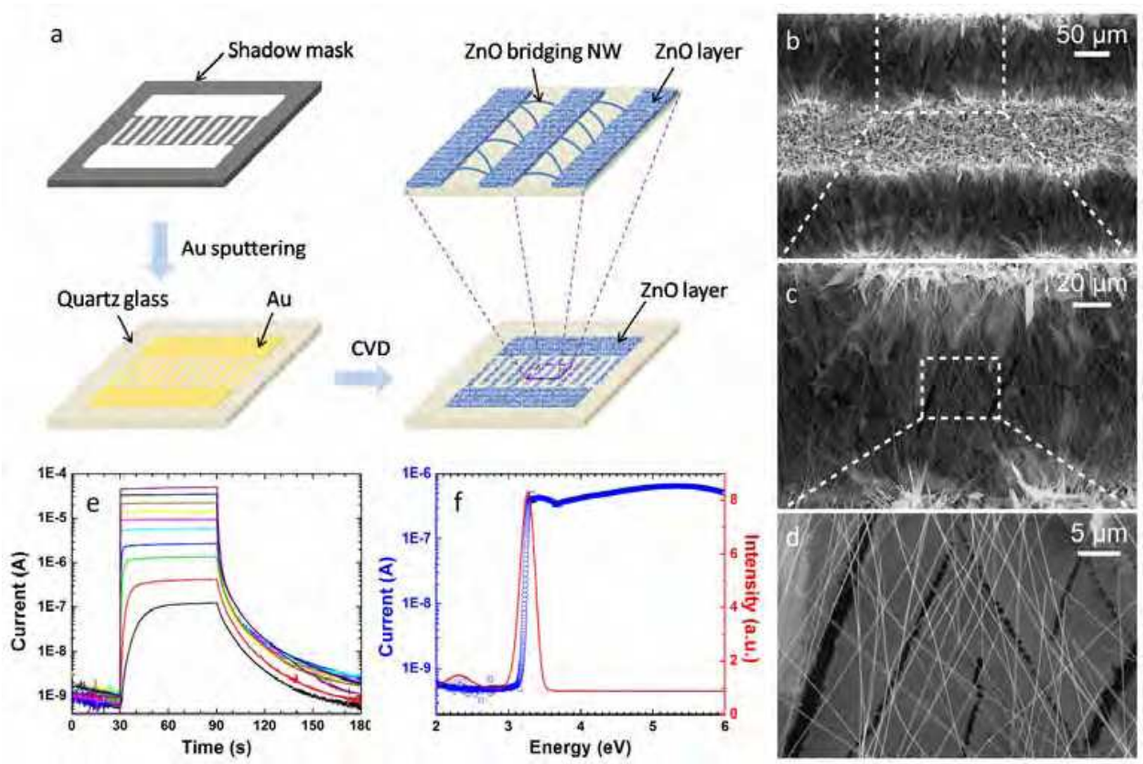

Fig. 5. (a) Schematic process flow of the single-step fabrication of ZnO bridging nanowires. (b-d) SEM images of the ZnO thick layer electrodes and the ZnO bridging nanowires. (e) Time-dependent UV photoresponse of the ZnO bridging nanowire UV photodetector. (f) Cathodoluminescence (CL) and spectral photoresponse of the ZnO bridging nanowires.

The conventional bridging method, as shown in the above examples, requires the fabrication of micro-trenches and electrode posts before the growth of nanowires. The process can be further simplified for some device applications. Li et al. have proposed a single-step bridging method to fabricate ZnO bridging nanowires without resorting to any microfabrication process (Li et al., 2008; Li et al., 2009a, b). In this method, the electrodes and the bridging nanowires are synthesized simultaneously in a CVD process. The schematic fabrication process is shown in Fig. 5a. First, a 2-nm-thick gold catalyst layer is sputtered on a quartz glass through a comb-shaped metal shadow mask. Then, ZnO is grown on the Au patterned substrate in a CVD process. After the CVD process, the Au pattern areas, i.e., the comb pads and fingers, are covered by a thick ZnO layer. SEM observation reveals that the thick layer consists of dense ZnO nanowires and nanosheets (Fig. 5b). The gap (~100 μm in width) between the comb fingers is bridged by many ultra-long nanowires, as shown in Fig. 5c-d. The key to this single-step bridging method is to achieve lateral growth of ultra-long nanowires at the edge of the thick layer, so that physical masking can be applied to pattern the Au catalyst instead of lift-off processes. The as-made structure can be directly used for photoresponse test by contacting the comb pads with In or Al which form ohmic contacts with ZnO. Time-dependent photoresponse of the device in Fig. 5e shows that the current increases drastically and rapidly when exposed to UV illumination. The current increases by

2 to 5 orders under an irradiance of 180 nW/cm^2 to 48 mW/cm^2. The photocurrent decay is also very fast. The decay time is in the order of a few seconds. With the current being insensitive to photon energy lower than ~3.2 eV (Fig. 5f), the device exhibits visible-blind spectral photoresponse. By eliminating lift-off from the fabrication process of the device, the nanowires are free of contamination, which is one of the major advantages of bridging technique as discussed above. Besides, the nanowires are lying over the substrate instead of being in contact with the substrate, rendering their surfaces fully exposed to the ambient atmosphere. This can be very beneficial to nanowire devices such as gas/chemical sensors, in which the surfaces of the nanowires play a central role in the sensing mechanism. Therefore, this single-step bridging method is suitable for the mass-production of low-cost and high-performance nanowire photodetectors and gas/chemical sensors.

4. Conclusion

The remarkable progress made on the synthesis of nanowires over recent years offers a wide selection of building blocks for future nanodevices which are deemed to change our life fundamentally. However, the assembly of these building blocks in reliable and economical ways should be addressed before the flourish of nanotechnology. In this chapter, technologies developed for the assembly of nanowire devices were reviewed. We focused on two main strategies for tackling this problem, that is, transfer with alignment of pre-grown nanowires onto a surface and direct growth of nanowires onto a substrate at desired locations. Nanowire devices demonstrated by these assembly techniques were introduced. By combining the current stage top-down techniques with the nanowire assembly techniques, the fabricated nanodevices show properties that motivate us on carrying on the research. It also points out future research directions for nanotechnology. Nevertheless, many practical problems have to be solved for integration of nanowires into devices. A lot more effort has to be put into the development of new nanowire assembly techniques, as we have been doing for the synthesis of nanowires. It is impossible to find a universal way that solves all the problems. Understanding the weaknesses of each technique is as important as understanding their advantages, for it can help us select the right one for a specific device application. A combination of two or more assembly techniques will be useful as illustrated by some of the cases given above. Through this review, we hope that readers not only learn the state-of-the-art nanowire assembly technologies, but also gain more confidence on the future of nanotechnology despite of all the difficulties.

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This volume is intended to orient the reader in the fast developing field of semiconductor nanowires, by providing a series of self-contained monographs focusing on various nanowire-related topics. Each monograph serves as a short review of previous results in the literature and description of methods used in the field, as well as a summary of the authors recent achievements on the subject. Each report provides a brief sketch of the historical background behind, the physical and/or chemical principles underlying a specific nanowire fabrication/characterization technique, or the experimental/theoretical methods used to study a given nanowire property or device. Despite the diverse topics covered, the volume does appear as a unit. The writing is generally clear and precise, and the numerous illustrations provide an easier understanding of the phenomena described. The volume contains 20 Chapters covering altogether many (although not all) semiconductors of technological interest, starting with the IV-IV group compounds (SiC and SiGe), carrying on with the binary and ternary compounds of the III-V (GaAs, AlGaAs, GaSb, InAs, GaP, InP, and GaN) and II-VI (HgTe, HgCdTe) families, the metal oxides (CuO, ZnO, ZnCoO, tungsten oxide, and PbTiO3), and finishing with Bi (a semimetal).

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