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Carbon Nanotube Capacitors

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1. Introduction

Capacitors are important components in many integrated circuits. They serve numerous roles in analog and mixed signal circuits, including switched capacitor filters and sample-and-hold circuits. In addition, capacitors provide a vital role in the decoupling of microprocessors, digital signal processors, and microcontrollers from power supply variations.

Traditional integrated circuit capacitors use a parallel plate structure. The capacitance of these parallel plate structures is fundamentally limited by the die area they consume and the thickness of the dielectric material between the parallel plates. However, increasing the capacitance of traditional parallel plate capacitors by increasing the die area (resulting in a more expensive component) or decreasing the dielectric thickness (resulting in a higher leakage current) contradicts two of the fundamental tenements of integrated circuit design (ITRS, 2008).

Carbon nanotubes (CNTs) are nanotechnology materials that have been in prominence for the last several years. They are cylinders of graphene that can exhibit radii on the order of nanometers. CNTs exhibit a number of properties that make them attractive as potential horizontal and vertical interconnects in future integrated circuits (Naeemi et al., 2004, Naeemi et al., 2005, Raychowdhury & Roy, 2004). The same properties allow CNTs to be used to create a new capacitor structure suitable for use in future integrated circuits (Budnik et al., 2006). In this chapter we introduce these CNT capacitor structures and compare their capacitance per unit area with existing technologies.

The chapter is organized as follows. Section 2 reviews the structure and limitations of traditional parallel plate capacitors in integrated circuits. Section 3 briefly introduces CNTs, their varieties, and how they can be manufactured. Section 4 reviews the electrical models that have been developed for CNTs for use in the development of a CNT capacitor model. Section 5 formally introduces CNT capacitor devices as an extrapolation of the currently proposed CNT interconnects. Three different CNT capacitor structures and their electrical models are presented in this section. Finally, the conclusions are presented in Section 6.

2. Capacitors

Traditional semiconductor capacitors use a parallel plate structure. The various semiconductor capacitors, however, use different electrode materials. The metal-oxide-

semiconductor capacitor (MOSC) uses a metal-oxide-semiconductor field effect transistor (MOSFET) to create the capacitor. The MOSFET's gate serves as one electrode, and its source and drain regions serve as the second electrode. The gate dielectric serves as the capacitor dielectric. Therefore, the inter-plate spacing is the MOSFET gate oxide thickness. Another integrated circuit parallel plate semiconductor capacitor is the metal-insulator-metal capacitor (MIM). The electrodes of the MIM are metal layers located in the higher metal levels of an integrated circuit. A thin dielectric material separates the plates. The capacitance of both the MOSC and MIM devices is approximated by the equation:

$$C = \frac{A \in}{d} \tag{1}$$

where A is the area of each parallel plate, d is the thickness of the dielectric, and $\in$ is the permittivity of the dielectric material separating the parallel plates.

However, due to their parallel plate structure, MOSC and MIM capacitors face numerous challenges in future integrated circuit technologies (ITRS, 2008). First, as component dimensions are scaled, decreased parallel plate area (scaled in width and length, an S^2 decrease) will result in a reduction in capacitance. Decreasing the dielectric thickness can offset the decrease in plate area, but the increase in capacitance is only linear (an S increase) with respect to reduced inter-plate spacing. In addition, decreasing the dielectric thickness can lead to higher leakage currents. Therefore, new capacitor structures are being investigated for future integrated circuits. For example, interdigitated Metal-Oxide-Metal (MOM) capacitors are similar to MIM capacitors and do not require additional processing steps (ITRS, 2008). However, even MOM devices are expected to have capacitance densities of less than 30fF/μm^2 through 2022 (see Figure 1).

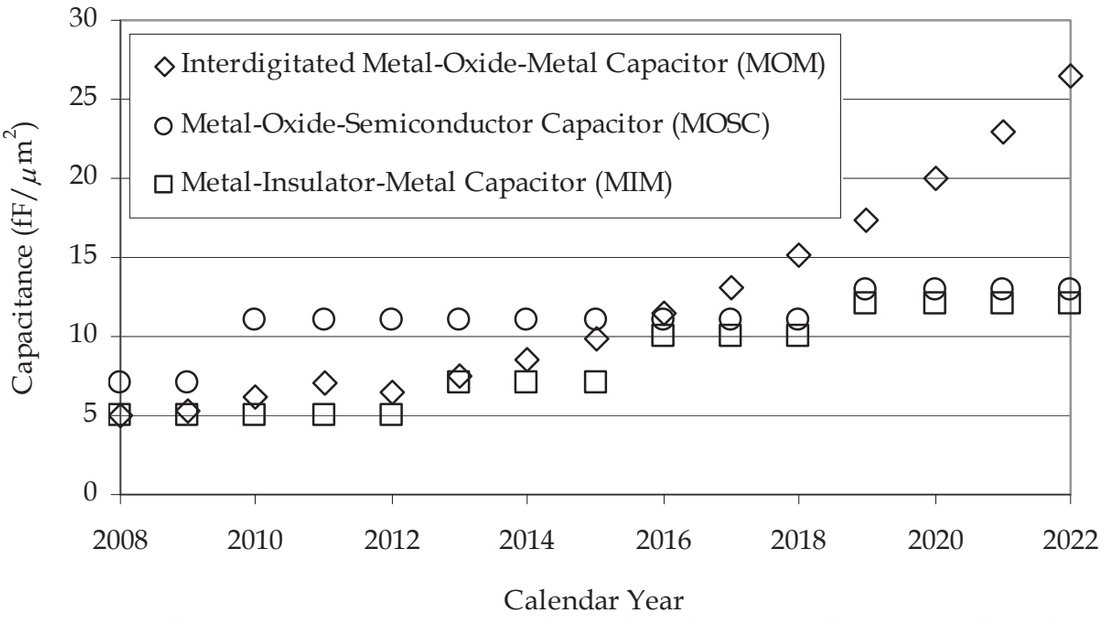

Fig. 1. Projected capacitance per unit area of metal-oxide-semiconductor, metal-insulator-metal, and interdigitated metal-oxide-metal capacitors (ITRS, 2008).

3. Carbon Nanotubes

CNTs are nanoscale devices that have unique strength and electrical properties. They are formed when a graphene sheet of carbon atoms is rolled into a cylindrical structure. These structures have a wall thickness of one atom, a diameter on the order of ten atoms and are typically over several micrometers in length (Dresselhaus et al., 2000).

A single cylinder nanotube is called a single wall carbon nanotube (SWCNT). Multi-wall carbon nanotubes (MWCNTs) contain multiple coaxial cylinders which are concentric SWCNTs. Both SWCNTs and MWCNTs can have varying diameter dimensions. SWCNTs have diameters from one to a few nanometers, while MWCNT diameters are from the tens to a hundred nanometers (Naeemi & Meindl, 2007). CNTs can be analyzed either in isolation (singularly) or in bundles (arrays of CNTs along a common axis).

One of the reasons CNTs have attracted so much interest is their electrical characteristics. CNTs can act as either metallic or semiconducting materials, depending on their structure. The circumference of a CNT can be represented by a chiral vector, which describes how carbon atoms within the tube are connected together. Depending on this vector, different types of nanotube structures can be constructed when the graphene sheet is rolled into a cylinder. If the chiral vector angle is 0°, then a *zigzag* structure is formed, and the CNT acts like a semiconductor. If the angle is 30°, an *armchair* structure occurs, and the CNT acts like a metal. All other nanotubes are labeled chiral nanotubes and will also act as semiconductors. Scientists have had limited success controlling the chiral vector; therefore, only about one third of carbon nanotubes that are manufactured are metallic (Dresselhaus et al., 2000).

CNTs are primarily manufactured using three different methods: arc-discharge, laser ablation, or chemical vapor deposition (Dresselhaus et al., 2000). Arc-discharge and laser ablation are similar in that both involve evaporating solid carbon sources to produce a condensation of carbon atoms. In contrast, chemical vapor deposition grows carbon nanotubes on top of a metal catalyst.

In the arc-discharge method, a carbon anode and cathode are set up in a chamber filled with helium gas. High currents are passed through the circuit, causing the evaporation of carbon atoms (Dresselhaus et al., 2000). The resulting carbon soot contains both MWCNTs and graphitic particles that are removed in a high-temperature oxygen environment. The growth of the nanotubes can be controlled by changing either the pressure of the gas in the chamber or the amount of arcing current used. To create SWCNTs, a metal catalyst, such as cobalt, must be added to the system.

Laser ablation is a similar method for manufacturing CNTs (Dresselhaus et al., 2000). A laser is used to ablate a carbon target within a tube furnace heated to 1200°C. The MWCNTs created from the process are carried down the chamber on an inert gas and then collected. SWCNTs are created if the carbon target contains small amounts of nickel and cobalt. Varying the temperature changes the diameters of the carbon nanotubes.

The final method used for manufacturing carbon nanotubes is chemical vapor deposition (CVD). In CVD, a metal catalyst such as nickel or cobalt is placed on a substrate in a tube furnace. The catalyst is heated at a high temperature (500-1000°C) while a hydrocarbon gas flows through the furnace (Dresselhaus et al., 2000). During the process, CNTs grow on the catalyst. The properties of the CNTs (single vs. multiwall, diameter) are determined by the catalyst used and the temperature of the furnace. This method has the most potential for commercial applications because the nanotubes can be grown on an existing substrate rather than being attached to new material after a collection process.

4. Electrical Models of Carbon Nanotube Interconnects

This section summarizes the primary electrical models that have been developed for SWCNTs. An understanding of these models is essential for the development of our CNT capacitor models. The (Naeemi & Meindl, 2007) SWCNT electrical model will be used to determine the electrical models for our CNT capacitors. However, for completeness, we also present two other models. The models in this section were based on the work that developed transmission line and *RLC* models for ideal SWCNTs (Burke, 2002; Burke, 2003).
An equivalent *RLC* circuit model for SWCNTs originally developed for interconnect applications is shown in Figure 2 (Naeemi & Meindl, 2007). This model is valid for isolated metallic SWCNTs of all lengths used in interconnect applications.

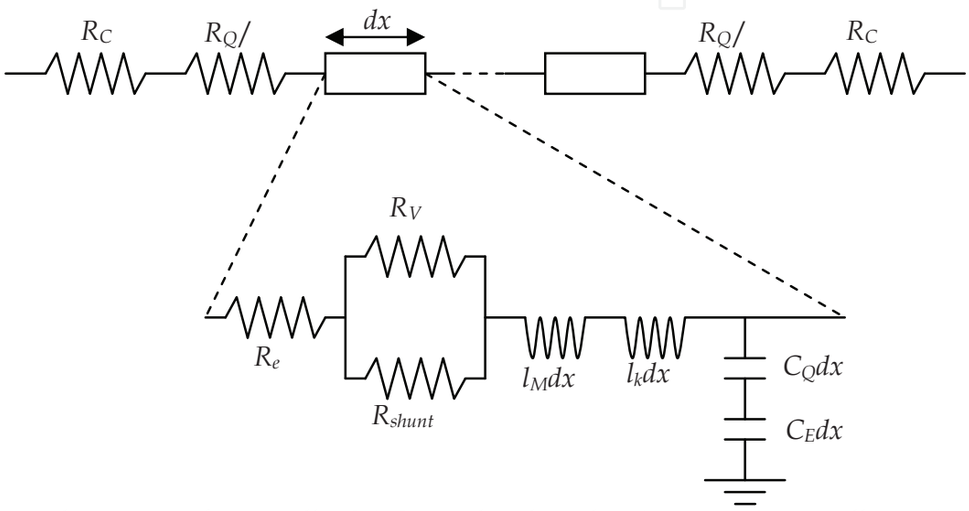

Fig. 2. Equivalent circuit for metallic SWCNTs developed in (Naeemi & Meindl, 2007).

The resistance components in the model include a lumped resistance at the two ends of the SWCNT and a distributed resistance throughout the SWCNT. The lumped resistance consists of the contact resistances (R_C) and the quantum resistance per channel (R_Q). The contact resistance can vary depending on the quality of the connection. If the connection is poor, the electron scattering at the contacts can cause a significant increase in the resistance. The quantum resistance is the minimum resistance associated with a quantum wire, which for a SWCNT is 6.45kΩ. It can be combined with the distributed resistances (R_e, R_V, and R_{shunt}) and simplified to form the overall resistance, R, which can be approximated by the equation:

$$R = R_Q\left(1+\frac{\ell}{\ell_{\,mpf,low}}\right)+\frac{V_{DROP}}{I_0} \tag{2}$$

where ℓ is the length of the SWCNT, $\ell_{\,mfp,low}$ is the SWCNT low-bias mean free path, V_{DROP} is the voltage drop across the SWCNT, and I_0 is the low-bias current through the SWCNT.
The capacitive components include a quantum capacitance (C_Q) in series with an electrostatic capacitance (C_E). The quantum capacitance is approximately 100aF/μm of CNT length. The electrostatic capacitance is typically much smaller than the quantum

capacitance. Since the two capacitances are in series, the quantum capacitance has little impact on the overall capacitance.

The kinetic (l_k) and magnetic (l_M) inductances are the inductive components of the SWCNT. The kinetic inductance, which is the kinetic energy of the electrons in the nanotube, is approximately 4nH/μm. This value is orders of magnitude larger than the magnetic inductance, so l_M can be disregarded when calculating the overall inductance in the SWCNT model.

To further improve the conductive performance of SWCNTs, they can be arranged in bundles. Fortunately, many of the electrical properties associated with isolated SWCNTs can be extended to SWCNTs bundles. For example, (Naeemi & Meindl, 2007) computes the conductivity of a SWCNT bundle using

$$\sigma_{SWCNT} = (n / A_{bundle}) / \left(\frac{R_C}{\ell} + R_Q \left(\frac{1}{\ell} + \frac{1}{\ell_{eff}} \right) \right) \tag{3}$$

where ℓ_{eff} is the mean free path length of electrons in the SWCNTs, n is the number of SWCNTs in the bundle, A_{bundle} is the cross sectional area of the bundle, and R_C is the contact resistance which quantifies the quality of the connections at each end. The quantum capacitance of SWCNT bundles is calculated by summing the quantum capacitances of all metallic SWCNTs in the bundle. Since all the nanotubes in the bundle have the same potential, the electrostatic capacitances between nanotubes can be ignored and, similar to metal interconnects, only the electrostatic capacitances to ground and neighboring bundles must be considered. The electrostatic capacitance values are again significantly less than the total quantum capacitance. Since the two capacitances are still in series, the quantum capacitance again has only a slight impact on the overall SWCNT bundle capacitance, however, it will be included in our development of the CNT capacitor electrical model.

For comparison, the circuit model by (Srivanstava & Banerjee, 2005) is given in Figure 3. It assumes that the length of the SWCNT is less than the mean free path of electrons and that there are ideal contacts at each end.

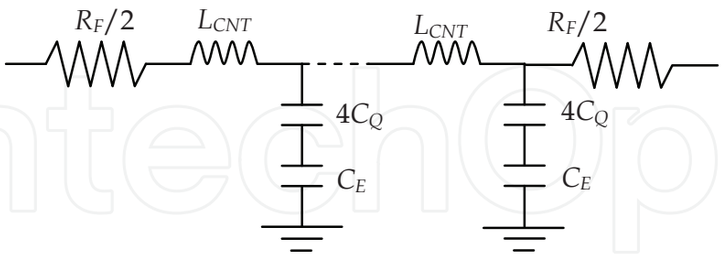

Fig. 3. Equivalent circuit for isolated SWCNTs developed by (Srivanstava & Banerjee, 2005).

The above model is similar to Figure 2 for isolated SWCNTs in that both have a lumped and distributed portion of the model. The inductance, L_{CNT}, contains both the mutual and kinetic inductance, which is also similar to the (Naeemi & Meindl, 2007) model. The main difference between the two SWCNT models is their quantum capacitance. In the (Srivanstava & Banerjee, 2005) model, C_Q is multiplied by a factor of four to account for the four conducting channels found in SWCNTs (with $4C_Q$ = 388aF/μm of SWCNT length).

There are also differences between the (Srivanstava & Banerjee, 2005) and (Naeemi & Meindl, 2007) models of SWCNT bundles for the calculation of the bundle resistance. The (Srivanstava & Banerjee, 2005) model assume that all SWCNTs in the bundle are metallic (and conducting), which makes the overall bundle resistance equal to the resistance of an isolated SWCNT divided by the number of tubes in the bundle.
The final model for comparison was developed by (Nieuwoudt et al., 2007) and is shown in Figure 4. They have created an *RLC* model that can be scaled to include bundles of SWCNTs.

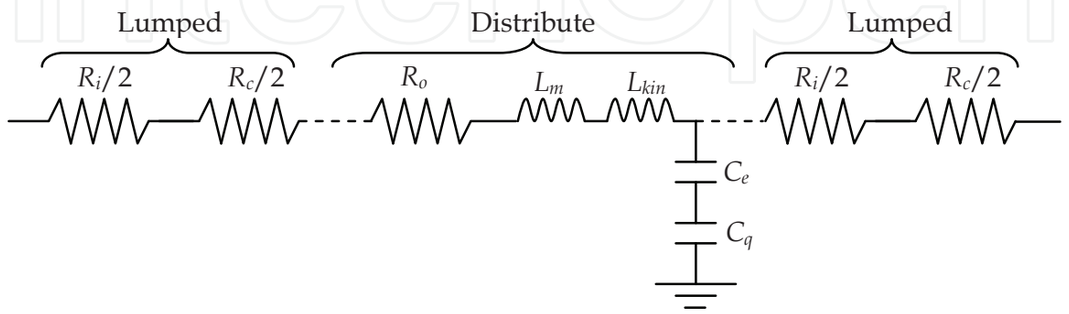

Fig. 4. Equivalent *RLC* circuit for isolated SWCNTs developed by (Nieuwoudt & Massoud, 2006a, 2006b).

The lumped portion of the model contains both an intrinsic and a contact resistance (R_i and R_c), while the distributed portion has an ohmic resistance (R_o), the kinetic and magnetic inductance (L_{kin} and L_m) and the electrostatic and quantum capacitance (C_e and C_q) of the SWCNT. This model of an isolated SWCNT is similar to the previous two models except that it also includes an ohmic resistance of the SWCNT. In addition, the model uses the diameters of the SWCNT as a variable affecting the ohmic and contact resistances (Nieuwouldt & Massoud, 2006a). Also, the model also considers the entire current loop when modelling the magnetic inductance. They argue this value can be as large as the kinetic inductance in some interconnect applications, and that it must also be considered when computing the overall inductance (Nieuwouldt & Massoud, 2006b). Finally, the capacitance of a bundle of SWCNTs is represented as a single conductor with a given width and height, which significantly decreases the computation needed to calculate the overall capacitance.

5. Carbon Nanotube Capacitor Structures

One potential application for SWCNT bundles in future integrated circuits is as replacements for vertical interconnect (via) structures. In such structures, the SWCNT bundle will connect two consecutive horizontal metal layers (see Figure 5). (Nihei et al., 2004) has shown how bundles of CNTs can be implemented as vias. They fabricated a bundle of about one thousand CNTs between two metal layers and observed no drop in current density through the via over a one hundred hour period.

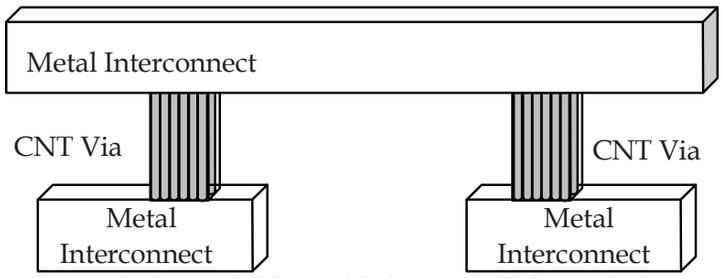

Fig. 5. Example of how a bundle of single wall carbon nanotubes can be used as vertical interconnect (via) structures in future integrated circuits.

If we refer back to Figure 5, we can readily see that by cutting the upper metal layer, we can create a vertical CNT capacitor (Wood & Budnik, 2007) (see Figure 6).

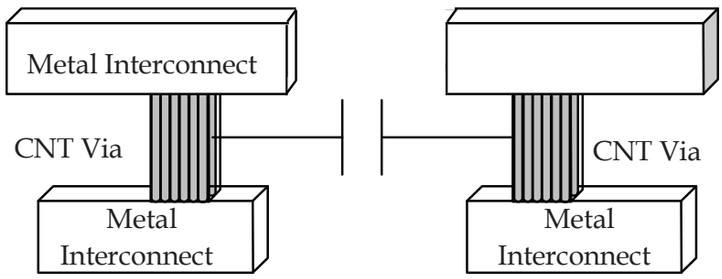

Fig. 6. Example of how a vertical carbon nanotube capacitor can be constructed from two carbon nanotube vias. (Wood & Budnik, 2007)

In the following subsections, we will examine three different structures for CNT capacitors:

- CNT vertical parallel plate capacitor
- CNT vertical bundle capacitor
- CNT vertical interleaved sheet capacitor

In each subsection, we show how the capacitors can be constructed. In addition, we develop a three element electrical model (Budnik et al., 2006) for each capacitor (see Figure 7). R_{CNCAP} is the CNT capacitor's equivalent series resistance, L_{CNCAP} is the CNT capacitor's equivalent series inductance, and C_{CNCAP} is the device's capacitance.

5.1 Carbon nanotube vertical parallel plate capacitor

The first CNT capacitor we introduce is the vertical parallel plate capacitor (Wood & Budnik, 2007). For this device, two bundles of CNTs are grown vertically in close proximity

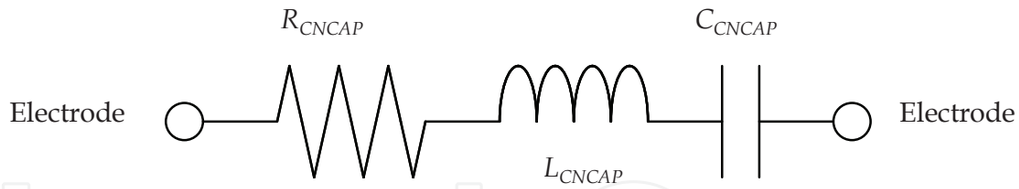

Fig. 7. Three element electrical model of a carbon nanotube capacitor (Budnik et al., 2006) to each other (see Figure 8). The bundles have a separation distance, *s*, width, *w*, and height, *h*. Each CNT has a radius, *r*.

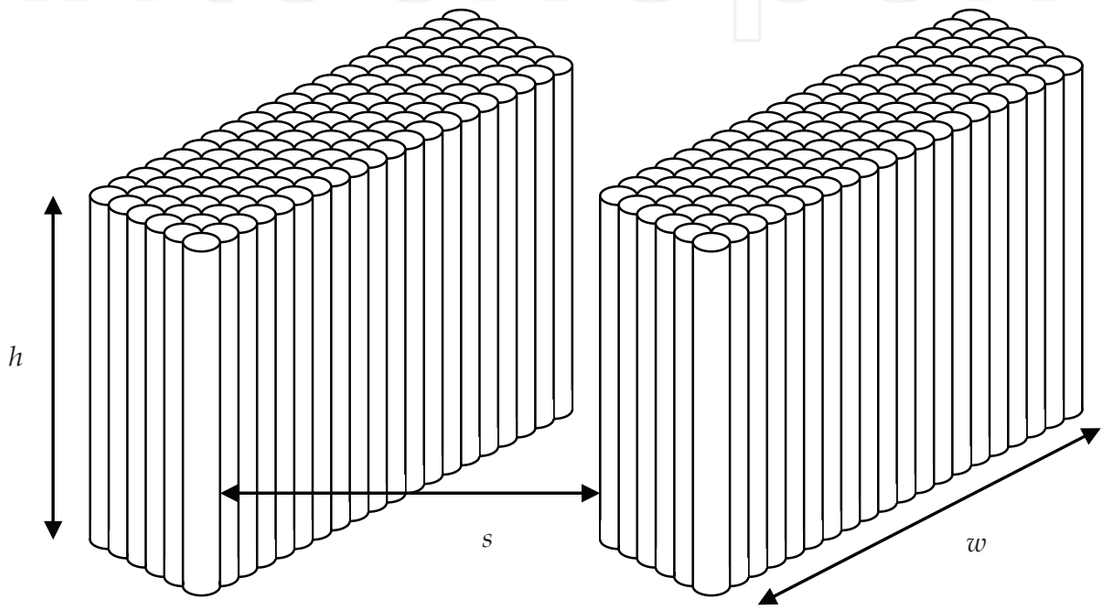

Fig. 8. Carbon nanotube vertical parallel plate capacitor.

The only difference between the ideally packed bundles in Figure 8 and perfectly smooth plates is the surface roughness of the bundles. When *r* is less than an order of magnitude less than *s*, however, the impact of the surface roughness on the electrostatic coupling capacitance is less than 3% (Naeemi & Meindl, 2007), based upon simulations with the field solver, RAPHAEL (RAPHAEL, 1999). This is consistent with the models developed by (Bruce et al., 1999). Therefore, we take the electrostatic coupling capacitance of the structure from (1) as:

$$C_{Plates} = \frac{wh\epsilon}{s} \tag{4}$$

For the two bundles, the number of SWCNTs on each vertical parallel plate is given by:

$$N_{Plate} = \frac{w}{2r} \tag{5}$$

where *r* is the radius of the individual SWCNTs. For SWCNTs, *r* is typically 0.5nm (Dresselhaus, 2000).
Since C_Q is in units of F/unit length, the total quantum capacitance of each bundle is:

$$C_{Q,Bundle} = N_{Plate}\left(hC_Q\right) \tag{6}$$

With C_{Plates} in series with the quantum capacitance of each bundle, the capacitance of a vertical SWCNT parallel plate capacitor is:

$$C_{CNCAP} = \frac{1}{\frac{1}{C_{Q,Bundle}} + \frac{1}{C_{Plates}} + \frac{1}{C_{Q,Bundle}}} \tag{7}$$

Substituting (4-6) into (7) yields:

$$C_{CNCAP} = \frac{1}{\frac{1}{N_{Plate}\left(hC_Q\right)} + \frac{1}{\frac{wh\in}{s}} + \frac{1}{N_{Plate}\left(hC_Q\right)}} \tag{8}$$

Simplifying (8) results in:

$$C_{CNCAP} = \frac{h}{\frac{2}{N_{Plate}\left(C_Q\right)} + \frac{s}{w\in}} \tag{9}$$

As an example, if we let h = 1μm, $\in$ = 3.9(8.854x10^{-12}F/m), and C_Q = 388aF/μm, we can plot C_{CNCAP} vs. s and w as shown in Figure 9. At an example point in this graph where s = 10nm and w = 100μm, C_{CNCAP} = 18.3fF.

Next, we turn our attention to the equivalent series resistance and inductance of the vertical SWCNT parallel plate capacitor. If the current in each SWCNT continues to flow in only a vertical direction inside each bundle, then the total number of SWCNTs conducting in each bundle is again N_{Plate}. Using a lumped model for the device, R_{CNCAP} and L_{CNCAP} will be given by:

$$R_{CNCAP} = \frac{1}{N_{Plate}}\left[2R_C + R_Q\left(1 + \frac{h}{\ell_{mpf,low}}\right) + \frac{V_{DROP}}{I_0}\right] \tag{10}$$

$$L_{CNCAP} = \frac{hL_k}{N_{Plate}} \tag{11}$$

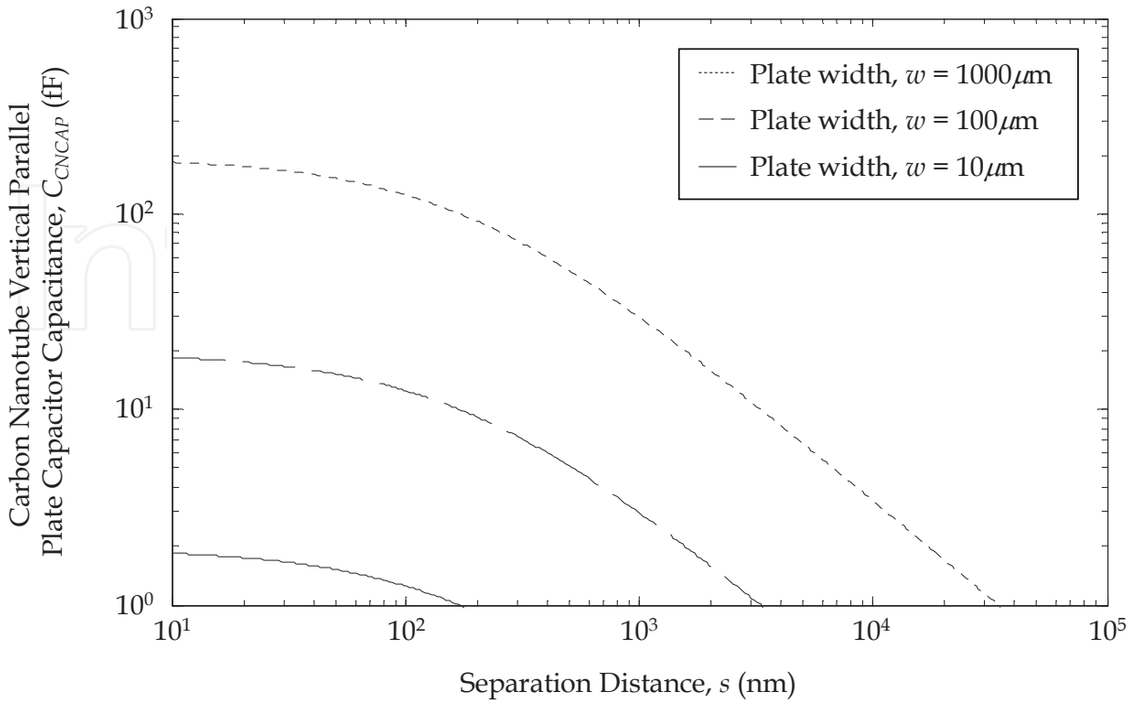

Fig. 9. Carbon nanotube vertical parallel plate capacitor capacitance, C_{CNCAP}, vs. plate separation distance, s, and plate width, w.

5.2 Carbon nanotube vertical bundle capacitor

From the CNT capacitor structure in the above sub-section, we can readily imagine an array of CNT bundles alternately connected to the capacitor's anode (A) and cathode (C). The capacitance between nearest neighbor bundles is C_{Bundle}. The cross section of the device is shown in Figure 10 (Wood & Budnik, 2007, Budnik & Johnson, 2009). The bundles have four sides of width w and are of height h. The inter-bundle spacing is s.

Extrapolating from the previous section, the electrostatic coupling capacitance C_{Bundle} is:

$$C_{Bundle} = \frac{wh \in}{s} \tag{12}$$

For the bundles, the number of CNTs on each bundle side is given by:

$$N_{Bundle\ Side} = \frac{w}{2r} \tag{13}$$

Since C_Q is in units of F/unit length, the total quantum capacitance of each bundle face is again:

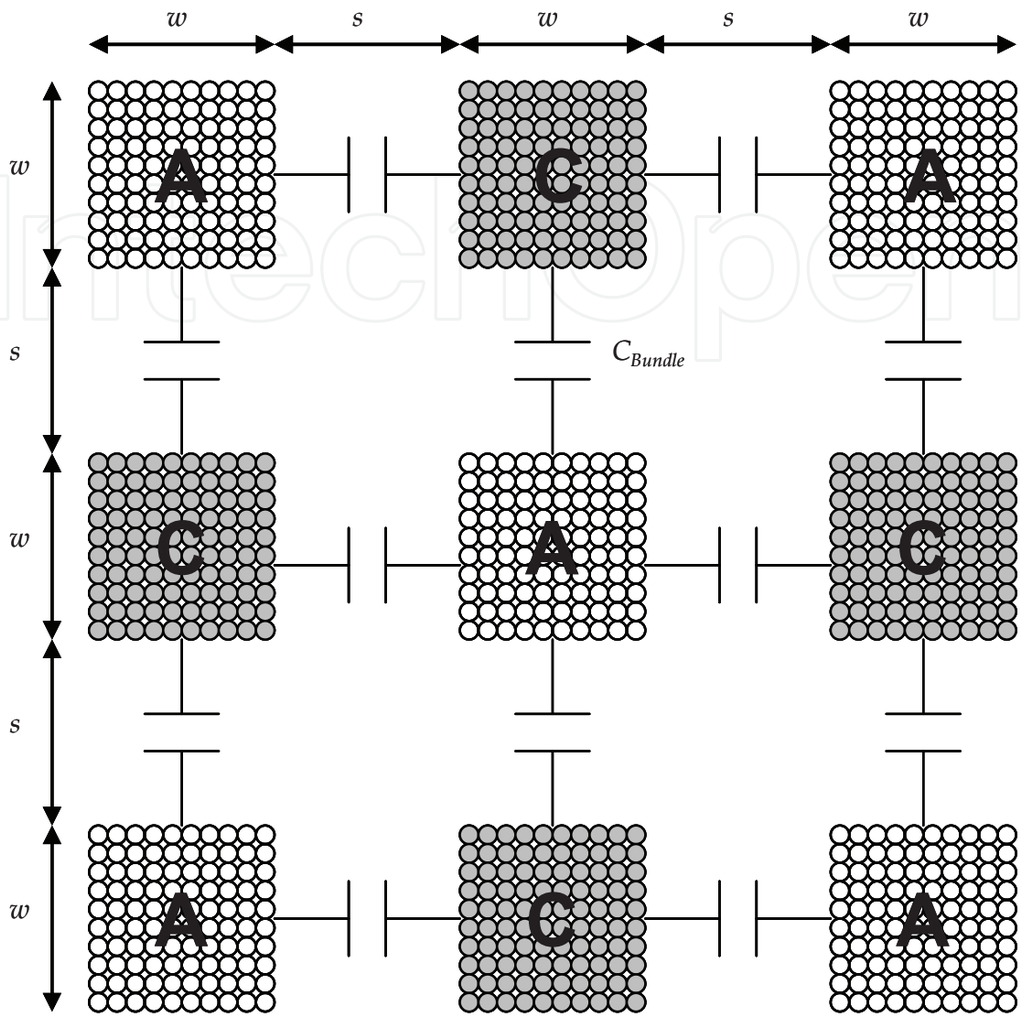

Fig. 10. Cross section of a carbon nanotube vertical bundle capacitor. Bundles are alternately connected to the device anode (A) or cathode (C).

$$C_{Q,Bundle} = N_{Bundle\ Side}\left(hC_Q\right) \tag{14}$$

With C_{Bundle} in series with the quantum capacitance of each bundle face, from (12-14) the capacitance between two nearest neighbor SWCNT bundle faces is:

$$C_{Bundle\ Faces,Total} = \frac{1}{\frac{1}{C_{Q,Bundle}} + \frac{1}{C_{Bundle}} + \frac{1}{C_{Q,Bundle}}} \tag{15}$$

$$C_{Bundle\ Faces,Total} = \frac{1}{\frac{1}{N_{Bundle\ Side}\left(hC_Q\right)} + \frac{1}{\frac{wh\in}{s}} + \frac{1}{N_{Bundle\ Side}\left(hC_Q\right)}} \tag{16}$$

Simplifying (16) results in:

$$C_{Bundle\ Faces,Total} = \frac{h}{\frac{2}{N_{Plate}\left(C_Q\right)} + \frac{s}{w\epsilon}} \tag{17}$$

To determine C_{CNCAP}, we need to determine the number of bundles per unit area. The unit cell of the vertical SWCNT bundle capacitor shown above in Figure 10 is:

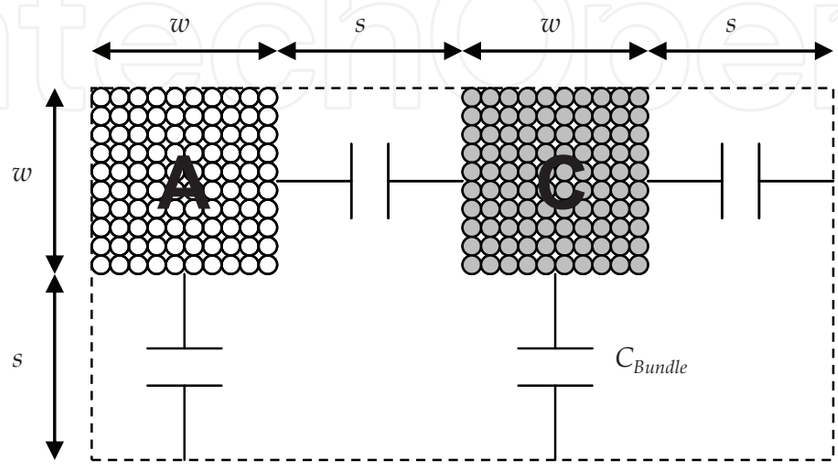

Fig. 11. Unit cell of vertical bundle capacitor in Figure 10.

The area of the unit cell is:

$$A_{Unit\ Cell} = \left(2w + 2s\right)\left(w + s\right) \tag{18}$$

When $w = s$, (18) simplifies to:

$$A_{Unit\ Cell} = \left(4w\right)\left(2w\right) = 8w^2 \tag{19}$$

There are four capacitors in the vertical SWCNT bundle capacitor unit cell. Neglecting fringe effects, from (17) and (19) the total capacitance per unit area of the device is:

$$C_{CNCAP} = \frac{4C_{Bundle\ Faces,Total}}{8w^2} \tag{20}$$

$$C_{CNCAP} = \frac{1}{2w^2}\left(\frac{h}{\frac{2}{N_{Plate}\left(C_Q\right)} + \frac{1}{\epsilon}}\right) \tag{21}$$

As an example, we again let r = 0.5nm, ϵ = 3.9(8.854x10^{-12}F/m), and C_Q = 388aF/μm. We plot C_{CNCAP} vs. s and h in Figure 12. At an example point in this graph where $s = w$ = 10nm and h = 1μm, C_{CNCAP} = 169fF/μm^2. This is more than one order of magnitude higher than the 2022 projections for MOSC and MIM devices (ITRS, 2008). If taller bundles of the SWCNTs are used in the CNT vertical bundle capacitor, the capacitance per unit area will increase linearly.

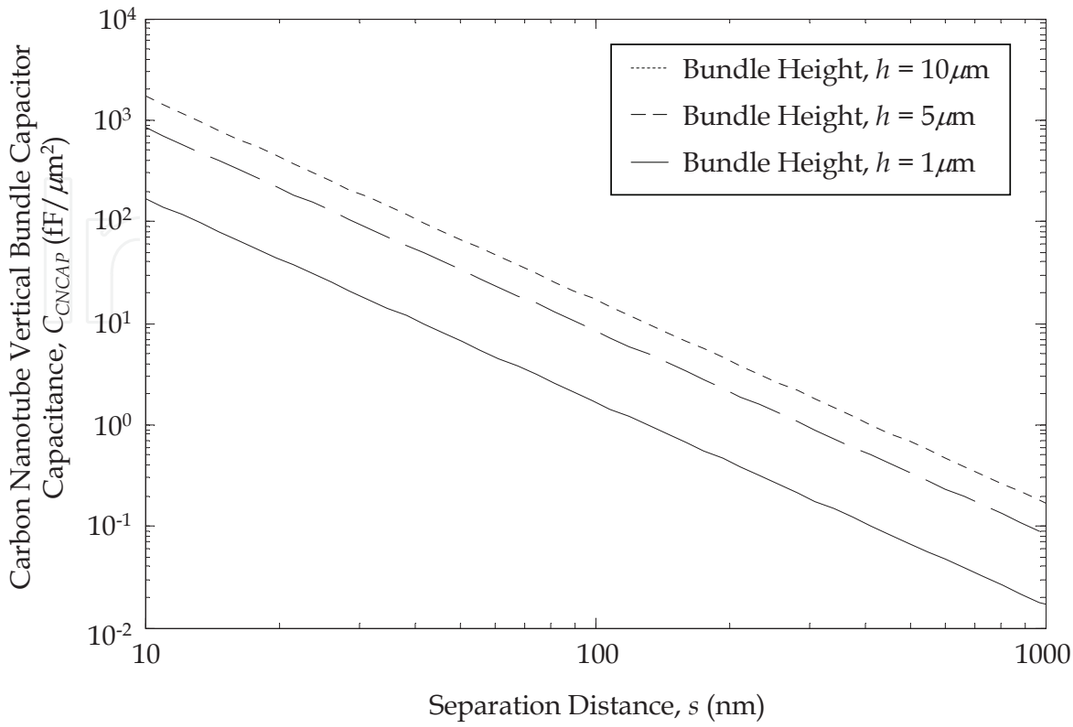

Fig. 12. Carbon nanotube vertical bundle capacitor capacitance per unit area (C_{CNCAP}) vs. bundle separation distance, s, and bundle height, h.

Next, we calculate the equivalent series resistance and inductance of the vertical SWCNT bundle parallel plate capacitor. Again, if the current in each SWCNT continues to flow in only a vertical direction inside each bundle, then the total number of SWCNTs conducting in each bundle face is again:

$$N_{Bundle\ Face} = \frac{w}{2r} \tag{22}$$

where r is the radius of the SWCNTs. However, because there are four capacitors in each unit cell, the equivalent series resistance-unit area of the vertical SWCNT bundle capacitor is:

$$R_{CNCAP} = \frac{A_{Unit\ Cell}}{4N_{Bundle\ Face}}\left[2R_C + R_Q\left(1 + \frac{h}{\ell_{mpf,low}}\right) + \frac{V_{DROP}}{I_0}\right] \tag{23}$$

Likewise, the equivalent series inductance-unit area is:

$$L_{CNCAP} = \frac{A_{Unit\ Cell}}{4N_{Bundle\ Face}}\left(h\,L_k\right) \tag{24}$$

5.3 Carbon nanotube vertical interleaved sheet capacitor

The cross section of a third CNT capacitor structure is shown in Fig. 13. It consists of densely packed, thin vertical plates of CNTs connected to alternating electrode polarities

(anode and cathode) (Budnik et al, 2008). The plates are formed by a single row of CNTs with radius *r* and height *h*. The plate width is *w* and the spacing between adjacent plates is *s*.

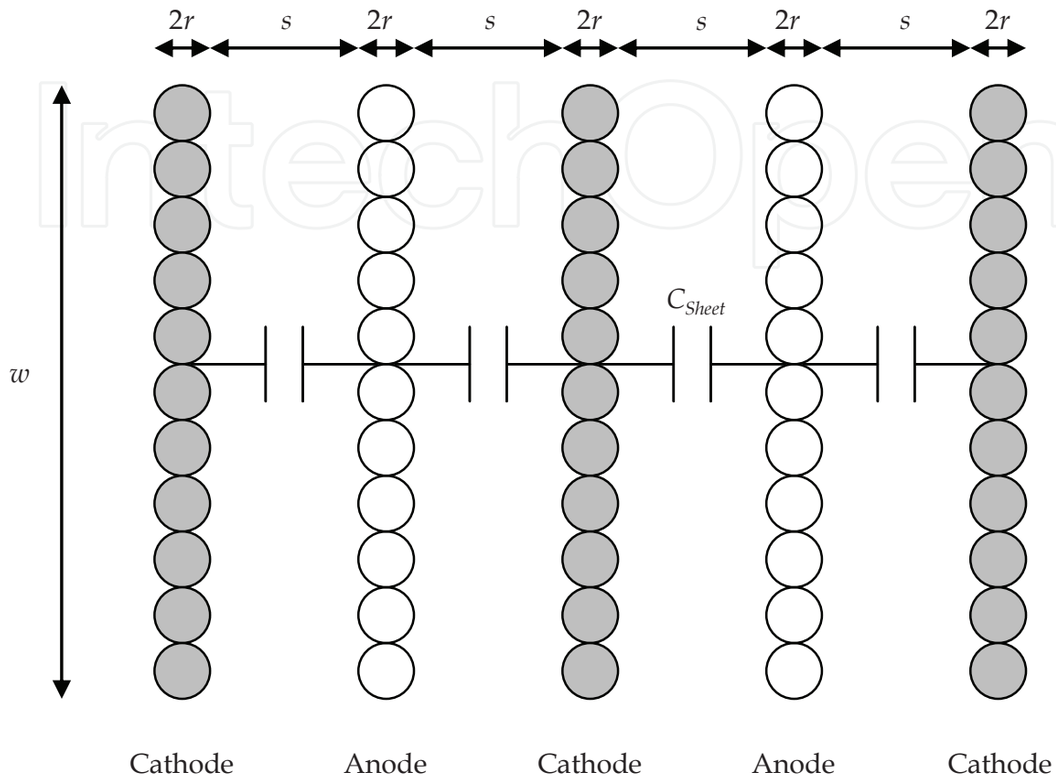

Fig. 13. Cross section of a carbon nanotube vertical interleaved sheet capacitor. Sheets are alternately connected to the device anode or cathode.

C_{Sheet} is given by:

$$C_{Sheet} = \frac{w h \in}{s} \tag{25}$$

The number of SWCNTs in each vertical sheet is given by:

$$N_{Sheet} = \frac{w}{2r} \tag{26}$$

where *r* is the radius of the individual SWCNTs.
For SWCNTs, since C_Q is in units of F/unit length, the total quantum capacitance of each sheet is:

$$C_{Q,Sheet} = N_{Sheet}\left(hC_Q\right) \tag{27}$$

With C_{Sheet} in series with the quantum capacitance of each sheet, the total capacitance between two vertical sheets is:

$$C_{2\,Sheets} = \frac{h}{\frac{2}{N_{Sheet}C_Q} + \frac{s}{w\in}} \tag{28}$$

To determine C_{CNCAP}, we need to determine the number of sheets per unit area. The area of the unit cell of the vertical SWCNT interleaved sheet capacitor in Figure 13 is:

$$A_{Unit\ Cell} = \left[2(2r) + 2s\right](w) \tag{29}$$

There are two capacitors in the vertical SWCNT interleaved sheet capacitor unit cell. Neglecting fringe effects, from (28) and (29) the total capacitance per unit area of the device is:

$$C_{CNCAP} = \frac{2C_{2\,Sheets}}{\left[2(2r) + 2s\right](w)} \tag{30}$$

$$C_{CNCAP} = \frac{1}{2r+s}\left(\frac{h}{\frac{2w}{N_{Sheet}C_Q} + \frac{s}{\in}}\right) \tag{31}$$

As an example, we again let h = 1μm, r = 0.5nm, $\in$ = 3.9(8.854x10^{-12}F/m), and C_Q = 388aF/μm. We plot C_{CNCAP} vs. s in Fig. 14. At an example point in this graph where s = 10nm and w = h = 1μm, C_{CNCAP} = 282fF/μm^2. This is again more than one order of magnitude higher than the 2022 projections for MOSC and MIM devices (ITRS, 2008).

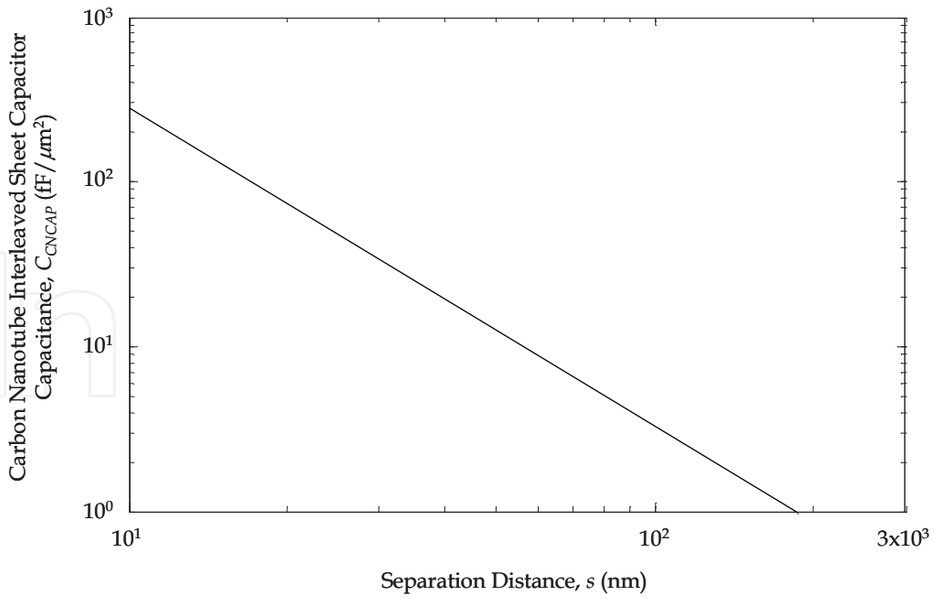

Fig. 14. Carbon nanotube vertical interleaved sheet capacitor capacitance per unit area (C_{CNCAP}) vs. bundle separation distance, s.

Finally, we turn our attention to the equivalent series resistance and inductance of the vertical SWCNT interleaved sheet capacitor. Using a lumped model for the device, R_{CNCAP} and L_{CNCAP} will be given by:

$$R_{CNCAP} = \frac{1}{N_{Sheet}}\left[2R_C + R_Q\left(1 + \frac{h}{\ell_{mpf,low}}\right) + \frac{V_{DROP}}{I_0}\right] \tag{32}$$

$$L_{CNCAP} = \frac{h L_k}{N_{Sheet}} \tag{33}$$

6. Conclusion

We began by examining the properties and shortcomings of various parallel plate capacitors used in traditional integrated circuits. Based on these shortcomings, it is projected that MOSC and MIM devices will exhibit capacitances per unit area of less than 15fF/μm^2 by 2022. Therefore, because of their attractive properties, we investigated the feasibility of using a vertical capacitor structure with CNT electrodes in future integrated circuit technologies.

Three separate CNT capacitor structures and their electrical models were presented. The first device was the CNT vertical parallel plate capacitor. While it had a limited capacitance per unit area, it was a simple transition from the CNT vertical parallel plate capacitor to our second device, the CNT vertical bundle capacitor. Through our analysis, we demonstrated how the CNT vertical bundle capacitor can exhibit capacitances per unit area of 169fF/μm^2 (based upon a 1μm tall structure). Finally, we presented a CNT interleaved sheet capacitor which can demonstrate an improved capacitance per unit area of 282fF/μm^2 (again based upon a 1μm tall structure).

CNT fabrication in integrated circuit technologies is still in its infancy. However, vertical CNT electrode capacitors have the potential of significantly improving the options available for future integrated circuit designers.

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The main purpose of this book is to describe important issues in various types of devices ranging from conventional transistors (opening chapters of the book) to molecular electronic devices whose fabrication and operation is discussed in the last few chapters of the book. As such, this book can serve as a guide for identifications of important areas of research in micro, nano and molecular electronics. We deeply acknowledge valuable contributions that each of the authors made in writing these excellent chapters.

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