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Interconnect Challenges and Carbon Nanotube as Interconnect in Nano VLSI Circuits

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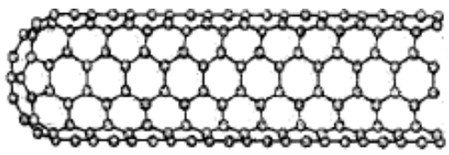
This chapter discusses about the behavior of Carbon Nanotube (CNT) different structures which can be used as interconnect in Very Large Scale (VLSI) circuits in nanoscale regime. Also interconnect challenges in VLSI circuits which lead to use CNT as interconnect instead of Cu, is reviewed. CNTs are classified into three main types including Single-walled Carbon Nanotube (SWCNT), CNT Bundle, and Multi-walled Carbon Nanotube (MWCNT). Because of extremely high quantum resistance of a SWCNT which is about 6.45 kΩ, rope or bundle of CNTs are used which consist of parallel CNTs in order to overcome the high delay time due to the high intrinsic (quantum) resistance. Also MWCNTs which consist of parallel shells, present much less delay time with respect to SWCNTs, for the application as interconnects. In this chapter, first a short discussion about interconnect challenges in VLSI circuits is presented. Then the repeater insertion technique for the delay reduction in the global interconnects will be studied. After that, the parameters and circuit model of a CNT will be discussed. Then a brief review about the different structures of CNT interconnects including CNT bundle and MWCNT will be presented. At the continuation, the time domain behavior of a CNT bundle interconnect in a driver-CNT bundle-load configuration will be discussed and analyzed. In this analysis, CNT bundle is modeled as a transmission line circuit model. At the end, a brief study of stability analysis in CNT interconnects will be presented.

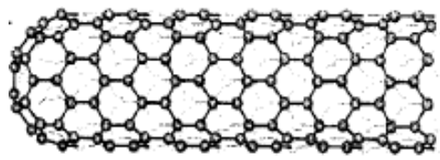
1. Interconnect Challenges in VLSI Circuits

As interconnect feature sizes shrink, copper resistivity increases due to surface and grain boundary scatterings and also surface roughness [1]. Furthermore, wires, especially power and ground lines, are becoming more and more vulnerable to electromigration because of rapid increases in current densities [2]. The resistance of copper interconnects, with cross-sectional dimensions of the order of the mean free path of electrons (~40 nm in Cu at room temperature) in current and imminent technologies [2], is increasing rapidly under the combined effects of enhanced grain boundary scattering, surface scattering and the presence of the highly resistive diffusion barrier layer [3]. The steep rise in parasitic resistance of copper interconnects poses serious challenges for interconnect delay [2] (especially at the global level where wires traverse long distances) and for interconnect reliability [4], hence it

has a significant impact on the performance and reliability of VLSI circuits. In order to alleviate such problems, changes in the material used for on-chip interconnections have been sought even in earlier technology generations, for example the transition from aluminum to copper some years back [3].
Carbon nanotubes (CNTs) exhibit a ballistic flow of electrons with electron mean free paths of several micrometers, and are capable of conducting very large current densities [3]. They are therefore proposed as potential candidates for signal and power interconnections [5], [6]. Because of their extremely desirable properties of high mechanical and thermal stability, high thermal conductivity and large current carrying capacity [7], CNTs have aroused a lot of research interest in their applicability as VLSI interconnects of the future. Depending on their chirality (the direction along which the graphene sheets are rolled up), CNTs demonstrate either metallic or semiconducting properties. Fig. 1 shows different structures depending on the chirality



Armchair_metallic



Zigzag_semiconducting

Fig. 1. Two different structures of carbon nanotubes for an armchair-type nanotube and a zigzag-type nanotube [8].

Carbon nanotubes are also classified into single-walled and multi-walled nanotubes.

2. Repeater Insertion as a Technique for the Delay Reduction

With the technology scaling in very deep submicron (VDSM) CMOS circuits, the gate delay decreases rapidly, while the delay of global interconnects tends to increase because of increasing their aspect ratio (thickness to width ratio) with scaling [2], [9], [10]. The repeater (buffer) insertion technique is generally used to reduce the delay of long (semi global) and global interconnects [9], [11]-[16]. An analytical model for obtaining the optimal buffer size and segment length for an equal partitioning network, in which the buffers sizes and segments lengths are constant, has been presented [12], [14], [17].
In [18] we have discussed about the optimization of global interconnects using unequal repeater (buffer) partitioning technique. This method which is discussed and reviewed in this chapter, is based on the segmentation of a long global interconnect into unequal parts, and inserting buffers with unequal sizes between them. The related structure is named as "*Unequal buffer partitioning network*" against "*Equal buffer partitioning network*" that was mentioned above. The optimum delay is a function of various parameters such as the

buffers sizes, the interconnect segments lengths, the load and so on [9], [11], [12], [15]-[17], [19]-[22]. It is shown that for the optimization of a buffer inserted interconnect behavior, the energy-delay product minimization is better than the delay minimization. Thus in this research, the energy-delay product has been chosen as target function for the minimization. There are different algorithms for minimizing a function, which in this chapter, the genetic algorithm (GA) using MATLAB [23] has been used for minimizing the energy-delay product function.

2.1 Equal Buffer Partitioning Network

Fig. 2 shows a global interconnect with the buffer insertion, in which each segment has equal length and all the buffers have the same size

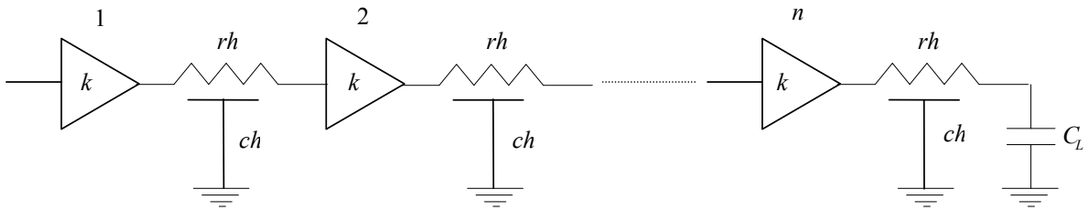


Fig. 2. Equal buffer partitioning network [18]

where r, c, and h are the interconnect resistance per unit length, the interconnect capacitance per unit length, and each segment length of the interconnect, respectively. Also k, n and C_L are the buffers size, the number of buffers, and the load capacitance, respectively. The total time delay of global line interconnect including the buffers and load, using Elmore relation [12], [21] will be

$$Delay_1 = n\left[R_{Bo}(C_{Bo}+ch)+\frac{1}{2}rch^2\right]+(n-1)\left(R_{Bo}+rh\right)C_{Bi}+\left(R_{Bo}+rh\right)C_L . \quad (1)$$

where $R_{Bo}=r_0/k$, $C_{Bi}=kc_0$, and $C_{Bo}=kc_p$ are the buffers output resistance, the buffers input capacitance, and the buffers output capacitance, respectively. Also r_0, c_0, and c_p are similar parameters of the minimum sized repeater (buffer), respectively. We can express the total energy as

$$Energy_1 = n\left[ch+k(c_0+c_p)+\frac{C_L}{n}\right]V_{dd}^2 \quad (2)$$

where V_{dd} is the power supply voltage. The energy-delay product will be written as

$$EDP_1 = Energy_1 \times Delay_1 , \quad (3)$$

$$EDP_1 = n^2\left[ch+k(c_0+c_p)+\frac{C_L}{n}\right]\times\left[\frac{r_0}{k}(kc_p+\frac{n-1}{n}kc_0+\frac{C_L}{n}+ch)+rh(\frac{n-1}{n}kc_0+\frac{C_L}{n}+\frac{1}{2}ch)\right]V_{dd}^2 . \quad (4)$$

2.2 Unequal Buffer Partitioning Network

Fig. 3 shows a global interconnect with buffer insertion, in which each segment length is *a* times of the previous segment length, and each buffer size is *f* times of the previous buffer size, respectively

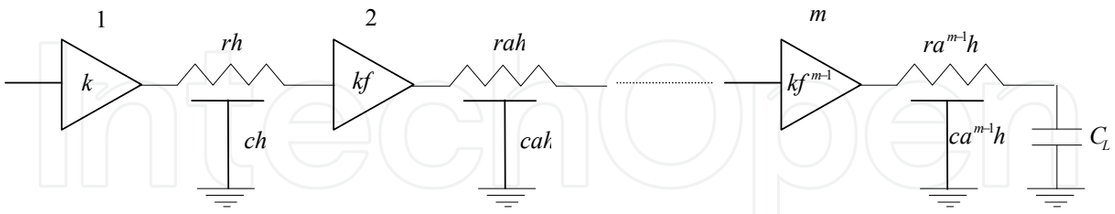


Fig. 3 Unequal buffer partitioning network [18]

where $h=l(1-a)/(1-a^m)$ which l is the total length of line (interconnect), k is the first buffer size, and m is the number of buffers. The other parameters are the same as in Fig.2. The total time delay of global interconnect in this structure, including the buffers and load, using Elmore relation [12], [21] will be

$$Delay_2 = mr_0c_p + (m-1)r_0c_0f + \left(\frac{1-\left(\frac{a}{f}\right)^m}{1-\frac{a}{f}}\right)\frac{r_0}{k}ch + \left(\frac{1-(af)^{m-1}}{1-af}\right)rhkfc_0 + \frac{1}{2}\left(\frac{1-a^{2m}}{1-a}\right)rch^2 + \left(\frac{r_0}{kf^{m-1}} + ra^{m-1}h\right)C_L \quad (5)$$

where r_0, c_0, and c_p are the output resistance, the input capacitance, and the output capacitance of the minimum sized buffer, respectively. We can express the total energy as

$$Energy_2 = \left[cl + \left(\frac{1-f^m}{1-f}\right)k(c_0 + c_p) + C_L\right]V_{dd}^2 . \quad (6)$$

Thus the energy-delay product for "*Unequal partitioning network*" will be written as

$$EDP_2 = Energy_2 \times Delay_2 , \quad (7)$$

$$EDP_2 = \left[cl + \left(\frac{1-f^m}{1-f}\right)k(c_0 + c_p) + C_L\right]$$

$$\times\left[mr_0c_p + (m-1)r_0c_0f + \left(\frac{1-\left(\frac{a}{f}\right)^m}{1-\frac{a}{f}}\right)\frac{r_0}{k}ch + \left(\frac{1-(af)^{m-1}}{1-af}\right)rhkfc_0 + \frac{1}{2}\left(\frac{1-a^{2m}}{1-a}\right)rch^2 + \left(\frac{r_0}{kf^{m-1}} + ra^{m-1}h\right)C_L\right]V_{dd}^2 . \quad (8)$$

2.3 Optimization Procedure

In this section, EDP[1] functions for the two networks "*Equal partitioning network*" and "*Unequal partitioning network*", which are defined and obtained in sections II and III, are minimized using the genetic algorithm (GA) of MATLAB [23]. This procedure is performed on the two networks for the three technology nodes 65, 90, 130 nm, which the specifications of global interconnect and the minimum sized repeater (buffer) in each technology node have been extracted from ITRS[2] [2], [9]. Also the interconnect capacitance per unit length is obtained using the formulations presented in [9]. Moreover, in each step of the optimization (minimization) procedure, the load capacitance has been taken as a parameter which varies from one to hundred times of the minimum sized buffer output capacitance.

In Figs. 4-9, the propagation delay improvement for "*Unequal partitioning network*" respect to "*Equal partitioning network*", versus the global interconnect length, and for three technology nodes 65, 90 , 130 nm, have been plotted whereas the capacitive load varies from one to hundred times of the minimum sized buffer output capacitance (c_p). The genetic algorithm (GA) of MATLAB [23] has been used as a tool for minimizing the energy-delay product (EDP) for the two networks at different technology nodes and various loads. For obtaining the correct results for each step of the minimization procedure, the algorithm has been done 1000 times in each step and the least value has been chosen as the best answer.

It is found from Figs. 4-9 that the improvement of the propagation delay, in unequal partitioning network is more than equal partitioning network. This improvement is obvious for the technology nodes 90, 130 nm and goes high with increasing the load capacitance. Also for technology node 65 nm, the delay improvement will be achieved for the high values of the load capacitance, which is cleared from Figs. 8, 9.

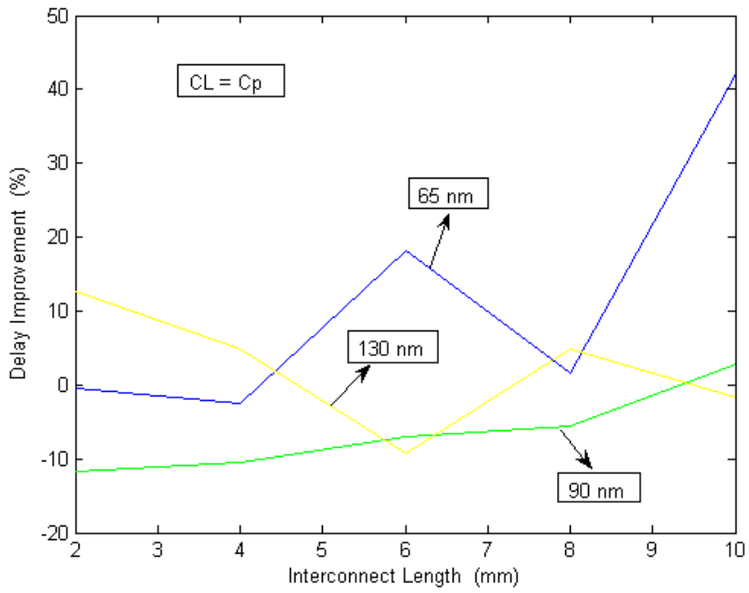


Fig. 4. The delay improvement of unequal partitioning network respect to equal partitioning network, for C_L=c_p [18].

[1] Energy-Delay Product

[2] International Technology Roadmap for Semiconductors

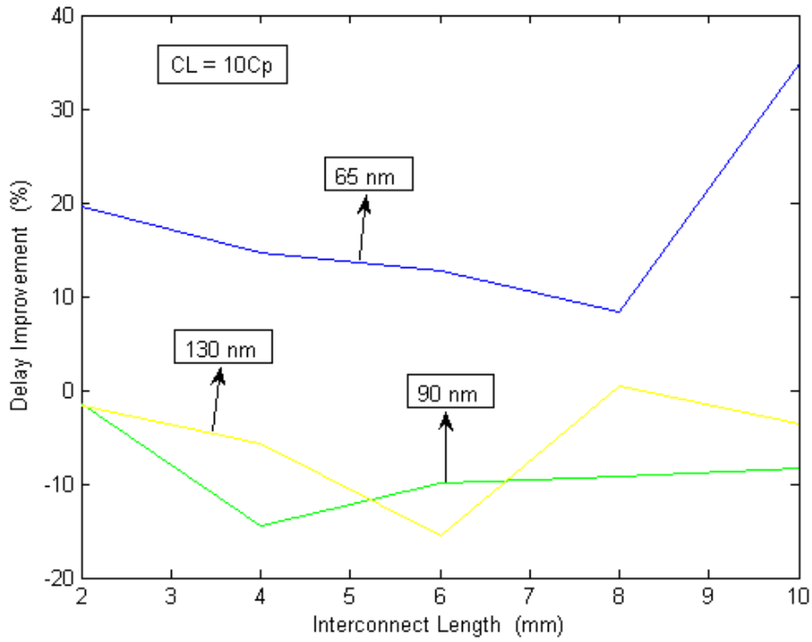


Fig. 5. The delay improvement of unequal partitioning network respect to equal partitioning network, for C_L=10c_p [18].

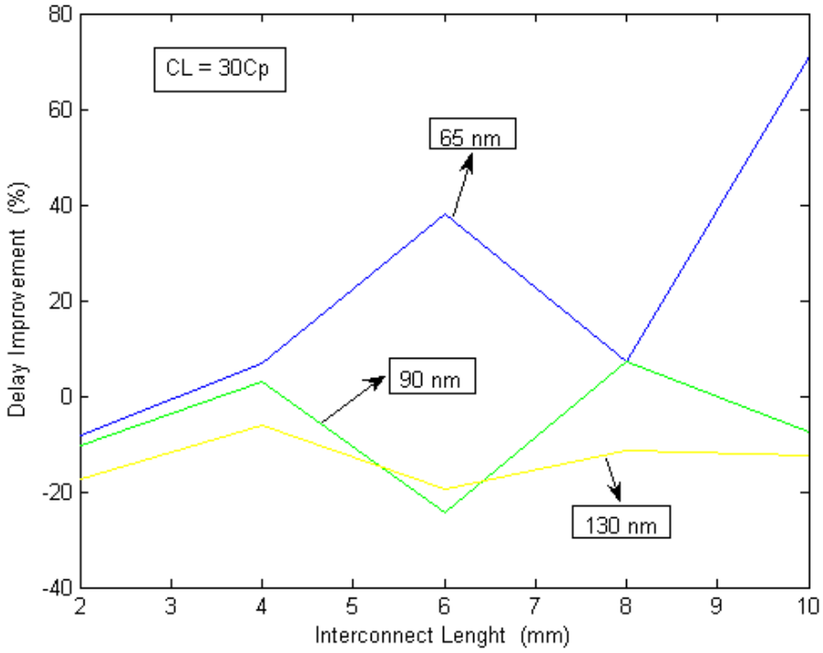


Fig. 6. The delay improvement of unequal partitioning network respect to equal partitioning network, for C_L=30c_p [18].

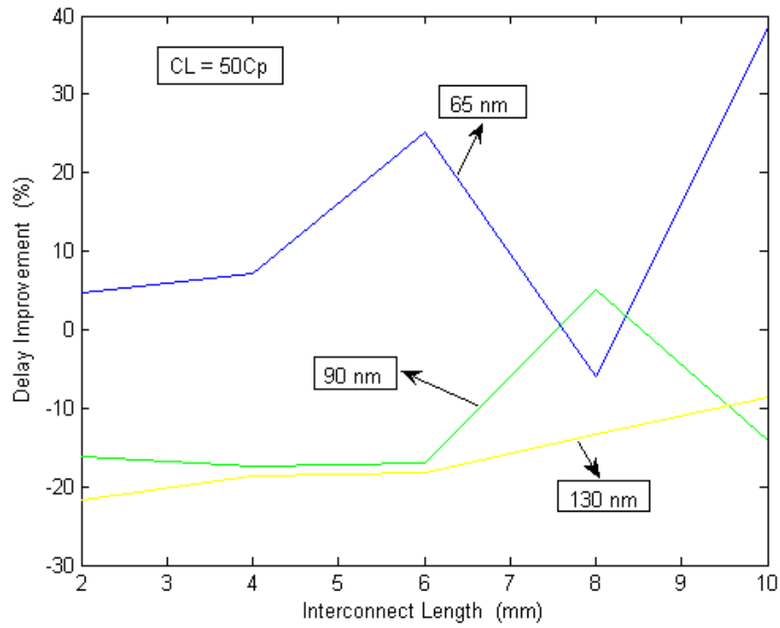


Fig. 7. The delay improvement of unequal partitioning network respect to equal partitioning network, for $C_L=50c_p$ [18].

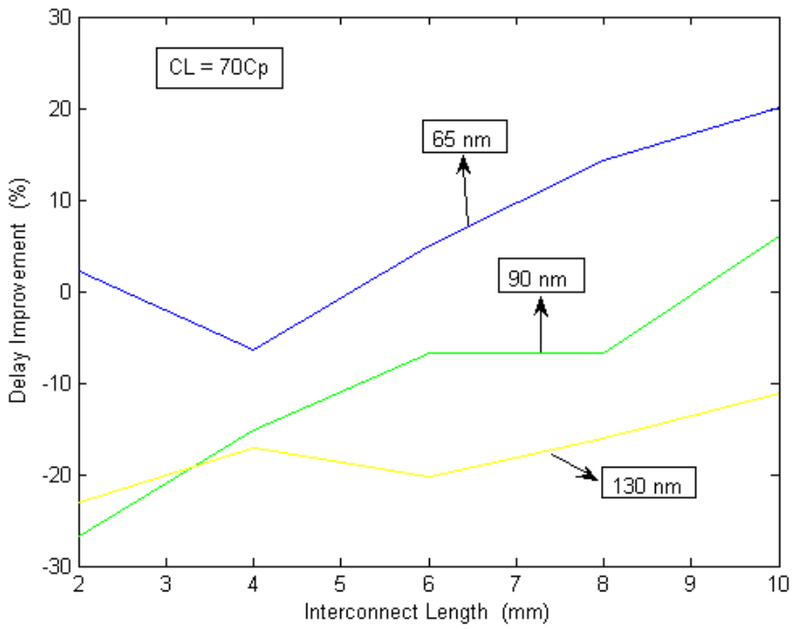


Fig. 8. The delay improvement of unequal partitioning network respect to equal partitioning network, for $C_L=70c_p$ [18].

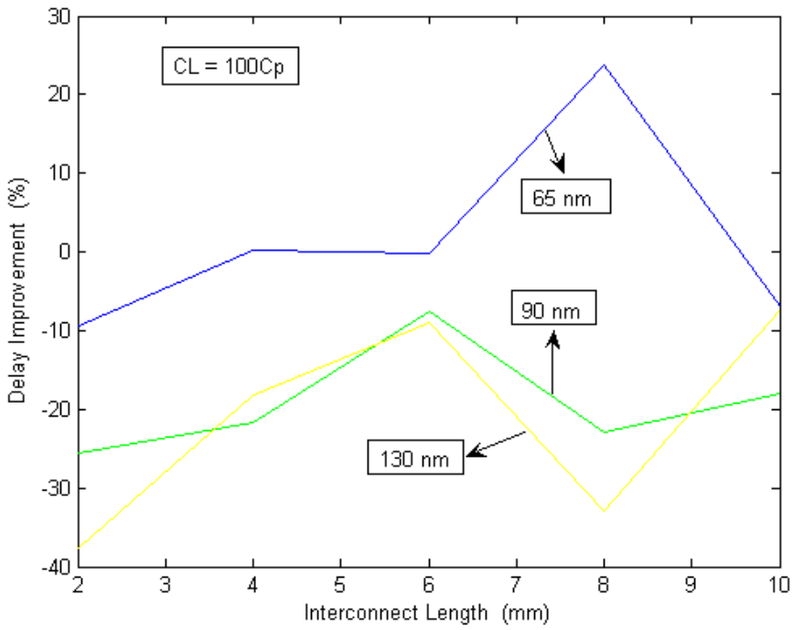


Fig. 9. The delay improvement of unequal partitioning network respect to equal partitioning network, for $C_L=100c_p$ [18].

3. Circuit Model and Parameters for CNT

Fig. 10 depicts the equivalent circuit for an isolated single-walled carbon nanotube (SWCNT) of length less than the mean free path of electrons in a CNT [24], [25].

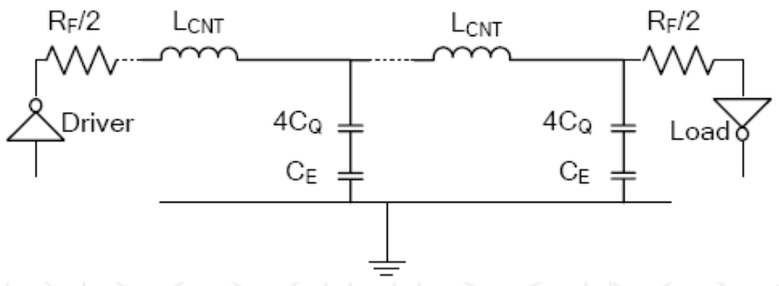


Fig. 10. Equivalent circuit model for an isolated SWCNT of length less than the mean free path of electrons, assuming ideal contacts [25].

In this figure, R_F is the fundamental (quantum) resistance, L_{CNT} is the total inductance, and C_Q and C_E are the quantum and electrostatic capacitances, respectively. In the following subsections, these parameters and their related formulations will be discussed.

3.1. CNT Resistance

Due to spin degeneracy and sub-lattice degeneracy of electrons in graphene, each nanotube has four conducting channels in parallel [3], [26]. Hence, the conductance of an isolated

ballistic single-walled CNT (SWCNT) assuming perfect contacts, is $4e^2/h$ = 155 μS, which yields a resistance of 6.45 KΩ [8], [24]. This is the quantum resistance associated with a SWCNT that cannot be avoided [3], [27]. This fundamental resistance, as shown in Fig. 11, is equally divided between the two contacts on either side of the nanotube and can be expressed as [27]

$$R_F = \frac{h}{4e^2} \tag{9}$$

where h is plank's constant and e is electron charge. The mean free path (MFP) of electrons in a CNT is typically 1 μm [3], [8], [28]. For CNT lengths less than λ_{CNT}, electron transport within the nanotube is essentially ballistic [3]. In this case, the resistance of nanotube with ideal coupling to the two metal contacts at its ends is independent of length and is given by $h/(4e^2) \approx 6.45$ KΩ [26], [27]. However, for lengths greater than the mean free path, scattering leads to an additional ohmic resistance which increases with length as [29]

$$R_{CNT} = R_F \frac{\ell}{\lambda_{CNT}} = \left(\frac{h}{4e^2}\right)\frac{\ell}{\lambda_{CNT}} \tag{10}$$

where ℓ and λ_{CNT} are the length and the mean free path of CNT, respectively. This has also been confirmed by experimental observations [3], [28]. It should be noted that this additional scattering resistance would appear as a distributed resistance per unit length [24] in the equivalent circuit, to account for resistive losses along the CNT length

$$R_{CNT}(p.u.l) = \frac{R_F}{\lambda_{CNT}} = \left(\frac{h}{4e^2}\right)\frac{1}{\lambda_{CNT}}. \tag{11}$$

It is necessary to note that there are inconsistent results published in literature, both experimental and theoretical, regarding the dependency of resistance on length [30]. Some of these results indicate an exponential relationship [31], [32]

$$R = R_F \exp\left(\frac{\ell}{2\lambda_{CNT}}\right) \tag{12}$$

and some show a linear dependency [28], [33]

$$R = R_F\left(1 + \frac{\ell}{\lambda_{CNT}}\right). \tag{13}$$

It can be observed from (10)-(13) that the value of mean free path (MFP) plays an important role in determining the resistance of the carbon nanotube. It has been proven that the MFP of a CNT, both for metallic and semiconductor types, is proportional to the diameter [34], [35]. For the MFP of metallic CNTs, we have [34], [36]

$$\lambda_{CNT} = \left(\frac{\sqrt{3}\pi\phi^2}{2\sigma_\varepsilon^2 + 9\sigma_\phi^2} \right).D \tag{14}$$

where D is the diameter of the CNT, φ is the nearest neighbor tight-binding parameter, ε is the on-site energies, and σ_ε and σ_φ are the variances of ε and φ, respectively. For the MFP of semiconducting CNTs, we have [34], [35]

$$\lambda_{CNT} = \left(\frac{v_F}{\alpha T} \right).D \tag{15}$$

where v_F is the Fermi velocity, a is the coefficient of scattering rate, and T is the temperature. For a typical SWCNT with diameter 1 nm, the value of MFP has been reported about 1 μm based on measurements [37], [38]. Thus irrespective of the nature of SWCNTs (shells in an MWCNT), metallic or semiconducting, we can assume $\lambda_{CNT} \approx 1000D$ [34].

Fig. 11 shows the equivalent distributed circuit model of an individual CNT (shell in a multi-walled CNT)

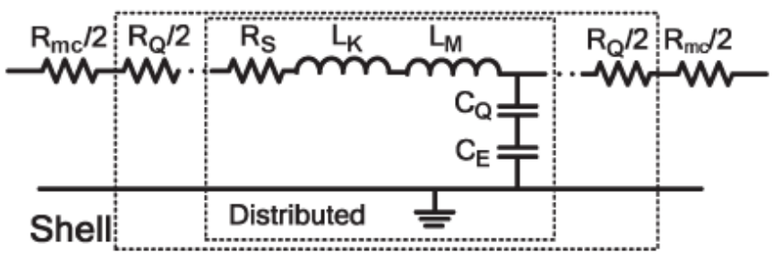


Fig. 11. Equivalent distributed circuit model of an individual CNT [34].

In this figure, R_{mc} is the imperfect contact resistance, R_Q is the quantum resistance (as the fundamental resistance R_F in Fig. 10), R_S is the scattering-induced resistance (as R_{CNT} in (10), (11)), L_K and L_M are the kinetic and magnetic inductances, respectively, and C_Q and C_E are the quantum and electrostatic capacitances, respectively.

The imperfect metal-to-nanotube contacts at each of the two ends of the nanotube, give rise to an additional resistance typically about 100 KΩ in series with the fundamental resistance R_F [24], [39].

3.2. CNT Capacitance

The total capacitance of a CNT arises from two sources: the electrostatic capacitance which is the intrinsic plate capacitance of an isolated CNT, and the quantum capacitance which accounts for the quantum electrostatic energy stored in the nanotube when it carries current [3], [26].

The electrostatic capacitance is calculated by treating the CNT as a thin wire placed away from a ground plane, as shown in Fig. 12, and its value per unit length is given by [3], [26], [30]

$$C_E = \frac{2\pi\varepsilon}{\cosh^{-1}\left(\frac{2y}{d}\right)} \approx \frac{2\pi\varepsilon}{\ln\left(\frac{y}{d}\right)} \tag{16}$$

where ε, d and y are the dielectric permittivity, the CNT diameter, and the distance of CNT from the ground plane, respectively.

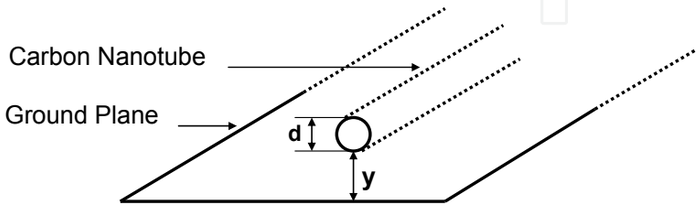


Fig. 12. Structure of an isolated CNT over a ground plane.

The electron cloud in a CNT can be assumed to be a quantum electron gas in one dimension. Hence, this follows Pauli's exclusion principle and it is not possible to add an electron with energy less than the Fermi energy of the system (E_F) [40]. The quantum capacitance is used to model the energy needed to add an electron at an available quantum state above the Fermi level [26]. By equating this energy to that of an effective capacitance, the expression for the quantum capacitance per unit length is obtained as [25]

$$C_Q = \frac{2e^2}{hv_F} \tag{17}$$

where v_F is the Fermi velocity in graphite [40] and is approximately 8×10^5 m/s [25]. Also for a CNT, C_Q is approximately 100 aF/μm [25], [26]. Since a CNT has four conducting channels as described before, the effective quantum capacitance resulting from four parallel capacitances is given by 4 C_Q.

In [34], the following relations for the quantum capacitance per unit length of a shell in a MWCNT have been expressed, according to the result in [25]

$$C_{Q/channel} = 2\times\frac{2e^2}{hv_F} \approx 193 \text{ aF}/\mu\text{m}, \tag{18}$$

$$C_{Q/shell} = C_{Q/channel} \times N_{shell}(D), \tag{19}$$

where

$$N_{shell}(D) \approx a.D + b \qquad D > 3 \text{ nm} \tag{20}$$

is the number of conducting channels (spin degeneracy is already considered) in any shell, D is the diameter of the shell, a = 0.0612 nm^{-1}, and b = 0.425.

On the other hand, in [38], the following relation for the number of conducting channels in any shell has been reported

$$N_{shell}(D) \approx a.D + b \qquad D > 3 \text{ nm}$$
$$\approx \frac{2}{3} \qquad D < 6 \text{ nm}. \tag{21}$$

It should be noted that the error introduced by (20), (21), due to different chiralities, is within 15% for all values of D [34], [38]. Note that the two regions in (21) have an overlap, and for 3 nm < D < 6 nm, both constant and linear functions can be used without any considerable error [38].

3.3. CNT Inductance

The total inductance of a CNT (L_{CNT} in Fig. 10) arises from two sources: the magnetic inductance and the kinetic inductance (L_M and L_K in Fig. 11). In the presence of a ground plane, the magnetic inductance per unit length is given by [25], [40]

$$L_M = \frac{\mu}{2\pi}\cosh^{-1}\left(\frac{2y}{d}\right) \approx \frac{\mu}{2\pi}\ln\left(\frac{y}{d}\right). \tag{22}$$

For a typical situation, the nanotube is placed on top of an insulating substrate (typically silicon dioxide), with a conducting medium below. A typical oxide thickness is between 10 nm and 1 μm with a typical nanotube radius of 1 to 2 nm. It can be noted that the magnetic inductance is a relatively weak function of the factor (y/d) and for typical geometries, it can be estimated to be around 1 pH/μm [40], [41].

In one-dimensional CNT conductors, apart from the magnetic inductance, another inductive component appears due to the kinetic energy of the electrons. The details of its derivation can be obtained in [40]-[42]. The kinetic inductance per unit length can be expressed as [25], [40], [41]

$$L_K = \frac{h}{2e^2 v_F}. \tag{23}$$

It is necessary to note that the four parallel conducting channels in a CNT give rise to an effective kinetic inductance of L_K /4. Also as it has been shown from (23), the kinetic inductance per unit length for a one dimensional CNT conductor is around 16 nH/μm [26], [40], more than 4 orders of magnitude larger than its magnetic counterpart L_M (≈ 1 pH/μm) [30], [40], [41], and will essentially play a vital role in high frequency applications [40].

In [34], the following relations for the kinetic inductance per unit length of a shell in a MWCNT have been expressed, according to the result in [25]

$$L_{K/channel} = \frac{h}{2e^2 v_F} \times \frac{1}{2} \approx 8 \text{ nH}/\mu\text{m} , \tag{24}$$

$$L_{K/shell} = \frac{L_{K/channel}}{N_{shell}(D)} \tag{25}$$

where N_{shell} (D) has been defined in (20), (21).

4. Different Structures of CNT as Interconnect

4.1. CNT Bundle as Interconnect

While SWCNTs have desirable material properties, individual nanotubes suffer from an intrinsic ballistic resistance of approximately 6.5 kΩ that is not dependent on the length of the nanotube [43]. As a result, the high resistance associated with an isolated CNT, causes excessive delay for interconnect applications. To alleviate the intrinsic resistance problem, bundles or ropes of CNTs conducting current in parallel, have been proposed and physically demonstrated as a possible interconnect medium for local, intermediate, and global interconnects [3], [43]. Fig. 13 shows a CNT bundle interconnect structure consists of a signal line and two ground return paths

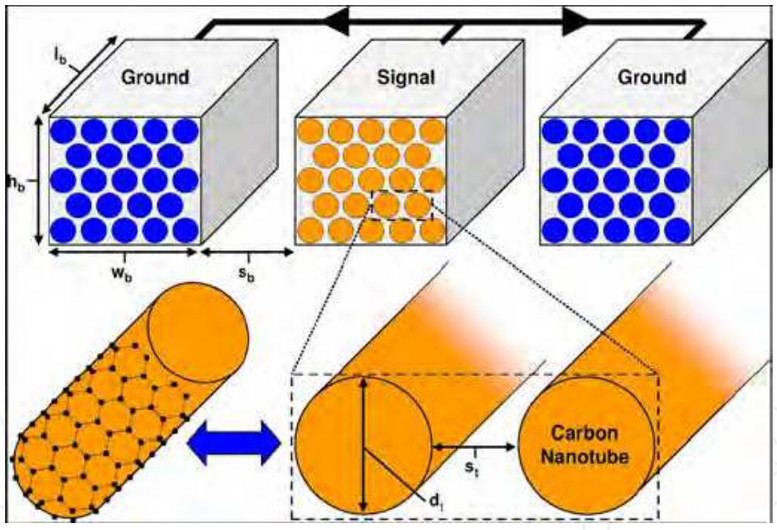


Fig. 13. System of SWCNT interconnect bundles implementing a signal line and two adjacent ground return paths [43].

Due to the lack of control on chirality, any bundle of CNTs consists of metallic as well as semi-conducting nanotubes. The required relations for the parameters of CNT bundles including the magnetic and kinetic inductances, the electrostatic and quantum capacitances, the fundamental and scattering resistances, can be obtained from [5]. In section 5 the time domain behaviour of a CNT bundle as interconnect is discussed based on [44].

4.2. Multi-walled CNT as Interconnect

Fig. 14 shows a geometric structure of a Multi-Walled carbon nanotube (MWCNT) over a ground plane.

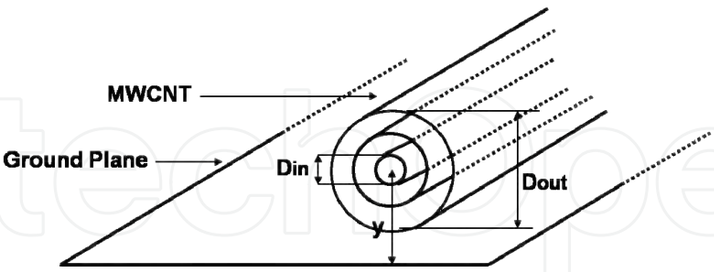


Fig. 14. Structure of a Multi-Walled CNT over a ground plane.

In this figure, D_{in} and D_{out} are the diameter of inner shell and the diameter of outer shell, respectively, and y is the height of inner shell from the ground plane. Recently wide spread studies regarding the benefits of the performance of MWCNTs as interconnect in comparison with CNT bundles and Cu have been performed. In [34] the performance of MWCNT interconnects has been analyzed and their circuit modelling has been discussed. Although MWCNT has an important role in the interconnect applications, the main scope of this chapter which follows in the subsequent section, is dedicated to the analysis of the behaviour of CNT bundle interconnects.

5. Time Domain Response

In [44] we have discussed about the time domain analysis of a CNT bundle interconnect in a driver-interconnect-load configuration and a new relation for the input-output transfer function in the related configuration has been extracted. A review of the discussion presented in [44] is brought in this section. Fig. 15 shows a CNT bundle interconnect with resistance, capacitance and inductance per unit length of R_S , C and L respectively, driven by a repeater of output resistance R_{tr} and output parasitic capacitance C_{out}, and driving an identical repeater with input capacitance equal to the load capacitance C_L.

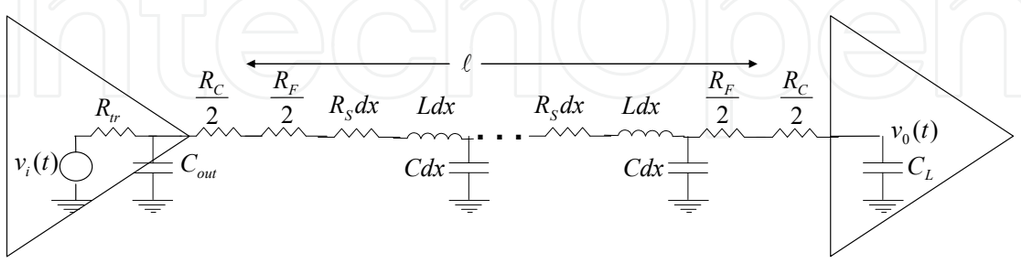


Fig. 15. Equivalent circuit of a driver-CNT bundle-load configuration, based on transmission line modeling [44].

In this figure, the CNT bundle interconnect has been modelled as a transmission line. For calculating the input-output transfer function of the configuration in Fig. 15, we need to

derivate the total transmission parameter matrix. Using the ABCD transmission parameter matrix for a uniform RLC transmission line of length ℓ as given in [45]-[47], we can express the total ABCD transmission parameter matrix of the configuration in Fig. 15 as

$$T_{total}=\begin{bmatrix}1 & R_{tr}\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ sC_{out} & 1\end{bmatrix}\begin{bmatrix}1 & R_{ex}\\ 0 & 1\end{bmatrix}\begin{bmatrix}\cosh(\theta^T\ell) & Z_0^T\sinh(\theta^T\ell)\\ \frac{1}{Z_0^T}\sinh(\theta^T\ell) & \cosh(\theta^T\ell)\end{bmatrix}\begin{bmatrix}1 & R_{ex}\\ 0 & 1\end{bmatrix} \tag{26}$$

where $R_{ex}=(R_C+R_F)/2$, $Z_0^T=\sqrt{(R_S+sL)/(sC)}$, $\theta^T=\sqrt{(R_S+sL)sC}$, and $s=j\omega$ is the complex frequency. The elements of matrix T_{total} can be written, using (26), as

$$A_T=(1+sR_{tr}C_{out})\cosh(\theta^T\ell)+\frac{(R_{tr}+R_{ex}+sR_{tr}R_{ex}C_{out})}{Z_0^T}\sinh(\theta^T\ell), \tag{27}$$

$$B_T=[R_{tr}+2R_{ex}+2sR_{tr}R_{ex}C_{out}]\cosh(\theta^T\ell)+[Z_0(1+sR_{tr}C_{out})+\frac{R_{ex}(R_{tr}+R_{ex}+sR_{tr}R_{ex}C_{out})}{Z_0^T}]\sinh(\theta^T\ell), \tag{28}$$

$$C_T=sC_{out}\cosh(\theta^T\ell)+\frac{1+sR_{ex}C_{out}}{Z_0^T}\sinh(\theta^T\ell), \tag{29}$$

$$D_T=(1+2sR_{ex}C_{out})\cosh(\theta^T\ell)+[sC_{out}Z_0^T+\frac{R_{ex}(1+sR_{ex}C_{out})}{Z_0^T}]\sinh(\theta^T\ell). \tag{30}$$

Therefore the input-output transfer function of the configuration in Fig. 15 can be written as

$$H(s)=\frac{V_0(s)}{V_i(s)}=\frac{1}{A_T+sC_LB_T}=\left(\begin{array}{l}[1+s(R_{tr}C_{out}+R_{tr}C_L+2R_{ex}C_L)+s^2(2R_{tr}R_{ex}C_{out}C_L)]\cosh(\theta^T\ell)\\ +\left[\begin{array}{l}\frac{R_{tr}+R_{ex}}{Z_0^T}+s\left(\frac{R_{tr}R_{ex}C_{out}+R_{ex}(R_{tr}+R_{ex})C_L}{Z_0^T}+Z_0^TC_L\right)\\ +s^2\left(\frac{R_{tr}R_{ex}^2C_{out}}{Z_0^T}+Z_0^TR_{tr}C_{out}\right)C_L\end{array}\right]\sinh(\theta^T\ell)\end{array}\right)^{-1}. \tag{31}$$

For simulation purposes, we need to extract a parametric linear approximation for (31). For this purpose, we need to calculate the equivalent linear terms for $\cosh(\theta^T\ell)$ and $\sinh(\theta^T\ell)/Z_0^T$, and put them in (31). Using the relation for the transfer function of a driver-CNT interconnect-load configuration, as discussed in [47], and rigorous calculations, we can extract the following linear expressions

$$\cosh(\theta^T \ell) = 1 + \left(\frac{R_S C \ell^2}{2!}\right) s + \left(\frac{LC\ell^2}{2!} + \frac{R_S^2 C^2 \ell^4}{4!}\right) s^2$$

$$+ \left(\frac{2R_S LC^2 \ell^4}{4!} + \frac{R_S^3 C^3 \ell^3}{6!}\right) s^3 + \left(\frac{L^2 C^2 \ell^4}{4!} + \frac{3R_S^2 LC^3 \ell^6}{6!} + \frac{R_S^4 C^4 \ell^8}{8!}\right) s^4, \tag{32}$$

$$\frac{\sinh(\theta^T \ell)}{Z_0^T} = sC\ell \left[1 + \frac{R_S C \ell^2}{3!} s + \left(\frac{LC\ell^2}{3!} + \frac{R_S^2 C^2 \ell^4}{5!}\right) s^2 + \left(\frac{R_S^3 C^3 \ell^6}{7!} + \frac{2R_S LC^2 \ell^4}{5!}\right) s^3\right]. \tag{33}$$

With substituting the two terms $\cosh(\theta^T \ell)$ and $\sinh(\theta^T \ell) / Z_0^T$ in (31), by (32) and (33), we can obtain the linear parametric equivalent for the transfer function of (31) as

$$H(s) = \frac{1}{1 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4 + a_5 s^5 + a_6 s^6} \tag{34}$$

where

$$a_1 = R_{tr}(C_{out} + C\ell + C_L) + R_{ex}(C\ell + 2C_L) + R_S \ell \left(\frac{C\ell}{2!} + C_L\right), \tag{35}$$

$$a_2 = R_{ex} R_{tr}(C_{out} C\ell + C_L C\ell + 2C_{out} C_L) + R_{tr} R_S C\ell^2 \left(\frac{C_{out} C\ell}{2!} + \frac{C^2 \ell^2}{3!} + C_{out} C_L + \frac{C\ell C_L}{2!}\right)$$

$$+ R_{ex} R_S C\ell^2 \left(\frac{C\ell}{3!} + C_L\right) + \frac{R_S^2 C^2 \ell^4}{4!} + \frac{LC\ell^2}{2!} + R_{ex}^2 C\ell C_L + \frac{R_S^2 C\ell^3 C_L}{3!} + L\ell C_L, \tag{36}$$

$$a_3 = \frac{2R_S LC^2 \ell^4}{4!} + \frac{R_S^3 C^3 \ell^6}{6!} + \left(R_{ex} + R_{tr} + \frac{R_S}{C} C_L\right)\left(\frac{LC^2 \ell^3}{3!} + \frac{R_S^2 C^3 \ell^5}{5!}\right)$$

$$+ [R_{tr}(C_{out} + C_L) + 2R_{ex} C_L]\left(\frac{LC\ell^2}{2!} + \frac{R_S^2 C^2 \ell^4}{4!}\right)$$

$$+ \frac{R_S C^2 \ell^3}{3!}\left(R_{ex} R_{tr}(C_{out} + C_L) + R_{ex}^2 C_L + \frac{L}{C} C_L + \frac{R_S}{C} R_{tr} C_{outL}\right)$$

$$+ R_{ex} R_{tr} C_{out} C\ell C_L (R_{ex} + R_S \ell) + R_{tr} C_{out} L\ell C_L, \tag{37}$$

$$a_4=\frac{L^2C^2\ell^4}{4!}+\frac{3R_S^2LC^3\ell^6}{6!}+\frac{R_S^4C^4\ell^8}{8!}+[R_{tr}(C_{out}+C_L)+2R_{ex}C_L]\left(\frac{2R_SLC^2\ell^4}{4!}+\frac{R_S^3C^3\ell^6}{6!}\right)$$
$$+\left(R_{tr}+R_{ex}+\frac{R_S}{C}C_L\right)\left(\frac{2R_SLC^3\ell^5}{5!}+\frac{R_S^3C^4\ell^7}{7!}\right)+2R_{tr}R_{ex}C_{out}C_L\left(\frac{LC\ell^2}{2!}+\frac{R_S^2C^2\ell^4}{4!}\right)$$
$$+\left(R_{tr}R_{ex}(C_{out}+C_L)+R_{ex}^2C_L+\frac{L}{C}C_L+\frac{R_S}{C}R_{tr}C_{out}C_L\right)\left(\frac{LC^2\ell^3}{3!}+\frac{R_S^2C^3\ell^5}{5!}\right)$$
$$+\frac{R_SC^2\ell^3}{3!}\left(R_{tr}R_{ex}^2C_{out}C_L+\frac{L}{C}R_{tr}C_{out}C_L\right), \tag{38}$$

$$a_5=[R_{tr}(C_{out}+C_L)+2R_{ex}C_L]\left(\frac{L^2C^2\ell^4}{4!}+\frac{3R_S^2LC^3\ell^6}{6!}+\frac{R_S^4C^4\ell^8}{8!}\right)$$
$$+2R_{tr}R_{ex}C_{out}C_L\left(\frac{2R_SLC^2\ell^4}{4!}+\frac{R_S^3C^3\ell^6}{6!}\right)$$
$$+\left(R_{tr}R_{ex}(C_{out}+C_L)+R_{ex}^2C_L+\frac{L}{C}C_L+\frac{R_S}{C}R_{tr}C_{out}C_L\right)\left(\frac{2R_SLC^3\ell^5}{5!}+\frac{R_S^3C^4\ell^7}{7!}\right)$$
$$+\left(R_{tr}R_{ex}^2C_{out}C_L+\frac{L}{C}R_{tr}C_{out}C_L\right)\left(\frac{LC^2\ell^3}{3!}+\frac{R_S^2C^3\ell^5}{5!}\right), \tag{39}$$

$$a_6=2R_{tr}R_{ex}C_{out}C_L\left(\frac{L^2C^2\ell^4}{4!}+\frac{3R_S^2LC^3\ell^6}{6!}+\frac{R_S^4C^4\ell^8}{8!}\right)$$
$$+\left(R_{tr}R_{ex}^2C_{out}C_L+\frac{L}{C}R_{tr}C_{out}C_L\right)\left(\frac{2R_SLC^3\ell^5}{5!}+\frac{R_S^3C^4\ell^7}{7!}\right). \tag{40}$$

Fig. 16 shows the step response of configuration in Fig. 15, for 32 nm technology node, using our extracted linear transfer function of (34), and HSPICE simulation.

The repeater size has been assumed 174 times larger than the minimum sized repeater, which its parameters have been extracted from ITRS 2007 [2]. Also the load capacitance has been considered equal to the input capacitance of repeater. Recall that $\lambda_{CNT}\approx 1000D$ [34] where D is the diameter of each individual CNT, the mean free path of CNT (λ_{CNT}) has been assumed 1 μm. As it is cleared from Fig. 16, there is an excellent match between the result of our extracted parametric transfer function and HSPICE simulation result. Fig. 17 shows the step response of configuration in Fig. 15, using our extracted linear parametric transfer function of (34), for the contact resistance values from 1 kΩ to 50 kΩ. As shown in Fig. 17, the propagation delay increases from 0.138 ns to 5.58 ns, with the increase of contact resistance value from 1 kΩ to 50 kΩ.

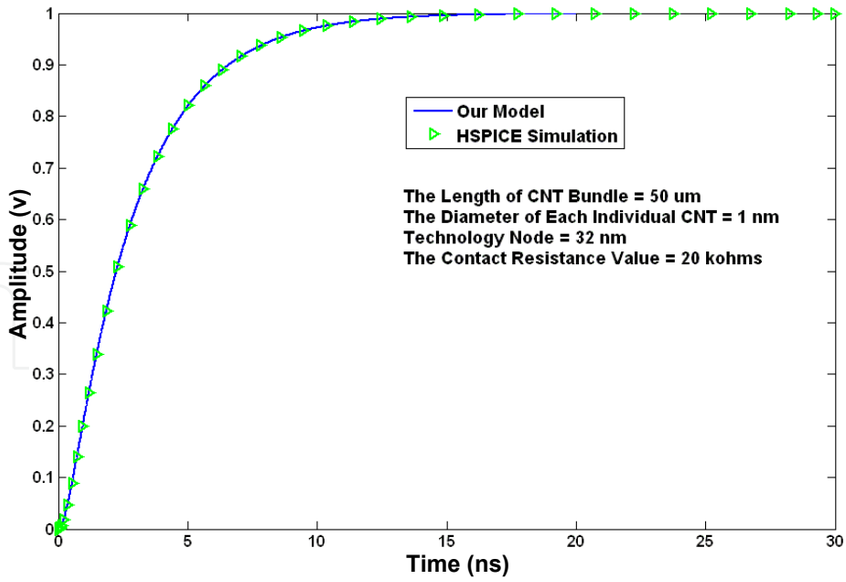


Fig. 16. The step response of configuration in Fig. 15, using our extracted linear parametric transfer function, and HSPICE simulation. In this figure, the number of transmission line model sections for HSPICE simulation, has been considered 400 [44].

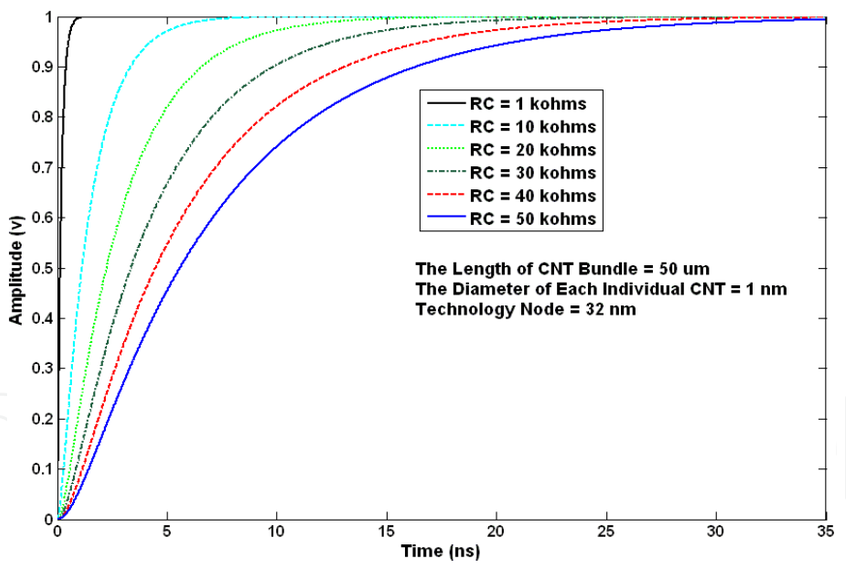


Fig. 17. The step response of configuration in Fig. 15, using our extracted linear parametric transfer function, for various values of the contact resistance [44].

Fig. 18 shows the propagation delay of configuration in Fig. 15, using our extracted linear parametric transfer function of (34), versus the contact resistance value, and for the CNT bundle lengths 50 μm, 200 μm, 500 μm and 1000 μm.

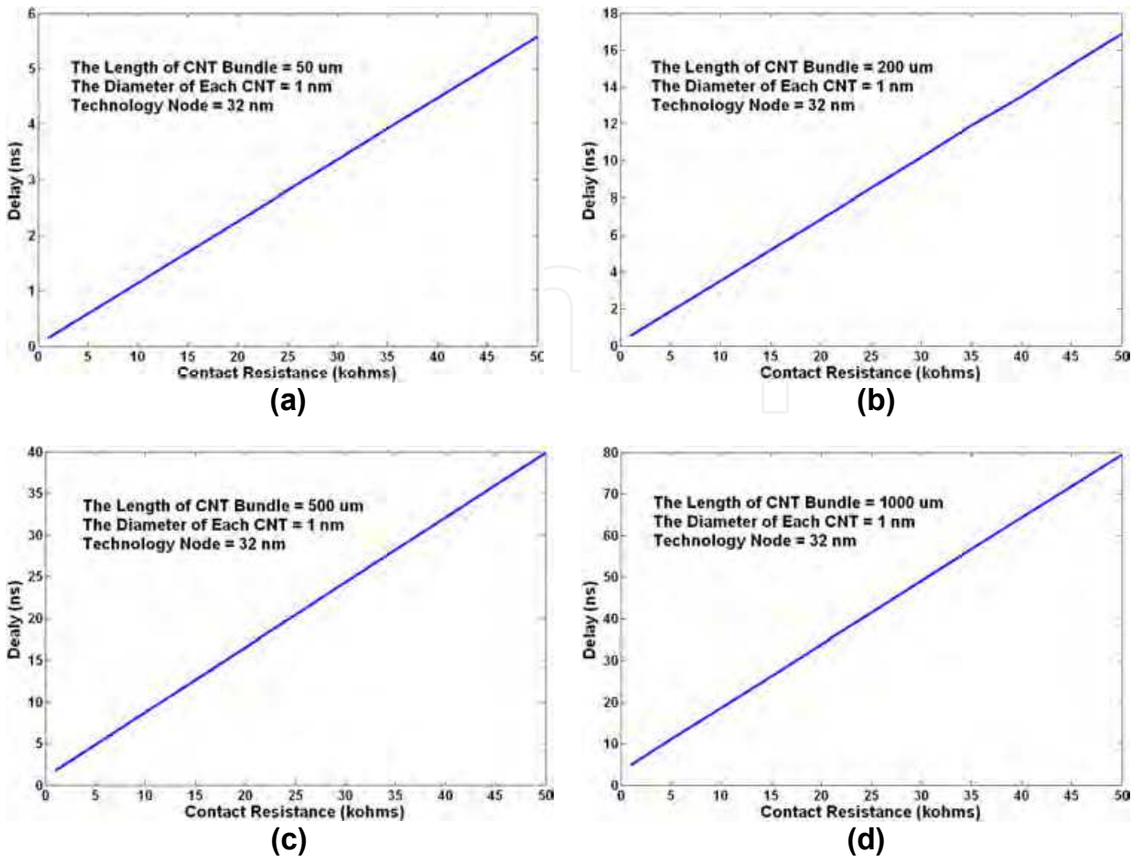


Fig. 18. The propagation delay of configuration in Fig. 15, using our new linear parametric transfer function, versus the contact resistance value, for the CNT bundle lengths: (a) 50 μm, (b) 200 μm, (c) 500 μm, (d) 1000 μm [44].

In this figure, the diameter of each individual CNT has been chosen 1 nm, and therefore as discussed before, the mean free path of CNT will be 1 μm. As shown in Fig. 18, for the length of CNT bundle equal to 50 μm, the propagation delay changes from 0.138 ns to 5.58 ns for the contact resistance values from 1 kΩ to 50 kΩ, i.e. a variation range of 39.43 times the minimum value. The related delay variation ranges for the length values 200 μm, 500 μm, and 1000 μm, are 31.37, 22.61, and 15.42 times the minimum value, respectively. This means that, the impact of the contact resistance on the propagation delay, decreases with the increase of the bundle length. The reason is that, with the increase of the bundle length, the role of scattering resistance which increases with the length [29], would be more important.
In Fig. 19, the nyquist diagrams for a driven CNT bundle interconnect, versus the length of CNT bundle and the diameter of each individual CNT, have been plotted using MATLAB [23].

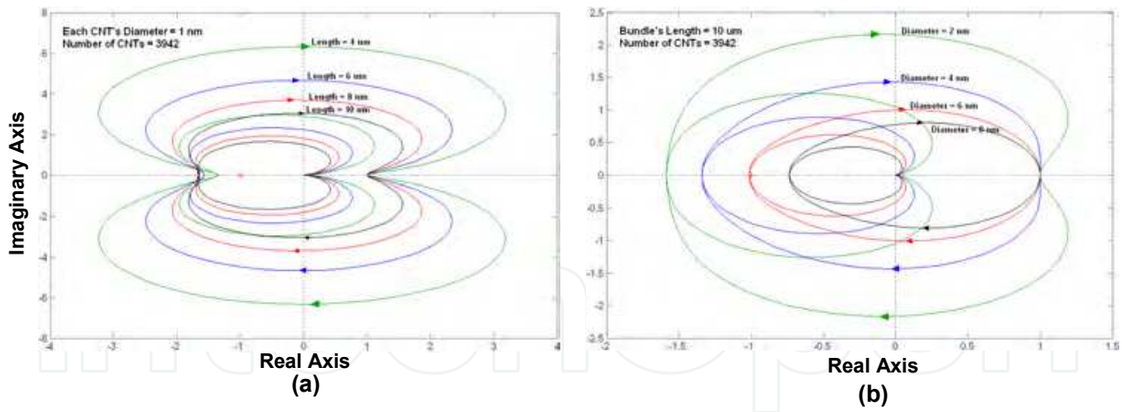


Fig. 19. The nyquist stability diagrams for a driven CNT bundle interconnect; (a) versus length; (b) versus diameter. In this figure, the space between two adjacent CNTs has been chosen as 0.34 nm, and the length, the width and the thickness of CNT bundle, have been considered 10 μm, 50 nm and 125 nm, respectively. Also the load capacitance has been assumed equal to 5 fF [44].

As shown in Fig. 19 (a), by increasing the length of CNT bundle, the complex point (-1,0) goes toward outside the diagram. So, by increasing the length of CNT bundle, the system becomes more stable. As shown in Fig. 19 (b), by increasing the diameter of each individual CNT, the complex point (-1,0) goes toward outside the diagram and then, the diagram goes farther from this point. So, by increasing the diameter of each individual CNT, the system becomes more stable. It should be noted that in simulations of Fig. 19, the driver has been considered ideal with perfect contacts, and all individual CNTs in the bundle have been assumed metallic. A more detailed discussion about the stability analysis in CNT interconnects has been presented in [48].

6. Summary

In this chapter, we have studied interconnect challenges and the behaviour of carbon nanotube (CNT) as interconnect in VLSI circuits. In this review we discussed about the two main structures of CNT, including CNT bundles and MWCNTs, which achieve good performance due to the parallel SWCNTs in a bundle or the parallel shells in a MWCNT. These optimized configurations give the better characteristics including decreased delay time in comparison with SWCNTs, which is a vital parameter for the application as interconnect. The repeater (buffer) insertion technique that is used for the reduction of delay time in the global interconnects, has been discussed. Also in this chapter, we analyzed the time domain response of CNT bundle interconnect in a driver-interconnect-load configuration, based on the formulations and discussions we have presented in the reference [44]. At the continuation, we discussed briefly about the stability concept in CNT bundle interconnects, versus the length and diameter of each CNT in a CNT bundle.

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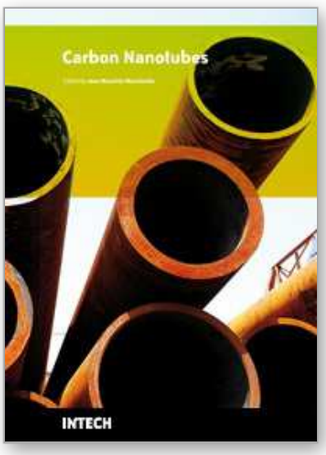

Carbon Nanotubes

Edited by Jose Mauricio Marulanda

ISBN 978-953-307-054-4
Hard cover, 766 pages
Publisher InTech
Published online 01, March, 2010
Published in print edition March, 2010

This book has been outlined as follows: A review on the literature and increasing research interests in the field of carbon nanotubes. Fabrication techniques followed by an analysis on the physical properties of carbon nanotubes. The device physics of implemented carbon nanotubes applications along with proposed models in an effort to describe their behavior in circuits and interconnects. And ultimately, the book pursues a significant amount of work in applications of carbon nanotubes in sensors, nanoparticles and nanostructures, and biotechnology. Readers of this book should have a strong background on physical electronics and semiconductor device physics. Philanthropists and readers with strong background in quantum transport physics and semiconductors materials could definitely benefit from the results presented in the chapters of this book. Especially, those with research interests in the areas of nanoparticles and nanotechnology.

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