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Dynamic Modelling and Control Design of Advanced Energy Storage for Power System Applications

Marcelo Gustavo Molina
CONICET, Instituto de Energía Eléctrica, Universidad Nacional de San Juan
Argentina

1. Introduction

In general, a large percentage of the electric power produced is generated in huge generation centres far from the consumption, and with centralized transmission and distribution systems, where the weak point of this scheme is the efficiency with high energy losses in the form of heat. This problem has been increased in the last years due to the significant growth of electric energy demand and in the case of structures of weakly meshed electrical grids, due to the high vulnerability in cases of faults that can originate frequently severe transient and dynamic problems that lead to the reduction of the system security (Dail et al., 2007). Many large blackouts that happened worldwide in the last decade are a clear example of the consequences of this model of electric power. These problems, far from finding effective solutions, are continuously increasing, even more impelled by energy factors (oil crisis), ecological (climatic change) and by financial and regulatory restrictions of wholesale markets, which causes the necessity of technological alternatives to assure, on one hand the appropriate supply and quality of the electric power and on the other one, the saving and the efficient use of the natural resources preserving the environment.

An alternative technological solution to this problem is using small generation units and integrating them into the distribution network as near as possible of the consumption site, making this way diminishing the dependence of the local electrical demand, of the energy transmission power system. This solution is known as in-situ, distributed or dispersed generation (DG) and represents a change in the paradigm of the traditional centralized electric power generation (El-Khattam & Salama, 2004). In this way, the distribution grid usually passive is transformed into active one, in the sense that decision making and control is distributed and the power flows bidirectionally. Here it is consolidated the idea of using clean non-conventional technologies of generation that use renewable energy sources (RESs) that do not cause environmental pollution, such as wind, photovoltaic (PV), hydraulic, biomass among others (Rahman, 2003).

At present, perhaps the most promising novel network structure that would allow obtaining a better use of the distributed generation resources is the electrical microgrid (MG) (Kroposki et al., 2008). This new paradigm tackles the distributed generation as a subsystem formed by distributed energy resources (DERs), including DG, RESs and distributed energy storage (DES) and controllable demand response (DR), also offering significant control

Source: Dynamic Modelling, Book edited by: Alisson V. Brito,
ISBN 978-953-7619-68-8, pp. 290, January 2010, INTECH, Croatia, downloaded from SCIYO.COM

capacities on its operation. This grid is designed to be managed as a group with a predictable unit of generation and demand, and can be operated as much interconnected to the main power system as isolated. In this way, the coordinated control of DERs and DR would allow maximizing the benefits for the owners of the microgrid, giving an attractive remuneration, as well as for the users, providing the thermal and electric demands with lesser energy costs and meeting the local requirements of security and dependability (Katiraei et al., 2008).

In recent years, due mainly to the technology innovation, cost reduction, and government policy stimulus there has been an extensive growth and rapid development in the exploitation of renewable energies, particularly wind and photovoltaic solar ones. However, the power provided by these RESs frequently changes and is hardly predictable, especially for the case of wind generation. Today, there exists an increasing penetration of large-scale wind farms (WF) and PV solar power plants into the electric power system all over the world (Battaglini et al., 2009). This situation can lead to severe problems that affect the micro grid security dramatically, particularly in a weak grid, i.e. system frequency oscillations due to insufficient system damping, and/or violations of transmission capability margin due to severe fluctuations of tie-line power flow, among others (Slootweg & Kling, 2003; Pourbeik et al., 2006). Even more, as presently deregulated power markets are taking place, generation and transmission resources are being utilized at higher efficiency rates, leading to a tighter control of the spare generation capacity of the system (Pourbeik et al., 2006a).

In order to overcome these problems, energy storage systems (ESS) advanced solutions can be utilized as an effective DES device with the ability of quickly exchanging the exceeding energy stored during off-peak load periods and thus providing a bridge in meeting the power and energy requirements of the microgrid. By combining the technology of energy storage with a recent type of power electronic equipments, such as flexible alternating current transmission systems (FACTS) (Song & Johns, 1999; Hingorani & Gyugyi, 2000), the power system can take advantage of the flexibility benefits provided by the advanced ESSs and the high controllability provided by power electronics. This allows enhancing the electrical grid performance, providing the enough flexibility to adapt to the specific conditions of the microgrid including intermittent RESs and operating in an autonomous fashion. There are many advanced technologies available in the market for energy storage with high potential of being applied in electrical microgrids. Such modern devices include super (or ultra) capacitors (SCES or UCES, respectively), superconducting magnetic energy storage (SMES), flywheels (FES) and advanced batteries (ABESS) among others. These ESSs can play a crucial, multi-functional role since storage facilities are designed to excel in a dynamic environment. Some factors driving the incorporation of these novel storage technologies include reduced environmental impact, rapid response, high power, high efficiency, and four-quadrant control, solving many of the challenges regarding the increased use of renewable energy sources, and enhancing the overall reliability, power quality, and security of power systems.

2. Overview of distributed energy storage technologies

A number of energy storage technologies have been developed or are under development for power system applications. These systems use different energy storage technologies, including conventional energy storage that have been extensively proven over many years, and recently developed technologies with high potential for applications in modern power systems, especially in electrical microgrids.

Four energy storage methodologies gather these technologies, i.e. chemical, electric, mechanic, and thermal energy storage (Molina & Mercado, 2001, 2003). Chemical storage methods use a reversible chemical reaction that takes place in the presence of an electrolyte for storing/producing DC electricity. This approach includes both, battery systems and fuel cells. Batteries contain the classic and well-known lead-acid type as well as the modern redox (reduction-oxidation) flow batteries and the advanced battery energy storage systems (ABESSs). ABESSs comprise new alkaline batteries, nickel chemistry (nickel-metal hydride–NiMH, and nickel-cadmium–NiCd), lithium chemistry (lithium–Li, and lithium-ion–Li-Ion), and sodium chemistry (sodium-sulfur–NaS, and sodium-salt–NaNiCl). Fuel cells (FC–hydrogen cycle and reversible/regenerative FCs) include five major types, that is alkaline fuel cells (AFC), proton exchange membrane fuel cells (PEMFC), phosphoric acid fuel cells (PAFC), molten carbonate fuel cells (MCFC), direct methanol fuel cells (DMFC), and solid oxide fuel cells (SOFC). Electric storage methods store energy directly as DC electricity in an electric or magnetic field, with no other intermediate energy transformation. This approach includes recent developments in superconducting magnetic energy storage (SMES) and the so-called super (or ultra) capacitor energy storage (SCES or UCES, respectively). Modern mechanical storage methods exchange their energy with the power system directly as AC electricity using a synchronous or asynchronous motor/generator. This methodology comprises updating of popular and well-proven pumped hydro, modern flywheels, and compressed air energy storage (CAES) systems. Thermal storage systems store energy as super-heated oil or molten salts. The heat of the salt or oil is used for steam generation and then to run a turbine coupled to an electric motor/generator.

Most of these technologies have been classified in terms of power and energy applications, grouped in short-term and long-term energy storage capabilities, as shown in Fig. 1 (Energy Storage Association, 2003). In general terms, power applications refer to energy storage systems rated for one hour or less, whereas energy applications would be for longer periods.

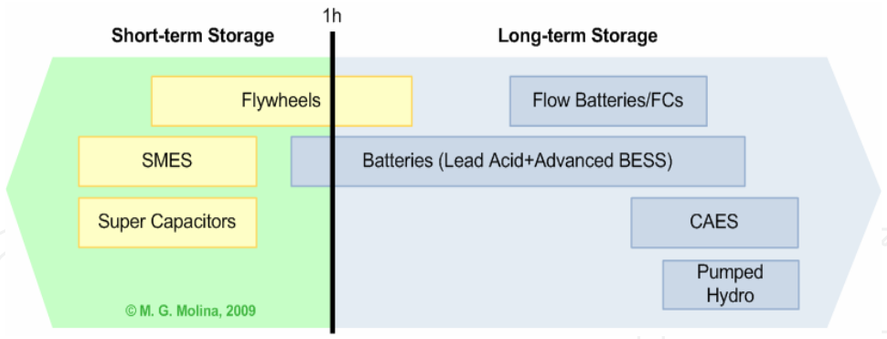


Fig. 1. Classification of energy storage technologies based on the storage capability

Energy storage in interconnected power systems has been studied for many years and the benefits are well-known and in general understood (Nourai, 2002; Energy Storage Association, 2003). In contrast, much less has been done particularly on distributed energy storage, but most of the same benefits apply. In both cases, storage costs, limited sitting opportunities, and technology limitations have restricted the use of energy storage during last decades. This chapter will address DES technologies for power applications in microgrids, i.e. considering only short-term energy storage capability requirements, since they are essential for allowing the microgrid operation in autonomous fashion and even more with high penetrations of intermittent renewable energy sources. They play the major

role in control and operation of a microgrid by providing an instantaneous bridge in meeting the power and energy requirements of the microgrid when DG sources primary reserve is not sufficient to meet the demand, particularly in response time. The analysis presented is focused on the three foremost advanced short-term energy storage systems, such as super capacitors, SMESs and flywheels.

2.1 Superconducting Magnetic Energy Storage – SMES

SMES is a type of energy storage system where energy is permanently stored in a magnetic field generated by the flow of DC current in a superconducting coil (SC). This coil is cryogenically cooled to a temperature below its critical temperature to exhibit its superconductivity property. The basic principle of a SMES is that once the superconducting coil is charged, the current will not decay and the magnetic energy can be stored indefinitely. This stored energy can be released back into the electric network by simply discharging the coil (Buckles & Hassenzahl, 2000). An attractive and a potentially cost-effective option for modern SMES systems is to use a high-temperature superconductor (HTS: Ceramic oxide compound) SMES cooled by liquid nitrogen instead of the usual low-temperature superconductor (LTS: Niobium-titanium alloy) SMES cooled by liquid helium to provide a short-term buffer during a disturbance in the power system.

The basic structure of a SMES device is shown in Fig. 2. The base of the SMES unit is a large superconducting coil, whose basic structure is composed of the cold components itself (the SC with its support and connection components, and the cryostat) and the cryogenic refrigerating system (Arsoy et al., 2003). On the other hand, the power conditioning system provides a power electronic interface between the AC power system and the SC, aiming at achieving two goals: one is to convert electric power from DC to AC, and the other is to charge/discharge efficiently the superconducting coil.

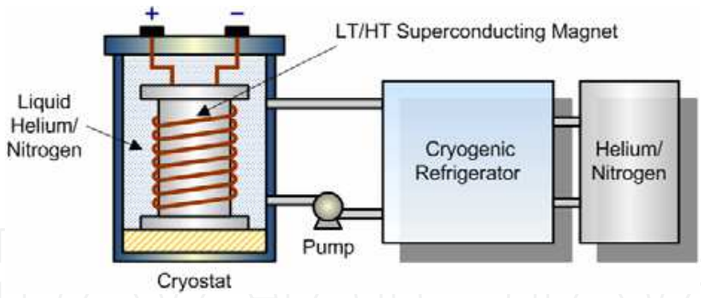


Fig. 2. Basic structure of a SMES device

SMES systems have many advantages over typical storage systems. The dynamic performance of a SMES system is far superior to other technologies. The superconducting feature of the SMES coil implies the "permanent" storage of energy because it has no internal resistance, which makes the stored energy not to be dissipated as heat. Moreover, this allows the coil to release all its stored energy almost instantaneously, a reason why they are very quick and have very short response times, limited by the switching time of the solid state components responsible of the energy conversion. On the other hand, the operation of the system and the lifetime are not influenced by the number of service cycles or the depth of discharge as in the case of traditional batteries. Additionally, a SMES system is highly efficient with more than 95% efficiency from input back to output, as well as highly reliable because of no using moving parts to carry out the energy storing.

Among the disadvantages of the SMES device is the high cost of superconducting wires and the large energy requirements for the refrigeration of the SMES system at cryogenic temperatures, particularly in conventional units (LTS); although this demand is considerably reduced by using modern HTS materials. In addition to these drawbacks is the use of huge magnetic fields, which can overcome 9 T.

2.2 Super Capacitor Energy Storage – SCES

Capacitors store electric energy through the electric field formed between two conducting plates (electrodes), when a DC voltage is applied across them. The so-called super capacitor energy storage (SCES), aka ultra capacitor energy storage (UCES), are a relative recent technology in the field of short-term energy storage systems and consist of a porous structure of activated carbon for one or both electrodes, which are immersed into an electrolytic solution (typically potassium hydroxide or sulphuric acid) and a separator that prevents physical contact of the electrodes but allows ion transfer between them (Barker, 2002). This structure effectively creates two equivalent capacitors (between each electrode and the electrolyte) connected in series, as shown in the schematic view of its internal components of Fig. 3. Energy is stored as a charge separation in the double layer formed at the interface between the solid electrode material surface and the liquid electrolyte in the micropores of the electrodes. Due to this feature, these capacitors are also known as electric double layer capacitors (EDLC) or simply advanced electrochemical capacitors.

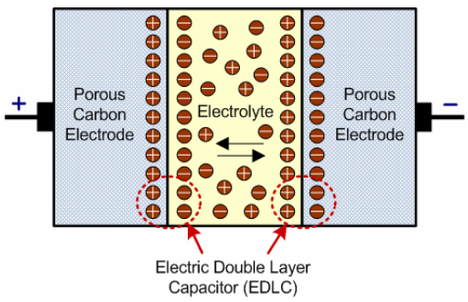


Fig. 3. Schematic view of a super capacitor

A super capacitor largely is subject to the same physics as a standard capacitor. That is, the capacitance is determined by the effective area of the electrodes, the separation distance of them and the dielectric constant of the separating medium. However, the key difference of the super capacitor is that with its structure of liquid electrolyte and porous electrodes (activated carbon material), an extremely high specific surface area is obtained (hundreds of m^2/g) compared to the conventional electrode structure (Conway, 1999). Furthermore, it ensures an extremely short distance at the interface between electrode and electrolyte (less than 1 μm). These two factors lead to a very high capacitance per unit of volume, which can be from hundreds to thousands times larger than electrolytic capacitors, up to a few thousand Farads (typically 5000 F) (Schindall, 2007). Unfortunately, the maximum voltage is limited to a few volts (normally up to 3 V) by the decomposition voltage of the electrolyte, mainly because of the presence of impurities.

Super capacitors have big advantages which make them almost non comparable in many applications. Because they have no moving parts, and require neither cooling nor heating, and because they undergo no internal chemical changes as part of their function, they are

robust and very efficient, reaching a cycle efficiency of 95% or more. Also, they require practically no maintenance and the lifetime is exceptionally high, with no lifetime degradation due to frequent and deep cycling. Presently, the life cycle of a typical super capacitor reaches over hundred thousands of duty cycles or more than 10 year life. Since super capacitors are capable of very fast charges and discharges, they make a perfect fit for voltage regulation in the power world.
Unfortunately, the most important disadvantage of super capacitors is that they are in the earliest stages of development as an ESS for power system applications and consequently costs are still extremely high. Presently, very small super capacitors in the range of seven to ten watts are widely available commercially for consumer power quality applications and are commonly found in household electrical devices. Development of larger-scale capacitors has been focused on electric vehicles. Presently, small-scale power quality (up to 250 kW) is considered to be the most promising utility use for advanced capacitors.

2.3 Flywheel Energy Storage – FES

A flywheel device stores electric energy as kinetic (or inertial) energy of the rotor mass spinning at very high speeds. Fig. 4 shows the structure of a conventional flywheel unit. The charging/discharging of the device is carried out through an integrated electrical machine operating either as a motor to accelerate the rotor up to the required high speeds by absorbing power from the electric grid (charge mode) or as a generator to produce electrical power on demand using the energy stored in the flywheel mass by decelerating the rotor (discharge mode). The system has very low rotational losses due to the use of magnetic bearings which prevent the contact between the stationary and rotating parts, thus decreasing the friction. In addition, because the system operates in vacuum, the aerodynamic resistance of the rotor is outstandingly reduced. These features permit the system to reach efficiencies higher than 80% (Nourai et al., 2005).
Flywheels have the ability to charge and discharge rapidly, and are almost immune to temperature fluctuations. They take up relatively little space, have lower maintenance requirements than batteries, and have a long life span. Flywheel devices are relatively tolerant of abuse, i.e. the lifetime of a flywheel system will not be shortened by a deep discharge unlike a battery. The stored energy is directly proportional to the flywheel rotor momentum and the square of the angular momentum, a reason why increments in the rotation speed yield large benefits on the storage energy density. Keeping this in mind, the classification in two types of flywheels arises: high speed flywheels (HS: approximately 40 000 rpm) and low speed flywheels (LS: approximately 7 000 rpm). High-speed flywheels allow obtaining very compact units with high energy densities (Liu & Jiang, 2007).
Conventional magnetic bearings have low specific power consumption (W/g), which is dissipated as heat in the copper of the bearing electromagnets. This power depends on the structure of the bearing and the utilized control system. Modern superconducting magnetic bearings, on the other hand, have demonstrated very low losses (10^{-2}–10^{-3}W/kg) in rotors at low speeds. This leads to a very high overall efficiency of the system, exceeding 90%.
Although most of the flywheel technology was developed in the automobile and aerospace industry, it is expected that flywheels have most commercial success targeted for power delivery capabilities of up to 1 MW. They are particularly suitable for the PQ and reliability market, but no large-scale applications of the technology have been installed to date. A big disadvantage of modern high-temperature superconducting flywheel devices is that they constitute a new technology, which is currently under development. Such systems would

offer inherent stability, minimal power loss, and simplicity of operation as well as increased energy storage capacity, which may show a promising future for use in the power sector.

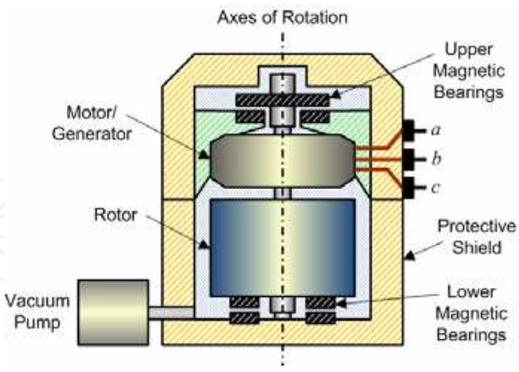


Fig. 4. Structure of a conventional flywheel

3. Application of advanced distributed energy storage in microgrids

For microgrids to work properly, an upstream interconnection switch must open typically during an unacceptable power quality (PQ) condition, and the DER must be able to provide electrical power to the islanded loads. This includes maintaining appropriate voltage and frequency levels for the islanded subsystem. In this way, the DER must be able to supply the active and reactive power requirements during islanded operation, so that fast-acting generation reserve is required. As a result, for stable operation to balance any instantaneous mismatch in active power, efficient distributed energy storage, such as super capacitors, SMESs and flywheels, must be used (Katiraei et al., 2008).

In a distributed energy storage system, the power conditioning system (PCS) is the interface that allows the effective connection to the electric power system. The PCS provides a power electronic interface between the AC electric system and the DES, aiming at achieving two major goals: one is to convert electric power from DC (or in some cases uncontrolled AC) to AC (established by the utility grid), and the other is to charge/discharge efficiently the DES device. The dynamics of the PCS directly influences the validity of the DES unit in the dynamic control of the microgrid. With the appropriate topology of the PCS and its control system design, the DES unit is capable of simultaneously performing both instantaneous active and reactive power flow control, as required in modern microgrid applications.

The progress in new technologies of power electronics devices (Bose, 2002; Carrasco et al., 2006), named flexible AC transmission systems (FACTS), is presently leading the use of advanced energy storage solutions in order to enhance the electrical grid performance, providing the enough flexibility to adapt to the specific conditions of the microgrid and operating in an autonomous fashion. Just as flexible FACTS controllers permit to improve the reliability and quality of transmission systems, these devices can be used in the distribution level with comparable benefits for bringing solutions to a wide range of problems. In this sense, FACTS-based power electronic controllers for distribution systems, namely custom power (CP) devices (or simply distribution FACTS), are able to enhance the reliability and the quality of power delivered to customers (Molina & Mercado, 2006). A distribution static synchronous compensator (DSTATCOM) is a fast response, solid-state power controller that belongs to advanced shunt-connected CP devices and provides flexible voltage control at the point of common coupling (PCC) to the utility distribution

feeder for power quality and stability improvements. It can exchange both active and reactive powers with the distribution system by varying the amplitude and phase angle of the PCS voltage with respect to the PCC voltage, if an energy storage system is included into the inner DC bus. The effect is a controlled current flow through the tie reactance between the DSTATCOM and the distribution network, this enabling the DSTATCOM to mitigate voltage fluctuations such as sags, swells and transients. Furthermore, it can be utilized for providing voltage regulation, power factor correction, harmonics compensation and stability augmentation. The addition of energy storage to the power custom device, through an appropriate interface, leads to a more flexible integrated controller. The ability of the DSTATCOM-DES (also known simply as DES system) to supply effectively active power allows expanding its compensation actions, reducing transmission losses and enhancing the operation of the electric microgrid (Molina et al., 2007).
Fig. 5 depicts a functional model of various advanced energy storage devices integrated with the appropriate power conditioning system for microgrid applications. This model consists mainly of a DSTATCOM, the energy storage system and the interface between the DSTATCOM and the DES, represented by the bidirectional converter.

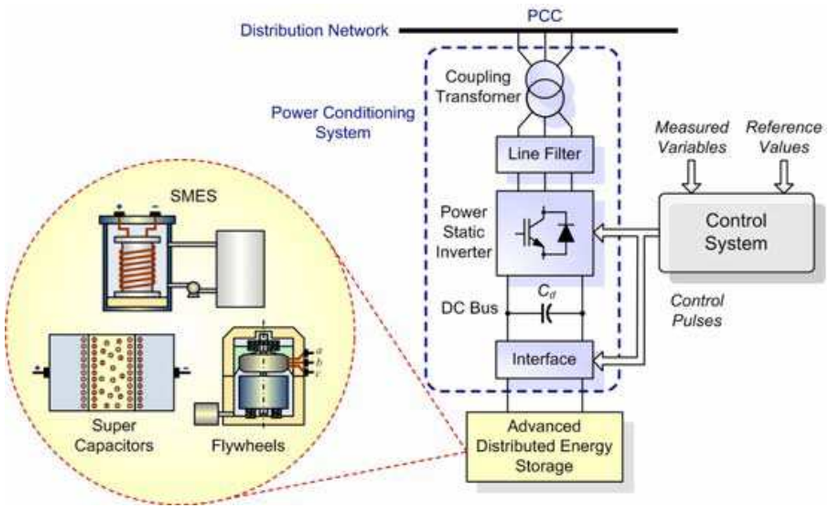


Fig. 5. Basic circuit of a custom power device integrated with advanced energy storage

The DSTATCOM consists mainly of a three-phase power inverter shunt-connected to the distribution network by means of a coupling transformer with line filter and the corresponding control scheme. The integration of the DES into the DC bus of the DSTATCOM device requires a rapid and robust bidirectional interface to adapt the wide range of variation in voltage and current levels between both devices, according to the specific DES employed. Controlling the DES rate of charge/discharge requires varying the voltage magnitude (and polarity in some cases) according to the state-of-operation, while keeping essentially constant the DC bus voltage of the DSTATCOM inverter. To this aim, a two-quadrant converter topology according to the DES unit employed is proposed in order to obtain a suitable control performance of the overall system.

4. Dynamic modelling and control design of the SMES system

A SMES system consists of several sub-systems, which must be carefully designed in order to obtain a high performance compensation device for microgrid applications. The base of

the SMES unit is a large superconducting coil (SC). On the other hand, the power conditioning system provides a power electronic interface between the AC electric system and the SC, allowing the grid-connected operation of the DES. Fig. 6 shows the proposed detailed model of the entire SMES system for applications in the distribution level. This model consists of the SMES coil with its filtering and protection system and the PCS for coupling to the electric grid.

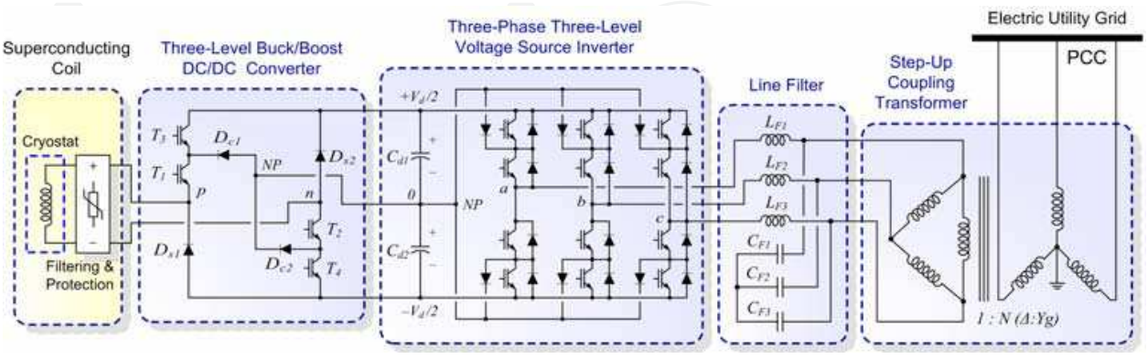


Fig. 6. Full detailed model of the proposed SMES system

4.1 Power conditioning system of the SMES

4.1.1 Three-phase three-level DSTATCOM

The key part of the PCS is the DSTATCOM device, and is shared by the three advanced selected DES systems, as will be described later. The proposed DSTATCOM essentially consists of a three-phase voltage source inverter (VSI) built with semiconductors devices having turn-off capabilities. This device is shunt-connected to the distribution network by means of a coupling transformer and the corresponding line sinusoidal filter. Its topology allows the device to generate at the point of common coupling to the AC network (PCC) a set of three almost sinusoidal voltage waveforms at the fundamental frequency phase-shifted 120º between each other, with controllable amplitude and phase angle. Since the SMES coil is basically a stiff current source, the use of a current source inverter (CSI) would emerge as the natural selection. However, the wide range of variation of the coil current and voltage would cause the device to exceed its rating, which makes impractical the use of conventional CSIs. On this basis, an analyses were performed to evaluate hybrid current source inverters (HCSI) and voltage source inverters (VSI); concluding that the later ones are a more cost-effective solution for the present application (Molina et al., 2007).

The three-phase VSI corresponds to a DC/AC switching power inverter using high-power insulated gate bipolar transistors (IGBTs). This semiconductor device is employed due to its lower switching losses and reduced size when compared to other devices. In addition, as the power rating of the inverter goes up to medium levels for typical DER applications (less than few MWs), the output voltage control of the VSI can be efficiently achieved through sinusoidal pulse width modulation (SPWM) techniques. The connection to the utility grid is made by means of a step-up Δ–Y coupling transformer, and second-order low pass sine wave filters are included in order to reduce the perturbation on the distribution system from high-frequency switching harmonics generated by the PWM control of the VSI. Since two ways for linking the filter can be employed, i.e. placing it before and after the coupling transformer, here it is preferred the first option because reduce notably the harmonics contents into the transformer windings, thus reducing losses and avoiding its overrating.

The VSI structure proposed is designed to make use of a three-level twelve pulse pole structure, also called neutral point clamped (NPC), instead of a standard two-level six pulse inverter structure (Rodriguez et al., 2002, Soto & Green, 2002). This three-level VSI topology generates a more smoothly sinusoidal output voltage waveform than conventional two-level structures without increasing the switching frequency and effectively doubles the power rating of the VSI for a given semiconductor device. Moreover, the three level pole attempts to address some limitations of the standard two-level by offering an additional flexibility of a level in the output voltage, which can be controlled in duration, either to vary the fundamental output voltage or to assist in the output waveform construction. This extra feature is used here to assist in the output waveform structure. In this way, the harmonic performance of the inverter is improved, also obtaining better efficiency and reliability. The output line voltage waveforms of a three-level VSI connected to a 380 V utility system are shown in Fig. 7. It is to be noted that in steady-state the VSI generates at its output terminals a switched line voltage waveform with high harmonics content, reaching the voltage total harmonic distortion (VTHD) almost 45% when unloaded. At the output terminals of the low pass sine wave filters proposed, the VTHD is reduced to as low as 1%, decreasing this quantity to even a half at the coupling transformer secondary output terminals (PCC). In this way, the quality of the voltage waveforms introduced by the PWM control to the power utility is improved and the requirements of IEEE Standard 519-1992 relative to power quality (VTHD limit in 5 %) are entirely fulfilled (Bollen, 2000).

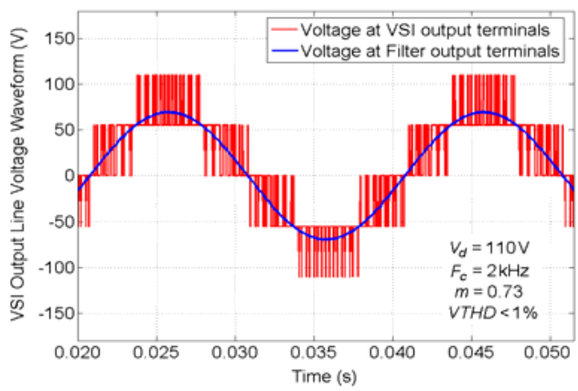


Fig. 7. Three-level NPC voltage source inverter output line voltage waveforms

The mathematical equations describing and representing the operation of the DSTATCOM can be derived from the detailed model shown in Fig. 6 by taking into account some assumptions respect to the operating conditions of the inverter. For this purpose, a simplified equivalent VSI connected to the electric system is considered, also referred to as an averaged model, which assumes the inverter operation under balanced conditions as ideal, i.e. the voltage source inverter is seen as an ideal sinusoidal voltage source operating at fundamental frequency, as depicted in Fig. 8. This consideration is valid since, as shown in Fig. 7, the high-frequency harmonics produced by the inverter as result of the sinusoidal PWM control techniques are mostly filtered by the low pass sine wave filters and the net instantaneous output voltages at the point of common coupling resembles three sinusoidal waveforms phase-shifted 120º between each other.

This ideal inverter is shunt-connected to the network at the PCC through an equivalent inductance L_s, accounting for the leakage of the step-up coupling transformer and an

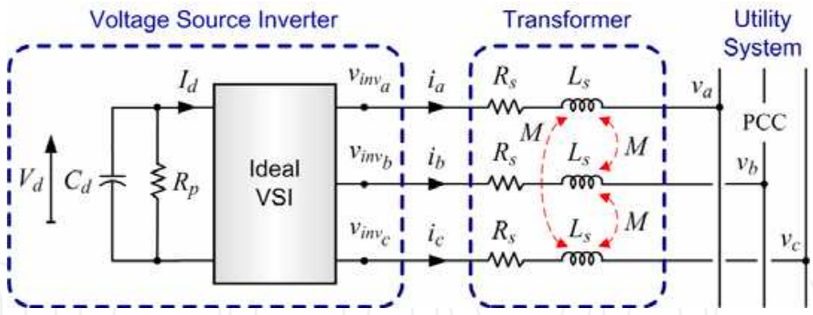


Fig. 8. Equivalent circuit diagram of the proposed inverter connected to the AC system

equivalent series resistance R_s, representing the transformers winding resistance and VSI semiconductors conduction losses. The magnetizing inductance of the step-up transformer can also be taken into consideration through a mutual equivalent inductance M. In the DC side, the equivalent capacitance of the two DC bus capacitors, C_{d1} and C_{d2} (C_{d1}=C_{d2}), is described through C_d=C_{d1}/2=C_{d2}/2 whereas the switching losses of the VSI and power losses in the DC capacitors are considered by a parallel resistance R_p. As a result, the dynamics equations governing the instantaneous values of the three-phase output voltages in the AC side of the VSI and the current exchanged with the utility grid can be directly derived from Fig. 8 by applying Kirchhoff's voltage law (KVL) as follows:

$$\begin{bmatrix} v_{inv_a} \\ v_{inv_b} \\ v_{inv_c} \end{bmatrix} - \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \left(\mathrm{R_s} + s\mathrm{L_s}\right) \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}, \tag{1}$$

where:

s: Laplace variable, being $s = d/dt$ for t > 0 (Heaviside operator p also used)

$$\mathrm{R_s} = \begin{bmatrix} R_s & 0 & 0 \\ 0 & R_s & 0 \\ 0 & 0 & R_s \end{bmatrix}, \ \mathrm{L_s} = \begin{bmatrix} L_s & M & M \\ M & L_s & M \\ M & M & L_s \end{bmatrix} \tag{2}$$

Under the assumption that the system has no zero sequence components (operation under balanced conditions), all currents and voltages can be uniquely transformed into the synchronous-rotating orthogonal two-axes reference frame, in which each vector is described by means of its d and q components, instead of its three a, b, c components. Thus, the new coordinate system is defined with the d-axis always coincident with the instantaneous voltage vector, as described in Fig. 9. By defining the d-axis to be always coincident with the instantaneous voltage vector v, yields v_d equals $|v|$, while v_q is null. Consequently, the d-axis current component contributes to the instantaneous active power and the q-axis current component represents the instantaneous reactive power. This operation permits to develop a simpler and more accurate dynamic model of the DSTATCOM.

By applying Park's transformation (Krause, 1992) stated by equation (3), equations (1) and (2) can be transformed into the synchronous rotating d-q reference frame as follows (equations (4) through (7)):

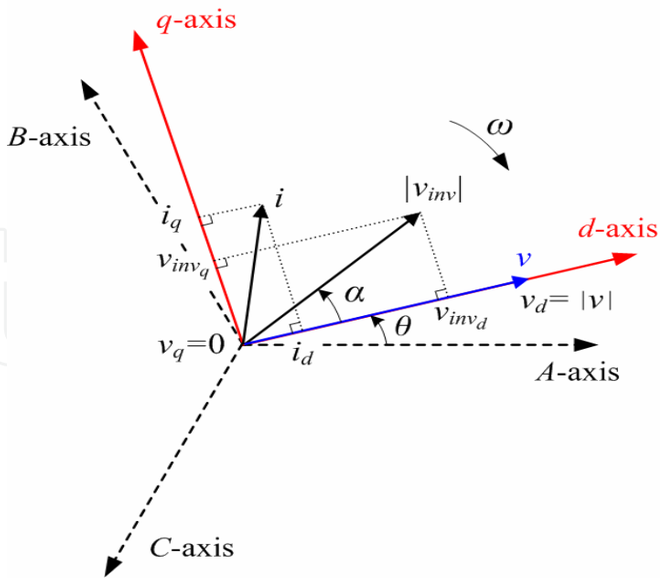


Fig. 9. DSTATCOM vectors in the synchronous rotating *d-q* reference frame

$$\mathrm{K_s}=\frac{2}{3}\begin{bmatrix}\cos\theta & \cos\left(\theta-\frac{2\pi}{3}\right) & \cos\left(\theta+\frac{2\pi}{3}\right)\\ -\sin\theta & -\sin\left(\theta-\frac{2\pi}{3}\right) & -\sin\left(\theta+\frac{2\pi}{3}\right)\\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2}\end{bmatrix}, \tag{3}$$

with:

$\theta=\int_0^t \omega(\xi)d\xi+\theta(0)$: angle between the *d*-axis and the reference phase axis,

and ξ: integration variable

ω: synchronous angular speed of the network voltage at the fundamental system frequency f (50 Hz throughout this chapter).

Thus,

$$\begin{bmatrix}v_{inv_d}-v_d\\ v_{inv_q}-v_q\\ v_{inv_0}-v_0\end{bmatrix}=\mathrm{K_s}\begin{bmatrix}v_{inv_a}-v_a\\ v_{inv_b}-v_b\\ v_{inv_c}-v_c\end{bmatrix},\quad \begin{bmatrix}i_d\\ i_q\\ i_0\end{bmatrix}=\mathrm{K_s}\begin{bmatrix}i_a\\ i_b\\ i_c\end{bmatrix} \tag{4}$$

Then, by neglecting the zero sequence components, equations (5) and (6) are derived.

$$\begin{bmatrix}v_{inv_d}\\ v_{inv_q}\end{bmatrix}-\begin{bmatrix}v_d\\ v_q\end{bmatrix}=\left(\mathrm{R_s}+s\mathrm{L'_s}\right)\begin{bmatrix}i_d\\ i_q\end{bmatrix}+\begin{bmatrix}-\omega & 0\\ 0 & \omega\end{bmatrix}\mathrm{L'_s}\begin{bmatrix}i_q\\ i_d\end{bmatrix}, \tag{5}$$

where:

$$\mathrm{R_s} = \begin{bmatrix} R_s & 0 \\ 0 & R_s \end{bmatrix},\ \mathrm{L'_s} = \begin{bmatrix} L'_s & 0 \\ 0 & L'_s \end{bmatrix} = \begin{bmatrix} L_s - M & 0 \\ 0 & L_s - M \end{bmatrix} \tag{6}$$

It is to be noted that the coupling of phases *abc* through the term *M* in matrix $\mathrm{L_s}$ (equation (2)), was fully eliminated in the *d-q* reference frame when the DSTATCOM transformers are magnetically symmetric, as is usually the case. This decoupling of phases in the synchronous-rotating system allows simplifying the control system design.
By rewriting equation (5), the following state equation can be obtained:

$$s\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \dfrac{-R_s}{L'_s} & \omega \\ -\omega & \dfrac{-R_s}{L'_s} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L'_s} \begin{bmatrix} v_{inv_d} - |v| \\ v_{inv_q} \end{bmatrix} \tag{7}$$

A further major issue of the *d-q* transformation is its frequency dependence (ω). In this way, with appropriate synchronization to the network (through angle θ), the control variables in steady state are transformed into DC quantities. This feature is quite useful to develop an efficient decoupled control system of the two current components. Although the model is fundamental frequency-dependent, the instantaneous variables in the *d-q* reference frame contain all the information concerning the three-phase variables, including steady-state unbalance, harmonic waveform distortions and transient components.
The relation between the DC-side voltage V_d and the generated AC voltage v_{inv} can be described through the average switching function matrix in the *dq* reference frame $\mathbf{S_{av,dq}}$ of the proposed inverter, as given by equation (8). This relation assumes that the DC capacitors voltages are balanced and equal to $V_d/2$.

$$\begin{bmatrix} v_{inv_d} \\ v_{inv_q} \end{bmatrix} = \mathbf{S_{av,dq}}\ V_d\,, \tag{8}$$

and the average switching function matrix in *dq* coordinates is computed as:

$$\mathbf{S_{av,dq}} = \begin{bmatrix} S_{av,d} \\ S_{av,q} \end{bmatrix} = \frac{1}{2} m_i\ a \begin{bmatrix} \cos\alpha \\ \sin\alpha \end{bmatrix}, \tag{9}$$

being,
m_i: modulation index of the voltage source inverter, $m_i \in [0, 1]$.
$a = \dfrac{\sqrt{3}}{\sqrt{2}} \dfrac{n_2}{n_1}$: turns ratio of the step-up Δ–Y coupling transformer,
α: phase-shift of the DSTATCOM output voltage from the reference position,
The AC power exchanged by the DSTATCOM is related with the DC bus power on an instantaneous basis in such a way that a power balance must exist between the input and the output of the inverter. In this way, the AC power should be equal to the sum of the DC resistance (R_p) power, representing losses (IGBTs switching and DC capacitors) and to the charging rate of the DC equivalent capacitor (C_d) (neglecting the SMES action):

$$P_{AC} = P_{DC} \tag{10}$$

$$\frac{3}{2}\left(v_{inv_d} i_d + v_{inv_q} i_q\right) = -\frac{C_d}{2} V_d s V_d - \frac{V_d^2}{R_p} \tag{11}$$

Essentially, equations (1) through (11) can be summarized in the state-space as described by equation (12). This continuous state-space averaged mathematical model describes the steady-state dynamics of the ideal DSTATCOM in the *dq* reference frame, and will be subsequently used as a basis for designing the middle level control scheme to be proposed.
As reported by Acha et al. (2002), modelling of static inverters by using a synchronous-rotating orthogonal *d-q* reference frame offer higher accuracy than employing stationary coordinates. Moreover, this operation allows designing a simpler control system than using *abc* or $\alpha\beta$.

$$s\begin{bmatrix} i_d \\ i_q \\ V_d \end{bmatrix} = \begin{bmatrix} \frac{-R_s}{L'_s} & \omega & \frac{S_{av,d}}{2L'_s} \\ -\omega & \frac{-R_s}{L'_s} & \frac{S_{av,q}}{2L'_s} \\ -\frac{3}{2C_d} S_{av,d} & -\frac{3}{2C_d} S_{av,q} & -\frac{2}{R_p C_d} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ V_d \end{bmatrix} - \begin{bmatrix} \frac{|v|}{L'_s} \\ 0 \\ 0 \end{bmatrix} \tag{12}$$

4.1.2 Two-quadrant three-level DC/DC converter

The inclusion of a SMES coil into the DC bus of the DSTATCOM VSI demands the use of a rapid and robust bidirectional interface to adapt the wide range of variation in voltage and current levels between both devices. Controlling the SMES coil rate of charge/discharge requires varying as much the coil voltage magnitude as the polarity according to the coil state-of-charge, while keeping essentially constant and balanced the voltage of the VSI DC link capacitors. To this aim, a two-quadrant three-level IGBT DC/DC converter or chopper is proposed to be employed, as shown in Fig. 6 (upper left side). This converter allows decreasing the ratings of the overall PCS (specifically VSI and transformers) by regulating the current flowing from the SMES coil to the inverter of the VSI and vice versa.
The three-level VSI topology previously described can be applied to reactive power generation almost without voltage imbalance problems. But when active power exchange is included, the inverter could not have balanced voltages without sacrificing output voltage performance and auxiliary converters would be needed in order to provide a compensating power flow between the capacitors of the DC link. For this reason, the use of a two-quadrant three-level DC/DC converter as interface between the DSTATCOM and the SMES is proposed instead of the commonly used standard two-level one (Molina & Mercado, 2007). This converter makes use of the extra level to solve the above-mentioned possible voltage imbalance problems, as will be described below. Major advantages of three-level DC/DC chopper topologies compared to traditional two-level ones include reduction of voltage stress of each IGBT by half, permitting to increase the chopper power ratings while maintaining high dynamic performance and decreasing the harmonics distortion produced. Furthermore, it includes the availability of redundant switching states, which allow generating the same output voltage vector through various states. This last feature is very significant to reduce switching losses and the VSI DC current ripple, but mainly to maintain the charge balance of the DC capacitors, thus avoiding generating additional distortion.

Table 1 lists all possible combinations of the chopper output voltage vectors, V_{pn} (defining the SMES side of the circuit as the output side) and their corresponding IGBT switching states. As derived, the chopper can be thought of as a switching matrix device that combines various states for applying either a positive, negative or null voltage to the SC coil. The addition of an extra level to the DC/DC chopper allows enlarging its degrees of freedom. As a result, the charge balance of the DC bus capacitors can be controlled by using the extra switching states, at the same time acting as an enhanced conventional DC/DC converter. The output voltage vectors can be selected based on the required SMES coil voltage and DC bus neutral point (*NP)* voltage. In this way, multiple subtopologies can be used in order to obtain output voltage vectors of magnitude *0* and $V_d/2$, in such a way that different vectors of magnitude $V_d/2$ produce opposite currents flowing from/to the neutral point. This condition causes a fluctuation in the *NP* potential which permits to maintain the charge balance of the dc link capacitors. By properly selecting the duration of the different output voltage vectors, an efficient DC/DC controller with *NP* voltage control capabilities is obtained.

States	T_1	T_2	T_3	T_4	V_{pn}
1	1	1	1	1	$+V_d$
2	0	0	0	0	$-V_d$
3	0	1	0	1	*0*
4	1	0	1	0	*0*
5	1	1	0	0	*0*
6	1	1	0	1	$+V_d/2$
7	1	1	1	0	$+V_d/2$
8	1	0	0	0	$-V_d/2$
9	0	1	0	0	$-V_d/2$

Table 1. Three-level chopper output voltage vectors and their resultant switching states

The DC/DC chopper has basically three modes of operation, namely the buck or charge mode, the stand-by or free-wheeling mode and the boost or discharge mode. These modes are obtained here by using a buck/boost topology control mode contrary to a bang-bang control mode (Aware & Sutanto, 2004), which is much simpler yet produces higher AC losses in the superconducting coil. The behaviour of the chopper for each mode of operation can be explained in terms of operating a combination of three of the switching states shown in Table 1 during a switching cycle T_s. The purpose of the chopper is to apply a positive, null, or negative average voltage to the SMES coil, according to the mode of operation.

In the first mode of operation, that is the charge mode, the chopper works as a step-down (buck) converter. Since power is supplied to the SC from the electric power system, this mode can also be called powering mode, and makes use of a combination of positive and null vectors. This is achieved through the switching states *1*, *5* and *6* or *7* in order to produce output voltage vectors $+V_d$, *0* and $+V_d/2$, respectively, with separate contribution of charge at the *NP* from capacitors C_{d1} and C_{d2}. In this mode, transistors T_1 and T_2 are always kept on, while transistors T_3 and T_4 are modulated to obtain the appropriate output voltage, V_{pn}, across the SMES coil. In this way, only subtopologies closest to the state *1* are used. In consequence, only one semiconductor device is switched per switching cycle; this reducing the switching losses compared to the standard two-level converter and thus also reducing the input/output current ripple.

Fig. 10(a) shows the switching function S_{ch} of the three-level chopper operating in buck mode. This function, which is stated in equation (13), is valid for the charge mode independently of the switching states utilized for maintaining the charge balance of the DC bus capacitors (states *6* or *7*).

$$S_{ch} = D_1 + D_2 + \sum_{h=1}^{\infty}\left[2\frac{\sin(h\,\pi D_2)}{h\pi}\cos\left[h\omega\left(t-\gamma_2-2\gamma_1\right)\right]\right] + \sum_{h=1}^{\infty}\left[\frac{\sin(2h\,\pi D_1)}{h\pi}\cos\left[h\omega\left(t-\gamma_1\right)\right]\right], \quad (13)$$

where, h=1, 2, 3 …

$D_1 = t_{on1}/2T_s$: duty cycle for switching states *6* or *7*

$D_2 = t_{on2}/T_s$: duty cycle for switching state 1

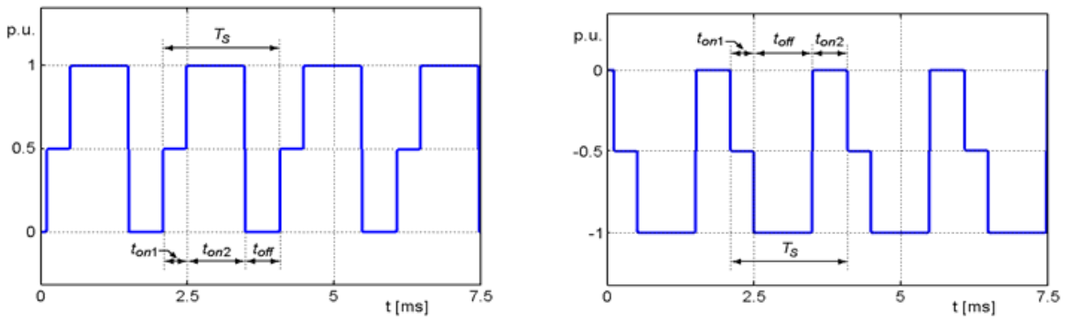
$\gamma_1 = D_1/f$: harmonic phase angle due to D_1

$\gamma_2 = D_2/2f$: harmonic phase angle due to D_2,

with f, being the fundamental electric grid frequency.

Once completed the charging of the SMES coil, the operating mode of the converter is changed to the stand-by mode, for which only the state *5* is used. In this second mode of operation transistors T_3 and T_4 are switched off, while transistors T_1 and T_2 are kept on all the time. In this way, the SMES coil current circulates in a closed loop, so that this mode is also known as free-wheeling mode. As in this mode no significant power losses are developed through semiconductors, the current remains fairly constant.

In the third mode of operation, that is the discharge mode, the chopper works as a step-up (boost) converter. Since power is returned back from the SC to the electric grid, this mode can also be called regenerative mode, and makes use of a combination of negative and null vectors. This is achieved through the switching states 2, *5* and *8* or *9* in order to produce output voltage vectors $-V_d$, *0* and $-V_d/2$ with independent contribution of charge at the *NP* from capacitors C_{d1} and C_{d2}. As can be observed from Fig. 10(b), in this mode transistors T_3 and T_4 are constantly kept off while transistors T_1 and T_2 are controlled to obtain the suitable voltage V_{pn}, across the SMES coil. In this way, only subtopologies closest to the state *2* are used. In consequence, as in the case of the charge mode, only one semiconductor device is switched per switching cycle.



(a) (b)

Fig. 10. Chopper switching functions. (a) Buck mode, S_{ch}. (b) Boost mode, S_{dch}

Fig. 10(b) shows the switching function S_{dch} of the three-level chopper operating in boost mode. This function, which is stated in equation (14), is valid for the discharge mode

independently of the switching states utilized for maintaining the charge balance of the DC capacitors (states *8* or *9*).

$$-S_{dch} = 1 - D_1 - D_2 + \sum_{h=1}^{\infty}\left[2\frac{\sin\left(h\,\pi\left(1-D_2\right)\right)}{h\pi}\cos\left[h\omega\left(t-\zeta_2-2\zeta_1\right)\right]\right] + \sum_{h=1}^{\infty}\left[\frac{\sin\left(2h\,\pi\left(1-D_1\right)\right)}{h\pi}\cos\left[h\omega\left(t-\zeta_1\right)\right]\right], \quad (14)$$

where, h=1, 2, 3 …

$\zeta_1 = (1-D_1)/f$: harmonic phase angle due to D_1

$\zeta_2 = (1-D_2)/2f$:harmonic phase angle due to D_2

By averaging the switching functions S_{ch} and S_{dch}, which results analogous to neglecting harmonics, a general expression relating the chopper average output voltage V_{ab} to the VSI average DC bus voltage V_d, can be derived through equation (15):

$$V_{ab} = m\,V_d\,, \quad (15)$$

being m, the modulation index expressed as:

$m = (D_1 + D_2)$: chopper in buck mode (charge)

$m = -(1 - D_1 - D_2)$: chopper in boost mode (discharge)

4.2 SMES coil

The equivalent circuit of the SMES coil makes use of a lumped parameter network implemented by a six-segment model based on Steurer & Hribernik (2005) and Chen et al. (2006), as described in Fig. 11. This representation allows characterizing the voltage distribution and frequency response of the SC coil with reasonable accuracy over a frequency range from DC to several thousand Hertz. The model comprises self inductances (L_i), mutual couplings between segments (i and j, M_{ij}), AC loss resistances (R_{Si}), skin effect-related resistances (R_{Shi}), turn-ground (shunt–C_{Shi}) and turn-turn capacitances (series–C_{Si}). A metal oxide semiconductor (MOV) protection for transient voltage surge suppression is included between the SMES model and the DC/DC converter.

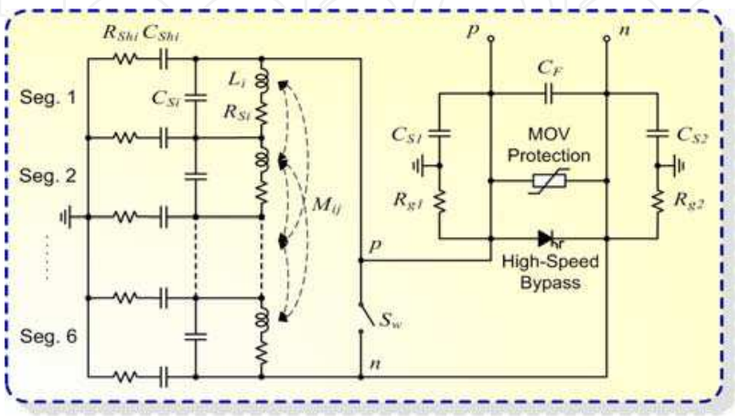
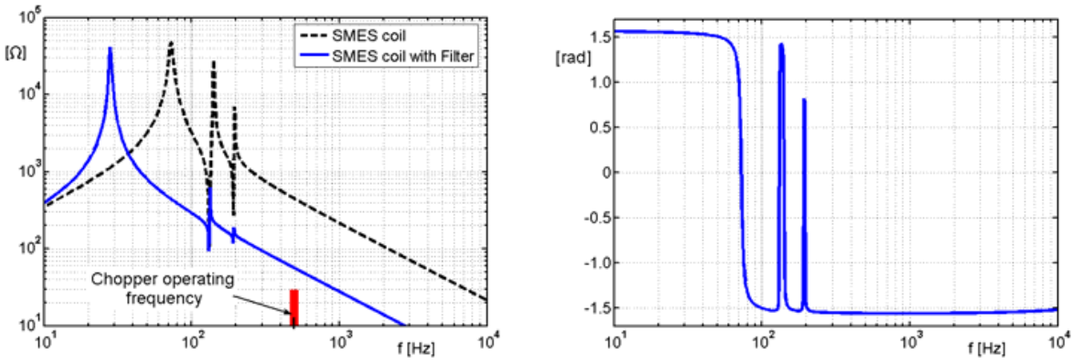


Fig. 11. Multi-segment model of the SMES coil

Fig. 12 shows the frequency domain analysis of the six-segment SMES model, measuring the impedance of the SC across its terminals (Z_{pn}) for the case of the coil including (solid-lines) and not including (dashed-lines) surge capacitors (C_{s1} and C_{s2}) in parallel with grounding-balance resistors (R_{g1} and R_{g2}) as well as a filter capacitor C_F for reducing the effect of resonance phenomena. As can be seen from the magnitude of the terminal impedance, the coil has parallel resonance (higher magnitudes of Z_{pn}) frequencies at around 70 Hz, 120 Hz, 200 Hz and series resonance (lower magnitudes of Z_{pn}) frequencies at about 110 Hz and 190 Hz. The chopper output voltage V_{pn} contains both even and odd harmonics of the switching frequency, which may excite coil resonances and cause significant voltage amplification of transients with the consequent addition of insulation stress within the SMES coil. Since the coil has a rather high inductance, these resonance frequencies become lower, turning this phenomena an issue for selecting the chopper operating frequency. In addition, high power DC/DC converters (several MWs) utilize low operating frequencies in order to minimize losses, being significant in consequence to take into consideration the coil resonance phenomena for choosing a safety frequency band of operation for the chopper. Fortunately, the negative effects of the harmonics decrease faster than the inverse of the harmonic order due to the skin effect occurring in the superconductor. In this way, for the case presented here, the chopper operating frequency can be set as low as 500 Hz without producing severe voltage amplification inside the SMES coil.



(a) (b)

Fig. 12. SMES coil terminal impedance Z_{pn} versus frequency: (a) Magnitude of SMES coil impedance (b) Phase angle of SMES coil impedance

The current and voltage of the superconducting inductor are related as:

$$i_{SC} = \frac{1}{L_{SC}} \int_{t_0}^{t} V_{SC}\, d\tau + I_{SC0} \tag{16}$$

where,

L_{SC}: equivalent full inductance of the SMES coil, accounting for all series self inductances L_i

I_{SC0}: initial current of the inductor

The amount of energy drawn from the SC coil is directly proportional to the equivalent inductance and to the change in the coil current (i_{SCi}–initial and i_{SCf}–final currents) as:

$$E_{SMES} = \frac{1}{2} L_{SC} \left({i_{SCi}}^2 - {i_{SCf}}^2 \right) \tag{17}$$

4.3 Proposed control scheme of the SMES system

The proposed hierarchical three-level control scheme of the SMES unit consists of an external, middle and internal level. Its design is based on concepts of instantaneous power on the synchronous-rotating *d-q* reference frame, as depicted in Fig. 13. This structure has the goal of rapidly and simultaneously controlling the active and reactive powers provided by the SMES (Molina & Mercado, 2009). To this aim, the controller must ensure the instantaneous energy balance among all the SMES components. In this way, the stored energy is regulated through the PCS in a controlled manner for achieving the charging and discharging of the SC coil.

4.3.1 External level control design

The external level control, which is outlined in Fig. 13 (left side) in a simplified form, is responsible for determining the active and reactive power exchange between the DSTATCOM-SMES device and the utility system. This control strategy is designed for performing two major control objectives: the voltage control mode (VCM) with only reactive power compensation capabilities and the active power control mode (APCM) for dynamic active power exchange between the SMES and the electric grid. To this aim, the instantaneous voltage at the PCC is computed by employing a synchronous-rotating reference frame. In consequence, by applying Park's transformation, the instantaneous values of the three-phase AC bus voltages are transformed into *d-q* components, v_d and v_q respectively, and then filtered to extract the fundamental components, v_{d1} and v_{q1}. As formerly described, the *d-axis* was defined always coincident with the instantaneous voltage vector v, then v_{d1} results in steady-state equal to $|v|$ while v_{q1} is null. Consequently, the *d*-axis current component of the VSI contributes to the instantaneous active power p while the *q*-axis current component represents the instantaneous reactive power q, as stated in equations (18) and (19). Thus, to achieve a decoupled active and reactive power control, it is required to provide a decoupled control strategy for i_{d1} and i_{q1}.

$$p = \frac{3}{2}(v_{d1}i_{d1} + v_{q1}i_{q1}) = \frac{3}{2}|v|\, i_{d1}\,, \tag{18}$$

$$q = \frac{3}{2}(v_{d1}i_{q1} - v_{q1}i_{d1}) = \frac{3}{2}|v|\, i_{q1}\,, \tag{19}$$

In this way, only v_d is used for computing the resultant current reference signals required for the desired SMES output active and reactive powers. Independent limiters are use for restrict both the power and current signals before setting the references i_{dr1} and i_{qr1}. Additionally, the instantaneous actual output currents of the SMES, i_{d1} and i_{q1}, are computed for use in the middle level control. In all cases, the signals are filtered by using second-order low-pass filters to obtain the fundamental components employed by the control system. A phase locked loop (PLL) is used for synchronizing, through the phase θ_s, the coordinate transformations from *abc* to *dq* components in the voltage and current measurement system. The phase signal is derived from the positive sequence components of the AC voltage vector measured at the PCC of the DSTATCOM-SMES.

The standard control loop of the external level is the VCM and consists in controlling (supporting and regulating) the voltage at the PCC through the modulation of the reactive component of the DSTATCOM output current, i_{q1}. This control mode has proved a very

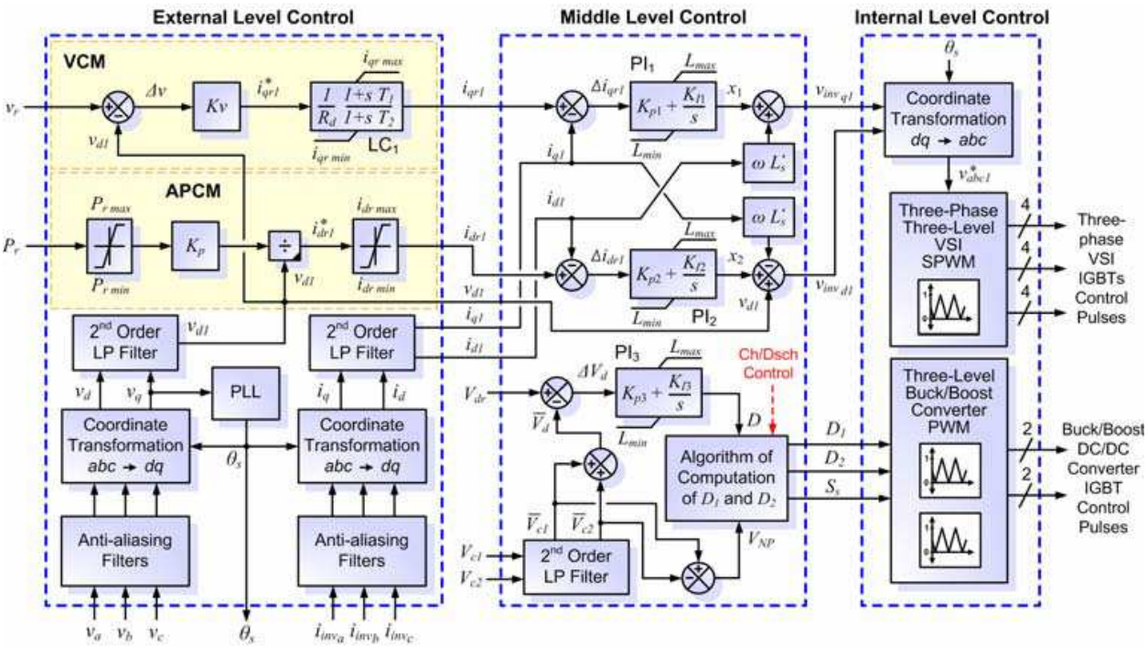


Fig. 13. Multi-level control scheme of the SMES system

good performance in conventional DSTATCOM controllers (with no energy storage). The design of this control loop in the rotating frame is simpler than using stationary frame techniques, and employs a standard proportional-integral (PI) compensator including an anti-windup system to enhance the dynamic performance of the VCM system. This control mode compares the reference voltage set by the operator with the actual measured value in order to eliminate the steady-state voltage offset via the PI compensator. A voltage regulation droop (typically 5%) R_d is included in order to allow the terminal voltage of the DSTATCOM-SMES to vary in proportion with the compensating reactive current. Thus, the PI controller with droop characteristics becomes a simple phase-lag compensator (LC_1), resulting in a stable fast response compensator. This feature is particularly significant in cases that more high-speed voltage compensators are operating in the area. This characteristic is comparable to the one included in generators´ voltage regulators.

The APCM allows controlling the active power exchanged with the electric system. The control strategy to be applied can be designed for performing various control objectives with dissimilar priorities, as widely presented in the literature (Molina & Mercado, 2006, 2007, 2009). In this chapter, a general active power command to achieve the desired system response is provided. To this aim, the in-phase output current component reference signal of the DSTATCOM, i_{dr1} is straightforwardly derived from the reference active power. In this way, the active power flow between the DSTATCOM-SMES and the power system can be controlled so as to force the SC to absorb active power when P_r is negative, i.e. operating in the charge mode, or to inject active power when P_r is positive, that is operating in the discharge mode.

4.3.2 Middle level control design

The middle level control makes the expected output, i.e. positive sequence components of i_d and i_q, to dynamically track the reference values set by the external level. The middle level

control design, which is depicted in Fig. 13 (middle side), is based on a linearization of the state-space averaged model of the SMES VSI in *d-q* coordinates, described in equation (12). Inspection of this equation shows a cross-coupling of both components of the SMES output current through ω. Therefore, in order to fully decouple the control of i_d and i_q, appropriate control signals have to be generated. To this aim, it is proposed the use of two control signals x_1 and x_2, which are derived from assumption of zero derivatives of currents ($s\, i_d$ and $s\, i_q$) in the upper part (AC side) of equation (12). This condition is assured by employing conventional PI controllers with proper feedback of the SMES actual output current components, as shown in Fig. 13. Thus, i_d and i_q respond in steady-state to x_1 and x_2 respectively with no crosscoupling, as derived from equation (20). As can be noticed, with the introduction of these new variables this control approach allows to obtain a quite effective decoupled control with the VSI model (AC side) reduced to first-order functions.

$$s\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \dfrac{-R_s}{L'_s} & 0 \\ 0 & \dfrac{-R_s}{L'_s} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} - \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \tag{20}$$

From equation (12), it can be seen the additional coupling resulting from the DC capacitors voltage V_d, as much in the DC side (lower part) as in the AC side (upper part). This difficulty demands to maintain the DC bus voltage as constant as possible, in order to decrease the influence of the dynamics of V_d. The solution to this problem is obtained by using another PI compensator which allows eliminating the steady-state voltage variations at the DC bus, by forcing the instantaneous balance of power between the DC and the AC sides of the DSTATCOM through the modulation of the duty cycle (D) of the DC/DC chopper. Finally, duty cycles D_1 and D_2 are computed through the novel controller in order to prevent dc bus capacitors voltage drift/imbalance, as formerly explained. This novel extra DC voltage control block provides the availability of managing the redundant switching states of the chopper according to the capacitors charge unbalance measured through the neutral point voltage, $V_{PN} = \overline{V_{c1}} - \overline{V_{c2}}$. This specific loop modifying the modulating waveforms of the internal level control is also proposed for reducing instability problems caused by harmonics as much in the SMES device as in the electric system. The application of a static determination of D_1 and D_2, such as the case of D_1=D_2=$D/2$, has proved to be good enough for reaching an efficient equalization of the DC bus capacitors over the full range of VSI output voltages and active/reactive power requirements.

4.3.3 Internal level control design

The internal level provides dynamic control of input signals for the DC/DC and DC/AC converters. This level is responsible for generating the switching control signals for the twelve valves of the three-level VSI, according to the control mode (SPWM) and types of valves (IGBTs) used and for the four IGBTs of the buck/boost three-level DC/DC converter. Fig. 13 (right side) shows a basic scheme of the internal level control of the SMES unit. This level is mainly composed of a line synchronization module and a firing pulses generator for both the VSI and the chopper. The coordinate transformation from Cartesian to Polar yields the required magnitude of the output voltage vector V_{inv} produced by the VSI, and its absolute phase-shift rating α. The line synchronization module simply synchronizes the

SMES device switching pulses with the positive sequence components of the AC voltage vector at the PCC through the PLL phase signal, θ_s.
In the case of the sinusoidal PWM pulses generator block, the controller of the VSI generates pulses for the carrier-based three-phase PWM inverter using three-level topology. Thus, the expected sinusoidal-based output voltage waveform V_{abc*} of the DSTACOM-SMES, which is set by the middle level control, is compared to triangular signals generated by the carriers generator for producing three-state PWM vectors (1, 0, -1). These states are decoded by the states-to-pulses decoder via a look-up-table that relates each state with the corresponding firing pulse for each IGBT of the four ones in each leg of the three-phase three-level VSI.
In the case of the DC/DC converter firing pulses generator block, the three-level PWM modulator is built using a compound signal obtained as the difference of two standard two-level PWM signals. According to the mode of operation of the chopper (charge/discharge), switching functions S_{ch} and S_{dch} are synthesized using equations (13) and (14).

5. Dynamic modelling and control design of the SCES system

Super capacitor energy storage (SCES) systems consist of several sub-systems, but share most of them with SMES systems since both operate at DC voltage levels. The base of the SCES system is the super capacitors bank. On the other hand, the power conditioning system provides an electronic interface between the AC electric system and the super capacitors, allowing the grid-connected operation of the DES. Fig. 14 shows the proposed detailed model of the entire SCES system for applications in the distribution level. This model consists of the super capacitors bank and the PCS for coupling to the electric grid (Molina & Mercado, 2008).

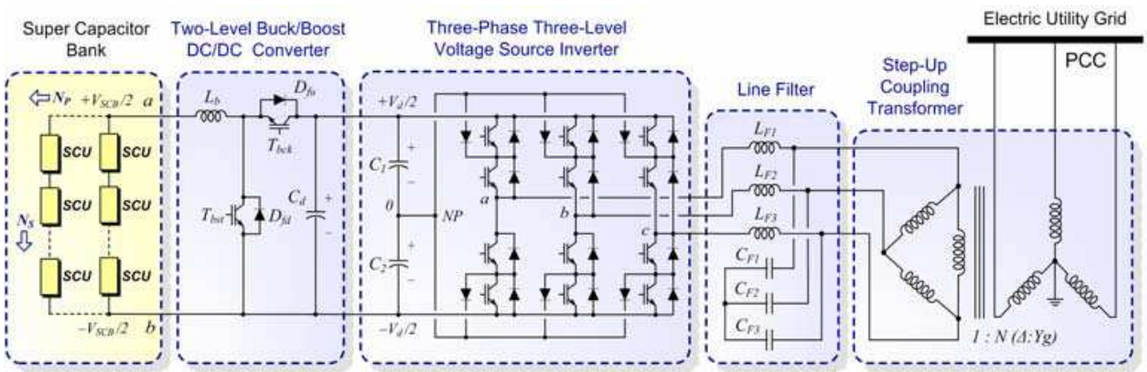


Fig. 14. Detailed model of the proposed SCES

5.1 Power conditioning system of the SCES

5.1.1 Three-phase three-level DSTATCOM

As in the prior case of the SMES system, the key part of the PCS is the DSTATCOM device, and utilizes the same topology that SMESs. The proposed DSTATCOM essentially consists of a three-phase three-level VSI built with semiconductors devices having turn-off capabilities, such as IGBTs, as shown in Fig. 14 (right side). This device is shunt-connected to the distribution network by means of a coupling transformer and the corresponding line sinusoidal filter. Equations governing the steady-state dynamics of the ideal DSTATCOM in the *dq* reference frame were previously derived and summarized in equation (12).

5.1.2 Two-quadrant two-level DC/DC converter

The integration of the SCES system into the DC bus of the DSTATCOM device requires a rapid and robust bidirectional interface to adapt the wide range of variation in voltage and current levels between both devices, especially because of the super capacitors dynamic behaviour, during both charge and discharge modes. Controlling the SCES system rate of charge/discharge requires varying the voltage magnitude according to the SCU state-of-operation, while keeping essentially constant the DC bus voltage of the DSTATCOM VSI (in contrast to SMES systems, in SCESs polarity does not change). To this aim, a combined two-quadrant two-level buck/boost DC/DC converter topology by using high-power fast-switched IGBTs is proposed in order to obtain a suitable control performance of the overall system. This step-down and step-up converter allows decreasing the ratings of the overall power devices by regulating the current flowing from the SCES to the inverter of the DSTATCOM and vice versa. Since there are no requirement for electrical isolation between input and output, no isolation circuit is considered in this work.

The basic structure of the DC/DC boost converter proposed is shown in Fig. 14. This switching-mode power device contains basically two couples of semiconductor switches (two power IGBT transistors connected in anti-parallel to respective free-wheeling diodes, T_{bck}–D_{fu} and T_{bst}–D_{fd}) and two energy storage devices (an inductor L_b and a capacitor C_d) for producing a single polarity DC voltage output with greater or lower level than its input DC voltage, according to the operation mode of the SCES. This bidirectional DC/DC converter has basically the three standard modes of operation, namely the charge mode, the discharge mode and the stand-by mode. In the charge mode, the chopper works as a step-down (buck) converter employing T_{bck}, D_{fd} and L_b. This topology makes use of modulation of transistor T_{bck} (upper IGBT in the leg), while keeping T_{bst} off at all times, in order to produce a power flow from the DC bus of the DSTATCOM to the UCES system. Once completed the charging of the UCES, the operating mode of the DC/DC converter is changed to the stand-by mode, for which both IGBTs are maintained continually switched off. In the discharge mode, the chopper operates as a step-up (boost) converter using T_{bst}, D_{fu}, L_b and C_d. This topology employs the modulation of the lower IGBT of the leg, i.e. T_{bst}, while preserves T_{bck} off all the time in order to produce a power flow from the UCES to the DSTATCOM DC bus. The operation of the DC/DC converter in the continuous (current) conduction mode (CCM), i.e. the current flows continuously in the inductor L_b during the entire switching cycle, facilitates the development of the state-space model because only two switch states are possible during a switching cycle for each operation mode, namely, (i) the power switch T_{bck} is on and the diode D_{fd} is off; or (ii) T_{bck} is off and D_{fd} is on, for the charge mode, and (i) the power switch T_{bst} is on and the diode D_{fu} is off; or (ii) T_{bst} is off and D_{fu} is on, for the discharge mode. In steady-state CCM operation, the state-space equation that describes the dynamics of the DC/DC converter is given by equation (21).

$$s\begin{bmatrix} I_{SCB} \\ V_d \end{bmatrix} = \begin{bmatrix} 0 & -\frac{S_{dc}}{L_b} \\ -\frac{S_{dc}}{C_d} & 0 \end{bmatrix} \begin{bmatrix} I_{SCB} \\ V_d \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix} \begin{bmatrix} V_{SCB} \\ I_d \end{bmatrix}, \tag{21}$$

where:

I_{SCB}: Chopper input current, matching the SCES output current.

V_{SCB}: Chopper input voltage, the same as the SCES output voltage.
V_d: Chopper output voltage, coinciding with the VSI DC bus voltage.
i_d: Chopper output current.
S_{dc}: Switching function of the buck/boost DC/DC converter.
The switching function S_{dc} is a two-levelled waveform characterizing the signal that drives the power switch of the DC/DC buck/boost converter, according to the operation mode.
If the switching frequency of the power switches is significantly higher than the natural frequencies of the DC/DC converter, this discontinuous model can be approximated by a continuous state-space averaged (SSA) model, where a new variable m_c is introduced. In the [0, 1] interval, m_c is a continuous function and represents the modulation index of the DC/DC converter. This variable is used for replacing the switching function in equation (21), yielding the following SSA expression:

$$s\begin{bmatrix} I_{UCB} \\ V_d \end{bmatrix} = \begin{bmatrix} 0 & -\frac{m_c}{L_b} \\ -\frac{m_c}{C_d} & 0 \end{bmatrix} \begin{bmatrix} I_{UCB} \\ V_d \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix} \begin{bmatrix} V_{UCB} \\ I_d \end{bmatrix}, \tag{22}$$

Since, in steady-state conditions the inductor current variation during both, on and off times of T_b are essentially equal, so there is not net change of the inductor current from cycle to cycle, and assuming a constant DC output voltage of the bidirectional converter, the steady-state input-to-output voltage conversion relationship of the buck/boost converter is easily derived from equation (22), by setting the inductor current derivative at zero, yielding equation (23).

$$V_{SCB} = m_c V_d \tag{23}$$

In the same way, the relationship between the average input current I_{SCB} and the DC/DC converter output current I_d in the CCM can be derived as follows:

$$I_d = m_c I_{SCB} \tag{24}$$

As can be observed, both the steady-state input-to-output current and voltage conversion relationships coincide with the modulation index m_c, which is defined as:
$m_c = D$: for the bidirectional chopper in buck mode (charge),
$m_c = (1 - D)$: for the bidirectional chopper in boost mode (discharge),
where $D \in [0, 1]$ is the duty cycle for switching T_{bck} or T_{bst} according to the operation mode, defined as the ratio of time during which the particular power switch is turned-on to the period of one complete switching cycle, T_s.

5.2 Super capacitors bank

The super capacitor unit (SCU) performance is based mainly on an electrostatic effect, which is purely physical reversible, rather than employing faradic reactions as is the case for batteries, although includes an additional pseudocapacitive layer contributing to the overall capacitance. Because of the complex physical phenomena in the double layer interface, traditional simple models such as the classical lumped-parameter electrical model (Spyker & Nelms, 2000) represented by a simple *RC* circuit composed only of a capacitance with an

equivalent series resistance (ESR), and an equivalent parallel resistance (EPR) are inadequate for modelling EDLCs. These models yield a large inaccuracy when compared with experimental results. Therefore, this work proposes the use of an enhanced electric model of a super capacitor, based on the ones previously proposed by Rafika et al. (2007) and Zubieta & Bonert (2000), which reflects with high precision the effects of frequency, voltage and temperature in the dynamic behaviour. This solution is easy to implement in any software environment (such as MATLAB, PSCAD, EMTP, etc) and allows an adequate simulation time when the SCES is used in applications containing many states and non-linear blocks such as the case of incorporating power electronic devices into electric power systems. The model proposed describes the terminal behaviour of the EDLC unit over the frequency range from DC to several thousand Hertz with sufficient accuracy.

The equivalent electric circuit model of the super capacitor unit is depicted in Fig. 15. In order to define the structure of this equivalent circuit, three major aspects of the physics of the double-layer capacitor should be taken into account. Firstly, based on the electrochemistry of the interface between two materials in different phases, the double layer capacitance is modelled by two ladder circuits consisting in resistive–capacitive branches with different time constants (R_E, R_I–C_A, R_V–C_V). Secondly, based on the theory of the interfacial tension in the double layer, the capacitance of the device turns out to be in a dependence on the potential difference, so that in order to reflect the voltage dependence of the capacitance, C_V is assumed to vary linearly with the voltage at its terminals (V_{SCB}) by the relation $C_V = 2K_V V_{UC}$, while C_A represents the constant capacitance and is empirically determined in the order of 2/3 of the nominal capacitance value provided by the manufacturer. Thirdly, the double-layer capacitor has a certain self-discharge as a consequence of the diffusion of the excess ionic charges at the interface between the electrode and the electrolyte, and due to the impurities in the SCU materials. This low current-leakage pathway between the SCU terminals determines the duration time of stored energy in open circuit, and is dependent of voltage and temperature. Hence, the super capacitor self-discharge cannot be represented by a simple single resistance. It is necessary to use two different time constant circuits, formed by R_{P1}–C_{P1} and R_{P2}–C_{P2}, which depend on the voltage V_{SCU} and on the SCU operating temperature T_{SC}. A parallel R_L resistance giving the long time leakage current contribution is also included. Circuit made up of R_I–C_I is introduced into the model to take into account the electrolyte ionic resistance temperature dependence in the low frequency range, with $R_I(T)$, while cancelling its effect in the high

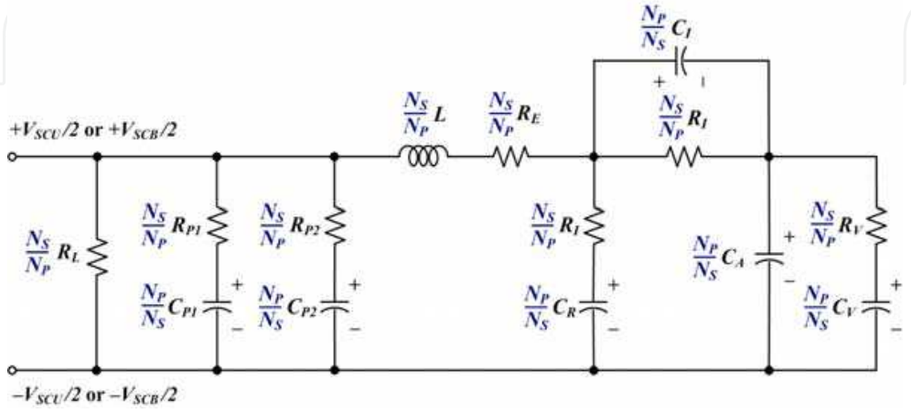


Fig. 15. Advanced equivalent electric circuit model of the super capacitor unit/bank

frequency range, through C_I. Circuit formed by R_I–C_R gives more precision to the model by increasing the value of the differential capacitance for the average frequencies. Eventually, a small equivalent series inductance (nano Henrys) is added to the model for pulsed applications.

Since the frequency characteristics of the complex impedance of electrochemical cells are useful for characterizing a UCES unit, electrochemical impedance spectroscopy (EIS) has been also performed on a BCAP0010 super capacitor (Maxwell Technologies, 2008) for extending the analysis from the time domain to the frequency domain. Thus, the EDLC is swept in frequency for various voltage levels and with different temperatures. Fig. 16 plots the real and imaginary components of super capacitor impedance as a function of frequency for a bias voltage of 2.5 V and a temperature of 20 ºC. As can be observed from the real part, the dependence of impedance on frequency can be divided into four distinct frequency zones. Zone I, in the range 1 mHz−10 mHz with characteristic time constant from 100 to 1000 s, is determined by series (R_I, R_E) and parallel resistances. However, at very low frequencies, leakage current represented by parallel resistance R_L dominates the contribution. Zone II, between 10 mHz and 10 Hz gives the information on the series resistances R_I and R_E. In this zone, the effect of parallel resistance is negligible and both, R_I and R_E contribute at 10 mHz to form the so-called DC series resistance ESR−DC given by manufacturers. Zone III, in the range 10 Hz−1 kHz shows mainly the resistance R_E due to all the connections, particularly the contact resistance between the activated carbon and the current collector as well as the minimal resistance of the electrolyte. In this range, manufacturers specify this series resistance as an AC series resistance, also called ESR−1 kHz. Zone IV, between 1 and 10 kHz is due to the super capacitor inductance and the parasitic inductance of the all connecting cables. As can be derived from the imaginary part of frequency characteristics of the SCES complex impedance, there exists a resonance frequency around 25 Hz below which the SCU behaviour is entirely capacitive. During more than ±1/2 decade of this resonance frequency, the imaginary component of the impedance magnitude is relatively flat and approximately zero, this demonstrating a purely resistive EDLC behaviour in this mid-frequency range. Above this frequency, the magnitude begins increasing indicating a completely inductive effect.

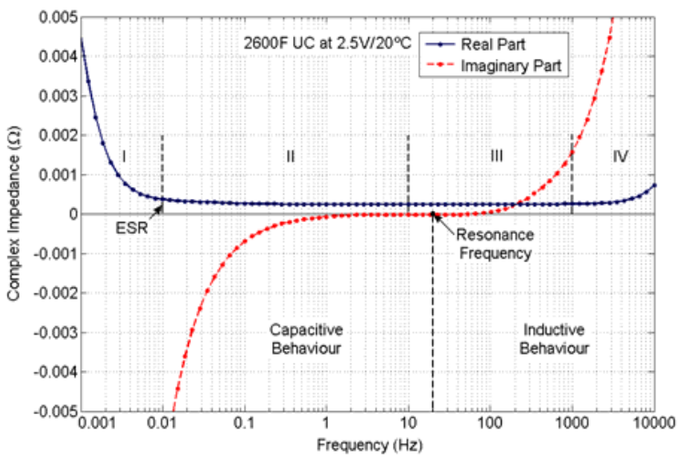


Fig. 16. Impedance real and imaginary part of 2600F super capacitor (BCAP0010) as a function of frequency with a bias voltage of 2.5V and a temperature of 20ºC

The amount of energy drawn from the super capacitor unit is directly proportional to the differential capacitance and to the change in the terminal voltage (V_{SCUi}–initial and V_{SCUf}–final voltages), as given by equation (28).

$$E_{SCU} = \frac{1}{2} C_{SCU} \left({V_{SCUi}}^2 - {V_{SCUf}}^2 \right) \tag{25}$$

For practical applications in power systems, the required amount of terminal voltage and energy of UCES exceed largely the quantities provided by an SCU. In this way, an SCES system can be built by using multiple SCUs connected in series to form a SCES string and in parallel to build a bank of SCUs (SCB), as depicted in Fig 14. For this topology, the terminal voltage determines the number of capacitors N_s which must be connected in series to form a string, and the total capacitance determines the number of super capacitors strings N_p which must be connected in parallel in the bank. The equivalent electric circuit model of the super capacitor unit can be extended to the SCB by directly computing the total resistances, capacitances and inductances according to the series and parallel contribution of each parameter, as depicted in Fig. 15 (blue text). This proposed advanced dynamic model of SCB shows a very good agreement with measured data at all the operating frequency range.

5.3 Proposed control scheme of the SCES system

The proposed hierarchical three-level control scheme of the SCES system consists of an external, middle and internal level, of which each level has its own control objectives. Its design, as in the case of the SMES device, is also based on the synchronous-rotating *d-q* reference frame, as depicted in Fig. 17 (Molina & Mercado, 2008).

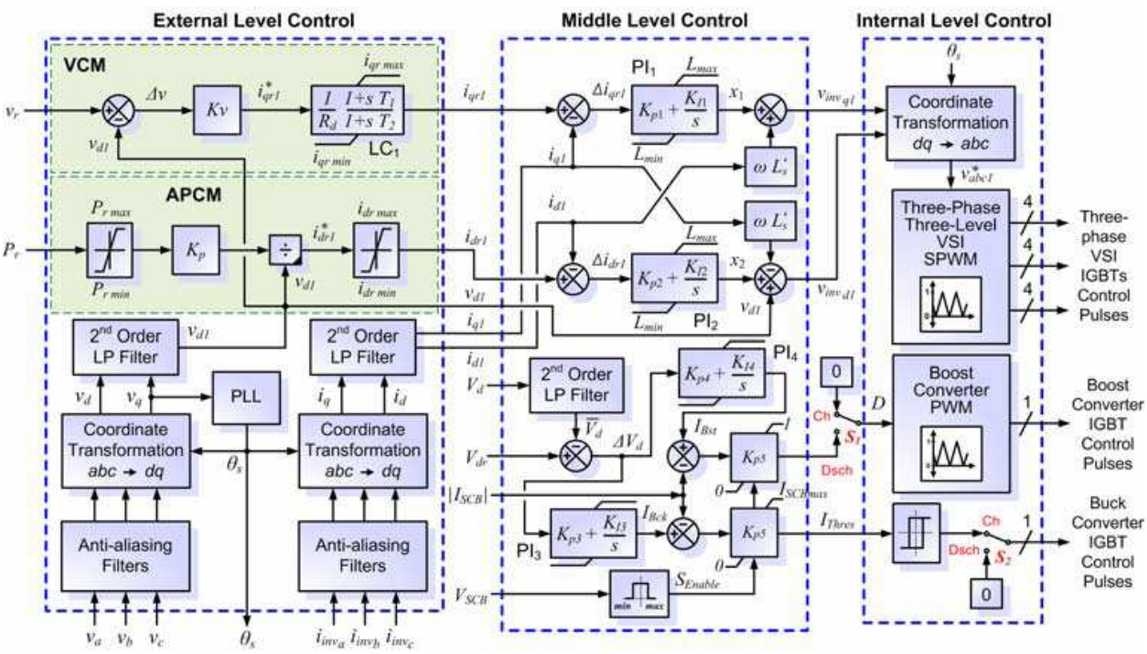


Fig. 17. Multi-level control scheme of the SCES system

5.3.1 External level control design

As in the former case of the SMES system, the external level control, which is outlined in Fig. 17 (left side), is responsible for determining the active and reactive power exchange between the DSTATCOM-SCES device and the electric grid. This control strategy is designed for performing the same major control objectives as SMES, i.e. VCM with only reactive power compensation capabilities produced locally by the DSTATCOM and independently of the storage device and the active power control mode (APCM) for dynamic active power exchange between the SCES and the electric grid.

5.3.2 Middle level control design

The middle level control shares part of the algorithms corresponding to the SMES one, since both devices utilize the same DSTATCOM topology and then the control of this last device is identical. The difference with the SMES system is in the control of the DC/DC converter, which is now specific for the SCB.

In the charge operation mode of the SCES, switches S_1 and S_2 are set at position Ch (charge), so that the DC/DC converter acts as a buck or step-down chopper. In this way, only the upper IGBT is switched while the lower one is kept off all the time. Since the super capacitor current is highly responsive to the voltage applied, being this relation especially increased by the SCES properties, i.e. the exceptionally low ESR and large capacitance, a hysteresis current control (HCC) method is proposed here for this operation mode. The HCC technique with fixed-band gives good performance, ensuring fast response and simplicity of implementation but with the main drawback of varying the IGBT switching frequency and then generating a variable-frequency harmonic content. To overcome this problem, an adaptive hysteresis (nearly constant-frequency) current control technique (AHCC) for the DC/DC converter operating in continuous conduction mode of I_{SCB} is proposed (Ninkovic, 2002). The basic concept in this hysteresis control is to switch the buck DC/DC converter IGBT to the opposite state (on-off) whenever the measured super capacitor current reaches above or below a given boundary determined by the hysteresis band. The AHCC is based on cycle-by-cycle hysteresis calculator, which generates the hysteresis window that will keep the switching frequency in a very narrow band centred on a programmed average value. The accuracy remains outstanding, and the ripple content allows the use of a smaller filter than typical HCC. This technique gives good performance, ensuring fast response and simplicity of implementation. In this way, the charging of the UCES is rapidly accomplished at a current I_{Thres} computed by the external level control, provided that the voltage V_{SCB} is below the limit V_{SCBmax}. During this process, the VSI DC bus voltage is controlled at a nearly constant level via a PI control of the error signal between the reference and the measured voltage at the DC bus, in such a way that a balance of powers are obtained between the DSTATCOM inverter and the SCB. When the super capacitor maximum voltage is reached, the DC/DC buck converter IGBT is switched-off and the charge operation mode of the UCES is changed to the stand-by mode.

In the discharge operation mode of the SCES, switches S_1 and S_2 are set at position Dsch (discharge), so that the DC/DC converter acts as a boost or step-up chopper. In this way, only the lower IGBT T_{bst} is switched while the upper one is kept off at all times. Since the ultracapacitor discharge current is to be controlled by the DC/DC converter input impedance, a pulse-width modulation (PWM) control technique with double-loop control

strategy is proposed to be employed. This control mode has low harmonic content at a constant-frequency and reduced switching losses. In this way, the discharging of the SCES is rapidly accomplished at a level determined by the external level control, provided that the voltage V_{SCB} is above the limit V_{SCBmin}. During this process, the VSI DC bus voltage is regulated at a constant level via a PI control of the error signal between the reference and the measured voltage at the DC bus. Thus, by adjusting the duty cycle D of the boost chopper, the energy released from the ultracapacitor unit towards the VSI is regulated. An inner current loop is introduced into the voltage loop to achieve an enhanced dynamic response of the ultracapacitor current I_{SCB}, so that rapid response can be derived from the DC/DC boost converter.

5.3.3 Internal level control design

The internal level (right side of Fig. 17) is responsible for generating the switching signals for the twelve valves of the DSTATCOM three-level VSI, in the same way as the SMES internal control, and for both IGBTs of the buck/boost DC/DC converter. This level is mainly composed of a line synchronization module, the three-phase three-level SPWM firing pulses generator, an adaptive hysteresis current control generator for the IGBT of the buck chopper and a PWM generator for the IGBT of the boost DC/DC converter.

6. Dynamic modelling and control design of the FES system

Flywheel energy storage (FES) systems are mainly composed of several sub-systems, such as the rotor, the bearing system, the driving motor/generator and housing, and the PCS for coupling to the electric grid. Unlike SMESs and SCESs that operate at DC voltage levels, FES systems use an electric machine, such as a permanent magnet synchronous machine (PMSM) in the proposed topology, in order to generate a set of three sinusoidal voltage waveforms phase-shifted 120º between each other, with variable amplitude and frequency. On the other hand, the power conditioning system provides an electronic interface between the two AC electric systems, i.e. the electric utility grid and the flywheel machine, allowing the grid-connected operation of the DES. The proposed detailed model and the global control scheme of an economical and reliable FES system for applications in the distribution level is depicted in Fig. 18.

6.1 Power conditioning system of the FES

The power conditioning system (PCS) used for connecting RESs to the distribution grid requires the flexible, efficient and reliable generation of high quality electric power. The PCS proposed in this work is composed of a back-to-back AC/DC/AC converter that fulfills all the requirements stated above. Since the variable speed rotor of the flywheel is directly coupled to the synchronous motor/generator, this later produces an output voltage with variable amplitude and frequency. This condition demands the use of an extra conditioner to meet the amplitude and frequency requirements of the utility grid, resulting in a back-to-back converter topology (Suvire & Mercado, 2008). Two voltage source inverters compose the core of the back-to-back converter, i.e. a machine-side inverter and a grid-side one. As can be clearly seen for Fig. 18, the grid-side VSI is part of the well-known DSTATCOM device employed in both SMESs and SCESs systems.

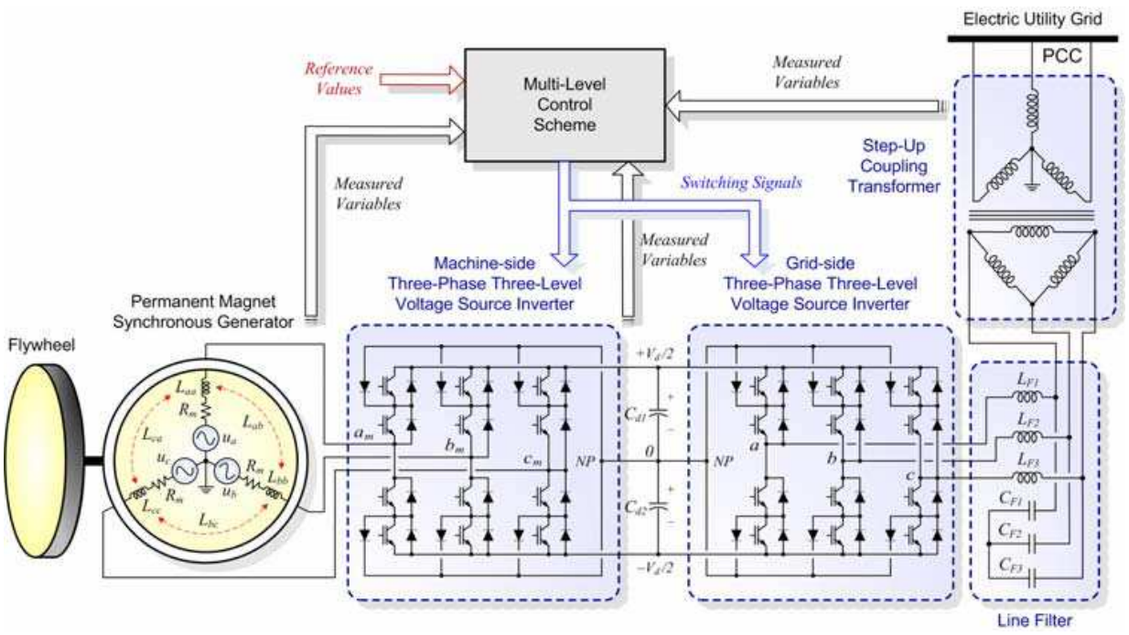


Fig. 18. Full detailed model of the proposed flywheel system

6.1.1 Three-phase three-level DSTATCOM

As in both prior cases of the SMES and SCES system, the key part of the PCS is the DSTATCOM device, and utilizes the same topology previously described. The proposed DSTATCOM essentially consists of a three-phase three-level VSI made with IGBTs, as shown in Fig. 18 (right side). This device is shunt-connected to the distribution network by means of a coupling transformer and the corresponding line sinusoidal filter. Equations governing the steady-state dynamics of the ideal DSTATCOM in the *dq* reference frame were previously derived and summarized in equation (12).

6.1.2 Two-quadrant three-level AC/DC converter

The machine-side three-phase three-level VSI corresponds to an AC/DC switching power inverter using high-power insulated gate bipolar transistors (IGBTs). This device is analogous to the grid-side VSI (DSTATCOM part) and converts the variable amplitude and frequency output voltage of the PMSM into a roughly constant DC voltage level of the DSTATCOM inner bus. The VSI structure proposed is equal to the DSTATCOM VSI, i.e. a three-level twelve pulse NPC structure, instead of a standard two-level six pulse inverter structure. This three-level VSI topology generates a more smoothly sinusoidal output voltage waveform than conventional two-level structures without increasing the switching frequency and effectively doubles the power rating of the VSI for a given semiconductor device while maintaining high dynamic performance. This feature is essential in order to reduce power loses in the electric machine and then for improving the efficiency of the entire FES system, but also mainly to maintain the charge balance of the intermediate DC bus capacitors, thus avoiding contributing to both AC systems (PMSG and electric grid) with additional distortion. Equations governing the steady-state dynamics of the ideal machine-side VSI in the *dq* reference frame are basically derived from the DSTATCOM VSI mathematical model described by equation (12), but modifying the electrical parameters of the grid by the PMSM as will be later explained.

6.2 Flywheels

The flywheel energy storage system is based on the principle that a rotating mass at high speed can be used to store and retrieve energy. Thus, the flywheel itself is just a mass with high inertia, which is coupled to an electric machine to form the DES. The use of a PMSM is proposed for this application since results very attractive due to advantages such as the inclusion of self-excitation, high power factor, and especially high efficiency and fast dynamic response (Zhou & Qi, 2009). This means that modelling the electrical behaviour of the system can be determined by modelling a PMSM with high inertia.

The permanent magnet synchronous machine can be electrically described using a simple equivalent circuit with an armature equation including back electromotive forces (emfs). This model assumes that saturation is neglected, the induced emfs are sinusoidal, the eddy currents and hysteresis losses are negligible, and that there are no field current dynamics (Samineni et al., 2003). In this way, voltage equations for the PMSM are given by:

$$\begin{bmatrix} u_{am} \\ u_{bm} \\ u_{cm} \end{bmatrix} - \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \left(\mathrm{R_m} + s\mathrm{L}\right) \begin{bmatrix} i_{am} \\ i_{bm} \\ i_{cm} \end{bmatrix}, \tag{26}$$

where:

$$\mathrm{R_m} = \begin{bmatrix} R_m & 0 & 0 \\ 0 & R_m & 0 \\ 0 & 0 & R_m \end{bmatrix}, \ \mathrm{L} = \begin{bmatrix} L_{aa} & L_{ab} & L_{ac} \\ L_{ab} & L_{bb} & L_{bc} \\ L_{ac} & L_{bc} & L_{cc} \end{bmatrix}, \tag{27}$$

being:

u_{im} (i=a, b, c): stator phase voltages in abc coordinates

u_i: back emfs in abc coordinates

i_{im}: stator currents in abc coordinates

L_{ij}: stator winding inductances, including self and mutual ones (combinations of i and j=a, b, c). It is considered symmetry for mutual inductances, so that L_{ij}=L_{ji}

The terminal voltages applied from the machine-side VSI to the stator, u_{im} and the back emfs, u_i are balanced three-phase voltages, being the later defined as follows:

$$u_i = \omega_s \Psi_{mi}, \tag{28}$$

with:

Ψ_{mi}: permanent-magnet flux linkage in abc coordinates

ω_s: synchronous angular speed of the electric machine, aka rotor electrical speed.

Since there is no functional equation for instantaneous reactive power in the abc reference frame, it is useful to apply a transformation to the synchronous-rotating orthogonal d-q set aligned with the rotor flux to equations (26) and (27) in order to analyze the electric machine. This is performed by applying Park's transformation defined in equation (3), replacing ω with the rotor electrical speed, ω_s and defining the q-axis to be always coincident with the instantaneous stator mmfs, which rotate at the same speed as that of the rotor (yielding u_q equals $|u|$, while u_d is null). This is beneficial because any AC signals that spins at w_s become DC quantities in the rotor dq frame. Then, by neglecting the zero sequence components, equations (29) and (30) are derived.

$$\begin{bmatrix} u_{dm} \\ u_{qm} \end{bmatrix} - \begin{bmatrix} u_d \\ u_q \end{bmatrix} = \left(\mathrm{R_m} + s\mathrm{L'_s}\right) \begin{bmatrix} i_{dm} \\ i_{qm} \end{bmatrix} + \begin{bmatrix} -\omega_s & 0 \\ 0 & \omega_s \end{bmatrix} \mathrm{L'_s} \begin{bmatrix} i_{qm} \\ i_{dm} \end{bmatrix}, \tag{29}$$

where:

$$\mathrm{R_m} = \begin{bmatrix} R_m & 0 \\ 0 & R_m \end{bmatrix},\ \mathrm{L'_s} = \begin{bmatrix} L_d & 0 \\ 0 & L_q \end{bmatrix},\ u_d = \omega_s \Psi_{qm},\ u_q = \omega_s \Psi_{dm} \tag{30}$$

Flux Linkages in the *dq* frame can be expressed in terms of the stator currents, inductances, and the flux linkage due to the permanent magnets of the rotor linking the stator, Ψ_m as:

$$\Psi_{dm} = L_d i_{dm} + \Psi_m \tag{31}$$

$$\Psi_{qm} = L_q i_{qm} \tag{32}$$

By rewriting equation (29), the following state equation can be obtained:

$$s \begin{bmatrix} i_{dm} \\ i_{qm} \end{bmatrix} = \begin{bmatrix} \frac{-R_m}{L_d} & \omega_s \\ -\omega_s & \frac{-R_m}{L_q} \end{bmatrix} \begin{bmatrix} i_{dm} \\ i_{qm} \end{bmatrix} + \begin{bmatrix} \frac{u_{dm}}{L_d} \\ \frac{u_{qm} - |u|}{L_q} \end{bmatrix}, \tag{33}$$

being $|u| = \omega_s \Psi_m$

In the rotor *dq* frame, the active and reactive powers are calculated as follows:

$$p = \frac{3}{2}(v_{dm} i_{dm} + v_{qm} i_{qm}) \tag{34}$$

$$q = \frac{3}{2}(v_{dm} i_{qm} - v_{qm} i_{dm}) \tag{35}$$

The developed electromagnetic torque of the electric machine takes the following convenient form:

$$T_e = \frac{3}{2} p_p \left[\psi_m i_{qm} + (L_d - L_q)\, i_{dm} i_{qm}\right], \tag{36}$$

where p_p is the number of pole-pairs of the PMSM.

For a non-salient-pole machine, as the employed here, the stator winding direct and quadrature inductances L_d and L_q, are approximately equal. Indeed this application uses a surface mount permanent magnet synchronous machine (SPMSM) which has zero saliency. This means that the direct-axis current i_{dm} does not contribute to the electrical torque T_e, as described by equation (37). The key concept is to keep null the direct current, i_{dm} by an appropriate transformation synchronization in order to obtain maximal torque with minimum current, i_{qm}.

$$T_e = \frac{3}{2} p_p\, \psi_m i_{qm} = K_{Te}\, i_{qm} \tag{37}$$

Using the convenient forms of active and reactive powers in the *d-q* reference frame, it can be derived a simple controller for the proposed machine.
The FES system rotor dynamics can be mechanically modelled using a single-mass model given by equation (38). In other word, as previously discussed, the flywheel is modelled as an additional inertia to the rotor of the PMSM.

$$T_e = T_l + B\omega_m + J_c \frac{d\omega_m}{dt}, \tag{38}$$

where:
T_l: load torque
B: viscous friction coefficient
J_c: combined inertia moment of the FES system (PMSM inertia, J_m plus flywheel rotor inertia, J_f)
ω_m: rotor mechanical speed (whereas ω_s is the rotor electrical speed)
Solving equation (38) for the rotor mechanical speed, it is obtained:

$$\omega_m = \int \left(\frac{T_e - T_l - B\omega_m}{J_c} \right) dt, \tag{39}$$

and

$$\omega_m = \frac{\omega_r}{p_p} \tag{40}$$

As can be noted, the flywheel rotor mechanical speed depends on the torque, the friction coefficient and on the inertia of the coupling flywheel-electric machine.
The machine torque can be then easily defined by the *emf* power, P_e:

$$T_e = \frac{P_e}{\omega_m} \tag{41}$$

The amount of energy drawn from the flywheel unit is directly proportional to the combined inertia of the flywheel-machine and to the change in rotation speed (ω_{mi}–initial and ω_{mf}–final speeds), as given by equation (42).

$$E_{FES} = \frac{1}{2} J_c \left(\omega_{mi}^{\,2} - \omega_{mf}^{\,2} \right) \tag{42}$$

6.3 Proposed Control Scheme of the FES System

As in both prior cases of the SMES and SCES system, the proposed three-level control scheme of the FES system consists of an external, middle and internal level. Since each control level has its own control objectives, independently of the other levels, some structures are identical to previous DES systems controllers. Its design is also performed in the synchronous-rotating *d-q* reference frame, as depicted in Fig. 19. This arrangement has the goal of rapidly and simultaneously controlling the reactive power generated by the DSTATCOM and the active power provided by the FES system during the charging/discharging process.

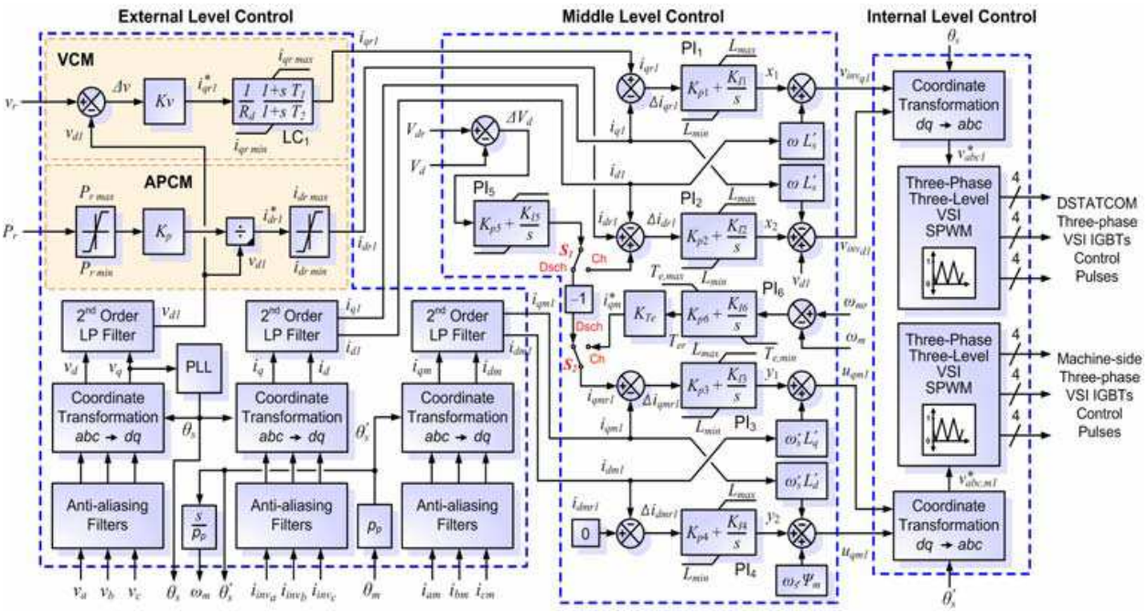


Fig. 19. Multi-level control scheme of the FES system

6.3.1 External level control design

As in the earlier both DES cases described, the external level control, which is outlined in Fig. 19 (left side), is responsible for determining the active and reactive power exchange between the DSTATCOM-FES device and the electric grid. This control strategy is designed for performing the same major control objectives, i.e. VCM with only reactive power compensation capabilities produced locally by the DSTATCOM and APCM for dynamic active power exchange between the FES and the microgrid. The only blocks added in the case of the FES control is the measurement system related to the PMSG. This block includes the stator instantaneous currents sensing and the *dq* transformation and filtering block in order to extract the fundamental components, i_{dm1} and $i_{dq1.}$ This method computes the rotor flux angle indirectly based on the measured rotor position, θ_m of the electric machine. As formerly described, the *q-axis* was defined always coincident with the instantaneous stator mmfs, such that only the quadrature-axis current i_{qm} contribute to the electrical torque T_e, this notably optimizing the machine torque and simplifying the middle level control design.

6.3.2 Middle level control design

The middle level control makes the expected output, i.e. positive sequence components of i_{dm} and i_{qm}, to dynamically track the reference values set by the external level. This level control design, which is depicted in Fig. 19 (middle side), is based on a linearization of the state-space averaged model of the FES system PCS. The dynamic performance of the proposed PCS, consisting of a back-to-back converter topology with two VSIs (a machine-side AC/DC converter and a grid-side DC/AC one), is described using equations (12) and (33), respectively. As can be noted, since all the presented DES devices utilize the same DSTATCOM topology as part of their respective PCSs, some algorithms corresponding to the middle level control are shared. The major difference is in the control of the AC/DC converter, which is now particular for the used electric machine drive (Toliyat et al., 2005).

Inspection of equation (33) shows a cross-coupling of both components of the PMSM output current through ω. Therefore, in order to fully decouple the control of i_{dm} and i_{qm}, appropriate control signals have to be generated. To this aim, two conventional PI controllers with proper feedback of the PMSM actual output current components are used, consequently responding in steady-state with no crosscoupling, as in the case of the DSTACOM VSI control.

Control of the FES system is in essence controlling the motor/generator that is coupled to the flywheel. The FES PCS has basically three modes of operation, namely the charge mode, the stand-by or free-wheeling mode and the discharge mode.

A typical setup when energy is stored into the device is allowing electrical power to flow into the electric machine (PMSM working as a motor), creating a torque which accelerates the speed of the rotating mass (flywheel). In the charge operation mode of the FES, switches S_1 and S_2 are set at position Ch (charge), so that the DC bus voltage is regulated by the DSTATCOM inverter (grid-side VSI), while the machine-side inverter is used for controlling the rotor mechanical speed. In this startup stage, since a high torque is required, a current control is essential. Thus, a reference torque command is employed from a speed PI controller acting on the speed error (ω_{mr}–ω_m). When the FES system maximum speed is reached, the PCS achieves the stand-by mode, which maintains stable the rotor speed.

When power is drawn from the FES device, the rotating mass is allowed to decelerate (PMSM working as a generator) and apply a torque to the electric machine, which discharges power at the machine terminals to the electric grid. In the discharge operation mode of the FES, switches S_1 and S_2 are set at position Dsch (discharge), so that the FES system itself regulates the DC bus voltage by decelerating the flywheel, when T_e is obtained from PI voltage controller acting on the voltage error (V_{dr}–V_d). Additionally, a negative gain is needed in the PI voltage controller because when the FES system releases energy, the current flows from the machine-side converter to the grid-side converter (opposite to the charge mode).

6.3.3 Internal level control design

The internal level (right side of Fig. 19) is responsible for generating the switching signals for the twelve IGBTs of the DSTATCOM three-level VSI (grid-side), and for the twelve IGBTs of the machine-side three-level VSI. This level is mainly composed of line and flux synchronization module, and the three-phase three-level SPWM firing pulses generator for both inverters of the back-to-back converter.

7. Digital simulation results

The distribution power system used to validate the proposed full detailed modelling and control approaches of the selected DSTATCOM-DES devices is depicted in Fig. 20 as a single-line diagram. This power system implements a substation feeding an electrical microgrid, which includes the selected advanced DES units. The small microgrid does not include any distributed generation for simplifying the study. The utility system is represented by a classical single machine-infinite bus type (SMIB) system. This basic 7-bus distribution network operates at 25 kV/50 Hz, and implements a 50 MW short circuit power level infinite bus through a Thevenin equivalent. A set of linear loads are grouped at bus 4 in the microgrid, and are modelled by constant impedances. A microgrid central breaker

(MGCB) with automatic reclosing capabilities is employed for the interconnection of the point of common coupling (PCC) of the MG (bus 4) to the substation of the utility distribution system through a 15 km tie-line. The proposed DSTATCOM-DES devices to be studied are placed at bus 4 and includes a 25 kV/1.2 kV step-up transformer with a ±1.5 MVA/2.5 kV DC bus DSTATCOM and an advanced 0.75 MW/4 MJ DES. DES devices included all previously modelled advanced ESSs, i.e. SMES, SCES and FES.

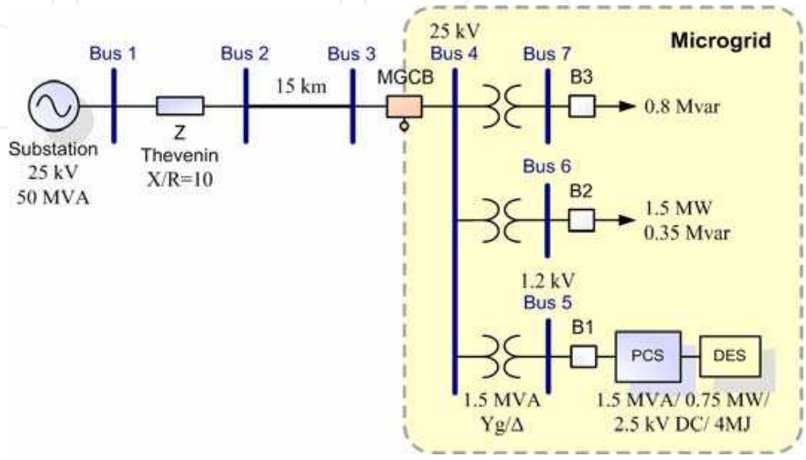


Fig. 20. Single-line diagram of the test power system with the microgrid containing DES

The dynamic performance of the proposed dynamic modelling and control schemes of the selected DES systems is assessed through digital simulations carried out in the MATLAB/Simulink environment (The MathWorks Inc., 2009), by using SimPowerSystems.
For full dynamic performance studies, independent control of active and reactive powers exchanged between the DES and the electric grid is carried out. To this aim, all DES systems are firstly charged to be initialized at the same energy level of 2 MJ (half capacity). Thus, the two control modes of the DSTATCOM-DES systems are analyzed using two case studies.
The first case study (Scenario 1) corresponds to the DSTATCOM-DES device operating in VCM. In this case, the topology presented in the test system without the activation of the DSTATCOM-DES, the so-called base case, is used as a benchmark for the reactive power studies. Under this situation, the distribution utility feeds the load of 1.5 MW/0.35 Mvar, i.e. only the breaker B2 is closed. The supply voltages and currents are balanced and in steady-state. The voltage obtained at bus 3 in this steady-state is 0.94 p.u. (base voltage at 25 kV). At t=0.4 s, a reactive load of 0.8 Mvar is suddenly connected at bus 3 by closing B3 and later disconnected at t=0.6 s. Fig. 21 presents the system response before, during and after the contingency described. As can be seen, the increase of the inductive reactive load produces a voltage sag (aka dip) at bus 3 of near 21 % respect to the value in steady-state during 200 ms, until the reactive load is disconnected. Although the DSTATCOM-DES is not operating, i.e. not exchanging power with the grid as can be seen from response of d and q current components, the DSTATCOM-DES is connected (B1 is closed) and still forced to generate an output voltage waveform accurately synchronized in amplitude and in phase with the grid positive sequence voltage at the PCC for being ready to be quickly activated when necessary. The DSTATCOM-DES signals of Fig. 21 were introduced for comparison purposes with the subsequent cases studied.

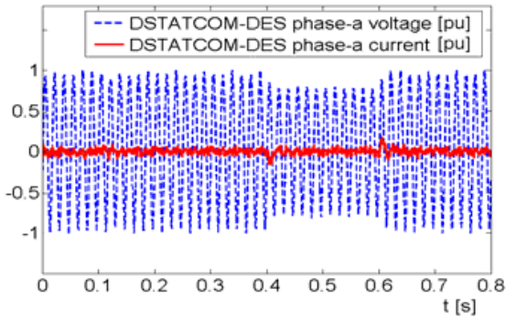
The second case study (Scenario 2) corresponds to the DSTATCOM-DES device operating in APCM. This case study is particular for each energy storage technology considered, since each DES device modifies in a different way the dynamics of the DSTATCOM device.
The SMES system studied is composed of a stack of 4 Bi-2212 HTS coils with a total equivalent nominal inductance of 8.3 H operated at 30 K, and a critical current of 1.2 kA. The SMES arrangement was initialized at about 2 MJ, so that the consequent initial coil current is set at about 722 A. The SCES system is made up of a string of 468 Maxwell Boostcap BCAP0010 (2600 F/2.5 V/20ºC) super capacitors with a total equivalent nominal capacitance of about 5.6 F and a maximum voltage of 1170 V at 20ºC. The super capacitors bank was also initialized at about 2 MJ, so that the corresponding initial voltage is fixed at near 850 V. In the case of the proposed FES system, it consists of a high speed flywheel with operating speed range of 14 000 rpm–28 000 rpm and total system inertia of 14e-3 kg-m². The PMSM is a three phase, two pair poles one and operates in the frequency range of 467 Hz–933 Hz. Since, the FES system is also initialized at 2 MJ, the initial rotor speed is fixed at about 22 000 rpm. The base case used for this study is the same previously described, but considering only the steady-state scenario prior to the voltage sag, i.e. until 0.4 s with the utility grid feeding only the load of 1.5 MW/0.35 Mvar (breaker B2 closed). In this case, the topology presented in the test system without the activation of the DSTATCOM-DES (base case) is also used as a benchmark for the APCM case study.

7.1 Scenario 1: Connection of the DSTATCOM-DES in voltage control mode

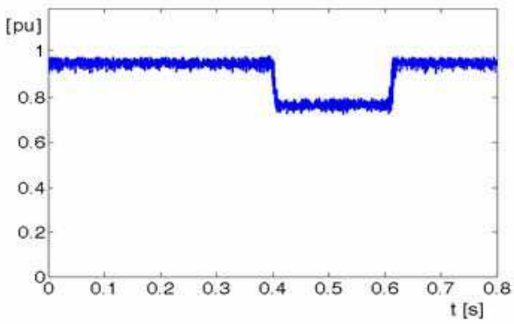
The dynamic response in controlling the reactive power locally generated by the DSTATCOM-DES independently of the active power exchange is now studied through the simulation results of Fig. 22. The good performance of the voltage regulator of the DSTATCOM device is evidently depicted by the rapid compensation of reactive power and the consequent improvement of the voltage profile, after activation at t= 0.2 s, and even more during the voltage sag between 0.4 s and 0.6 s. As can be noted from actual and reference values of i_q, the only reactive power exchange with the utility system, independent of the active power, allows efficiently regulating the voltage at bus 3, from 0.94 p.u. in the base case up to the reference value of near 1 p.u., and particularly during the sag, when the voltage goes down to 0.75 p.u. in the base case and the VCM allows restoring quickly the voltage back to about 1 p.u. and thus mitigating completely the voltage perturbation. The DSTATCOM-DES provides near 0.83 Mvar of capacitive reactive power for improving the voltage profile during the sag and about 0.22 Mvar during the previous steady-state. As a consequence of the global improvement of the voltage profile at bus 3 (PCC), the active power demanded by loads is slightly enlarged. The decoupling characteristics between the active and reactive powers are excellent because of the full decoupled current control strategy implemented in the *d-q* frame. It is significant to note that, since only reactive power is exchanged with the grid in this control mode, there is no need for energy storage or any other external energy source. In fact, this reactive power is locally and electronically generated just by the DSTATCOM, so that the results of Fig. 21 and 22 are valid for any DES coupled to the DSTATCOM. This DES is maintained idle (or in stand-by mode) during the entire VCM operation by using the electronic interface which couples it to the DSTATCOM. Since in this control mode only reactive power is injected/absorbed at the PCC, the maximum apparent power of the DSTATCOM VSI, i.e. 1.5 MVA, can be used for compensating deeper sags. When active power is included in the control goals, some

criterion of dynamic distribution of limits should be considered according to priorities set by the DSTATCOM-DES operator.

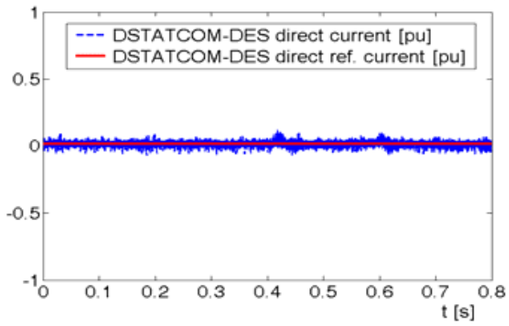
DSTATCOM-DES phase voltage and current, v_a, i_a



Bus 3 (PCC) voltage, v_d



DSTATCOM-DES actual and ref. current, i_d, i_{dref}



DSTATCOM-DES actual and ref. current, i_q, i_{qref}

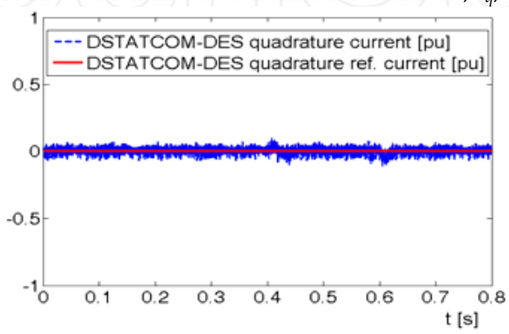
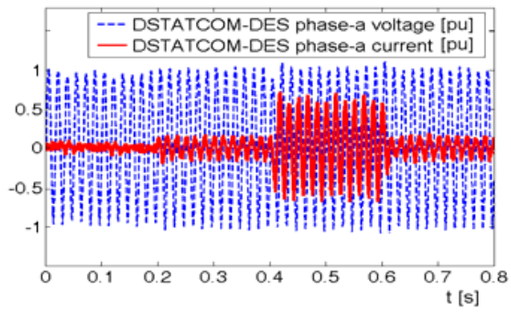
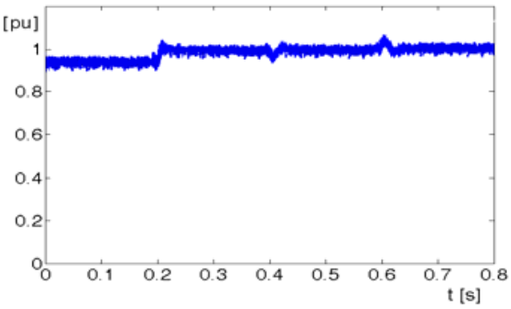


Fig. 21. Simulation results for the base case (with no activation of DSTATCOM-DES)

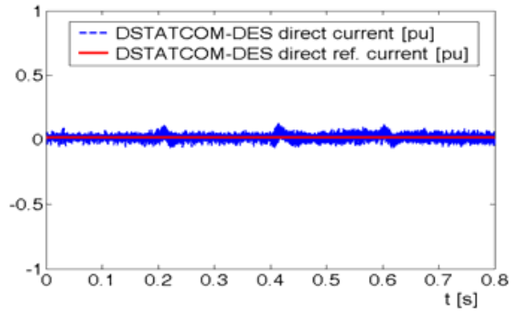
DSTATCOM-DES phase voltage and current, v_a, i_a



Bus 3 (PCC) voltage, v_d



DSTATCOM-DES actual and ref. current, i_d, i_{dref}



DSTATCOM-DES actual and ref. current, i_q, i_{qref}

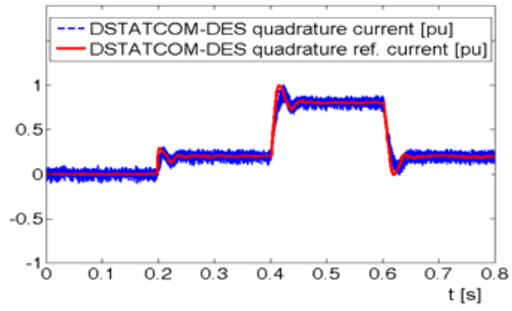


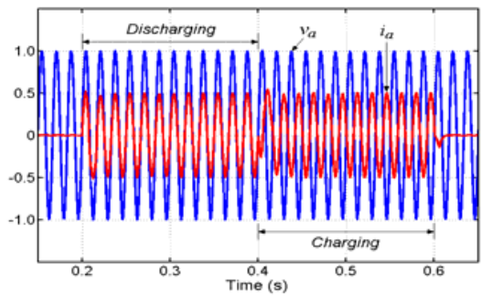
Fig. 22. Simulation results for the case with the DSTATCOM-DES in VCM

7.2 Scenario 2: Connection of the DSTATCOM-DES in active power control mode

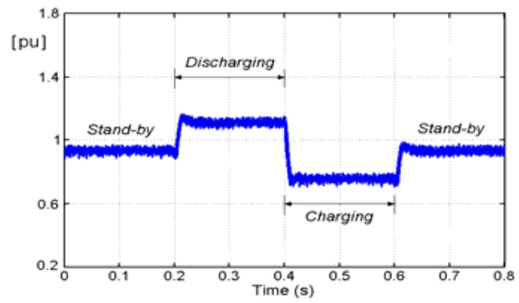
The full dynamic response in controlling the active power flow injected/absorbed by the DES unit independently of the reactive power generated is now analyzed through the

simulation results of Fig. 23. This case study is particular for each energy storage technology, but the three DESs selected for power applications in microgrids shown some almost coincident responses, so that the study is focused on the SMES device dynamic behaviour analysis and the difference with the other devices will be remarked when is required. In this case study, an active power command P_r is set to make step changes of 0.5 MW during 200 ms as much in the discharge as in the charge modes of operation with the VCM control scheme deactivated. Thus, reactive power is not generated and the device is fully used to exchange active power with the microgrid. Under these circumstances, an active power of around 30 % of the active power demanded by the load is injected during the discharge mode and absorbed during the charge mode of the SMES coil. As can be noted from actual and reference values of i_d and i_q shown in Fig. 23 only active power is rapidly exchanged with the utility system, in both discharge/charge modes of operation, independently of the reactive power. As can be seen, there exists a very low transient

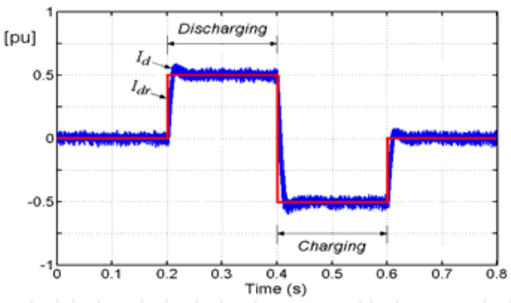
DSTATCOM-SMES phase voltage and current, v_a, i_a



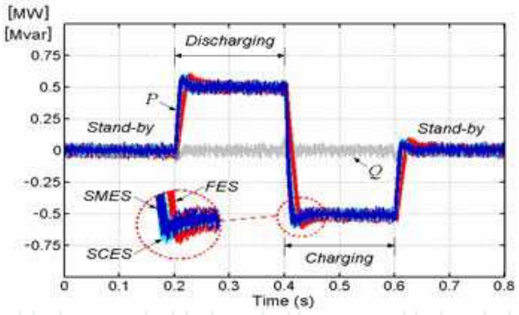
Bus 3 (PCC) voltage, v_d



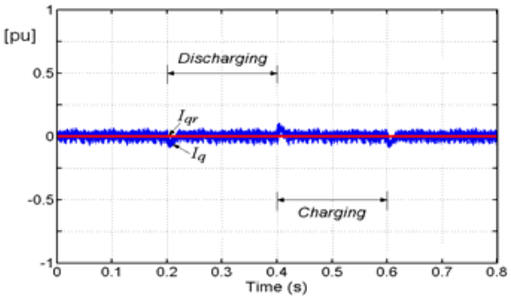
DSTATCOM-SMES actual and ref. current, i_d, i_{dref}



DSTATCOM-SMES active and reactive power



DSTATCOM-SMES actual and ref. current, i_q, i_{qref}



DSTATCOM-SMES coil current, i_{SC}

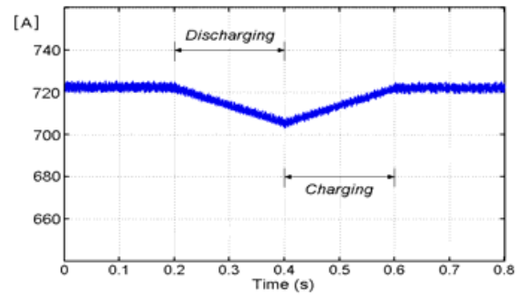


Fig. 23. Simulation results for the case with the DSTATCOM-DES in active power control mode

coupling between the active and reactive powers exchanged by the SMES due to the full decoupled current control strategy in the synchronous-rotating *d-q* reference frame. As expected, the phase ´a´ voltage at the PCC (bus 3) is in-phase with the SMES DSTATCOM output current during the active power injection (discharge mode) and in opposite-phase during the active power absorption (charge mode). This active power exchange produces substantial changes in the terminal voltage v_{d1}, because the test power grid studied is pretty weak. A significant issue to be noted is that the dynamic active power response of the SMES in APCM is very fast and better than the reactive power one in VCM. This is a consequence of the PI compensator included for voltage regulation at the PCC, which inevitably adds a lag in the response. As can be also seen from the comparison of transient responses of the three selected DES devices, SMESs and SCESs are the faster DES devices and response almost identically in one and a half cycle, with a settling time of approximately 30 ms. In the same way, the FES device is hardly slower than both later and its response exceed the two cycles with a settling time of almost 45 ms. The discharging and charging processes performed produce a variation of about 0.1 MJ of the energy stored in the DES devices. In the case of the SMES system, this variation is carried out by reducing the coil current from 722 A down to about 705 A and then returning to the initial value (without considering loses). The SCES bank obtains this energy variation by changing the terminal voltage from 850 V in the initial state to 828 V and then going back to the original state of charge. In the case of the FES device, the energy change is performed by decelerating the flywheel rotor speed from 22 000 rpm to 21 673 rpm and then accelerating back to the previous condition.

8. Conclusion

This chapter has thoroughly discussed the power application of advanced distributed energy storage systems in modern electrical microgrids. More specifically, of the various advanced storage systems nowadays existing, the three foremost ones for power applications have been considered, i.e. ultra capacitors, SMESs and flywheels. To this aim, major operating characteristics of these modern devices have been analyzed and a real detailed full dynamic model of all DES units has been studied. Moreover, a novel power conditioning system of the selected DES units to simultaneously and independently control active and reactive power flow in the distribution network level and a new three-level control scheme have been proposed, comprising a full decoupled current control strategy in the synchronous-rotating *d-q* reference frame. The dynamic performance of the proposed systems has been fully validated by digital simulations carried out by using SimPowerSystems of MATLAB/Simulink. The dynamic modelling approaches proposed describe the dynamic behaviour of the DES units over the frequency range from DC to several thousand Hertz with sufficient accuracy. The results show that the novel multi-level control schemes ensure fast controllability and minimum oscillatory behaviour of the DES systems operating in the four-quadrant modes, which enables to effectively increase the transient and dynamic stability of the power system. The improved capabilities of the integrated DSTATCOM-DES controllers to rapidly control the active power exchange between the DES and the utility system, simultaneously and independently of the reactive power exchange, permit to greatly enhance the operation and control of the electric system. The fast response DES devices show to be very effective in enhancing the distribution power quality, successfully mitigating disturbances such as voltage sags and voltage/current harmonic distortion, among others.

9. Acknowledgments

The author wishes to thank CONICET (Argentinean National Research Council for Science and Technology), IEE/UNSJ (Institute of Electrical Energy at the National University of San Juan) and ANPCyT (National Agency for Scientific and Technological Promotion) under grant FONCYT PICT 2005 – Cod. No. 33407, for the financial support of this work.

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Dynamic Modelling

Edited by Alisson V. Brito

ISBN 978-953-7619-68-8
Hard cover, 290 pages
Publisher InTech
Published online 01, January, 2010
Published in print edition January, 2010

When talking about modelling it is natural to talk about simulation. Simulation is the imitation of the operation of a real-world process or systems over time. The objective is to generate a history of the model and the observation of that history helps us understand how the real-world system works, not necessarily involving the real-world into this process. A system (or process) model takes the form of a set of assumptions concerning its operation. In a model mathematical and logical assumptions are considered, and entities and their relationship are delimited. The objective of a model – and its respective simulation – is to answer a vast number of “what-if” questions. Some questions answered in this book are: What if the power distribution system does not work as expected? What if the produced ships were not able to transport all the demanded containers through the Yangtze River in China? And, what if an installed wind farm does not produce the expected amount of energyt? Answering these questions without a dynamic simulation model could be extremely expensive or even impossible in some cases and this book aims to present possible solutions to these problems.

InTech Europe
University Campus STeP Ri
Slavka Krautzeka 83/A
51000 Rijeka, Croatia
Phone: +385 (51) 770 447
Fax: +385 (51) 686 166
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